Freescale Semiconductor
Application NoteWhite Paper

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MPC8536E PowerQUICC III Bring-Up Guide

This application note provides recommendations for new designs based on the MPC8536E PowerQUICC III family of integrated host communications processors (collectively referred to throughout this document as MPC8536E):

- MPC8536E
- MPC8536
- MPC8535E
- MPC8535

NOTE

Please see Appendix C of *MPC8536E PowerQUICC III Integrated Host Processor Family Reference Manual* for the differences between MPC8536 and MPC8535.

This document may also be useful for debugging newly designed systems by highlighting those aspects of a design that merit special attention during initial system startup.

For updates to this document, refer to the website listed on the back cover of this document.

Contents

1 Introduction

This section outlines recommendations to simplify the first phase of design. Before designing a system with a MPC8536E device, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

1.1 MPC8536E Overview

This section provides a high-level overview of MPC8536E features. Figure 1 shows the major functional units within the device.

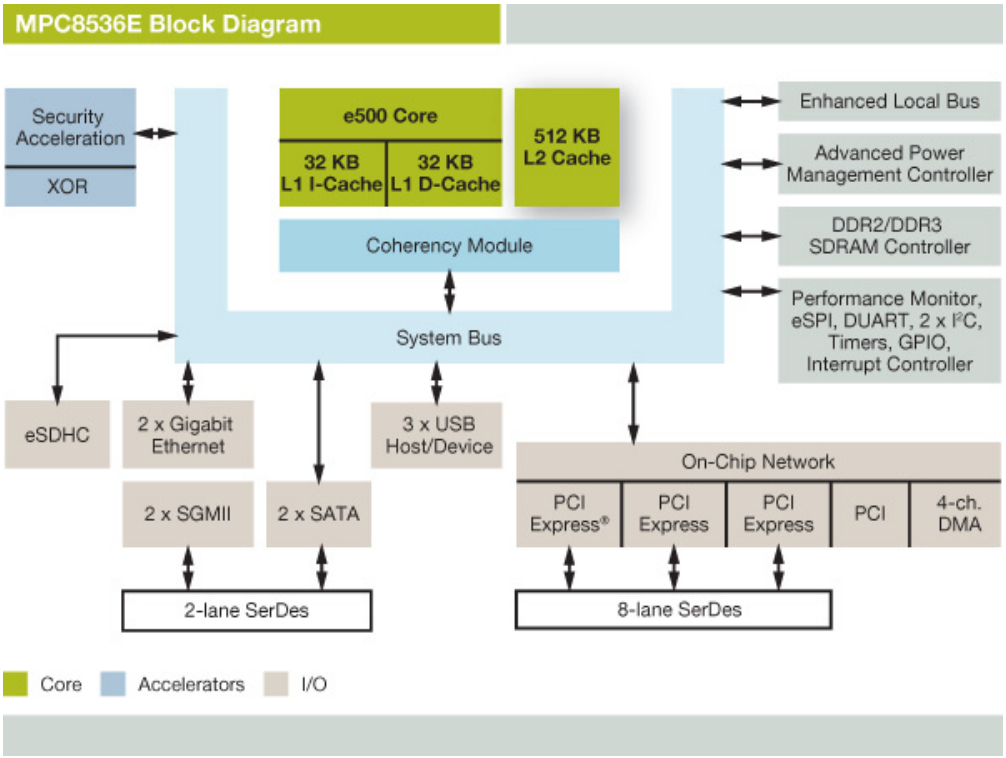


Figure 1. MPC8536E Block Diagram

1.2 References

Some references listed may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

1.2.1 Collateral

Table 1. Collateral

Document Title	Document ID
MPC8536E PowerQUICC III Integrated Host Processor Family Reference Manual	MPC8536ERM
Errata to MPC8536E PowerQUICC III Integrated Host Processor Family Reference Manual	MPC8536ERMAD

Table 1. Collateral (continued)

Document Title	Document ID
Device Errata for the MPC8536E PowerQUICC III	MPC8536ECE
MPC8536E PowerQUICC III Integrated Processor Hardware Specifications	MPC8536EEC
MPC8535E PowerQUICC III Integrated Processor Hardware Specifications	MPC8535EEC
A Strategy for Routing the MPC8536E in a Six-Layer PCB	AN3444
PowerQUICC DDR2 SDRAM Controller Register Setting Considerations	AN3369
Programming the PowerQUICC III/PowerQUICC II Pro DDR SDRAM Controller	AN2583
Hardware and Layout Design Considerations for DDR2 SDRAM Memory Interfaces	AN2910
Hardware and Layout Design Considerations for DDR3 SDRAM Memory Interfaces	AN3940
Booting from On-Chip ROM	AN3659
Hardware Debugging Using the CodeWarrior IDE	AN3830
Implementing SGMII Interfaces on the PowerQUICC III	AN3869
Determining the I2C Frequency Divider Ratio for SCL	AN2919
PowerQUICC and QorIQ DDR3 SDRAM Controller Register Setting Considerations	AN4039

1.2.2 Tools

- Software
  - Boot Sequencer Generator Tool (I2CBOOTSEQ)
  - UPM Programming Tool (LBCUPMIBCG)
- Hardware
  - Development System (MPC8536DS) including schematics, bill of materials, board errata list, user's guide, and configuration guide
  - Advanced Development Kit (MPC8536-ADK), which runs Android operating system, including board errata, user's guide, and configuration guide.

1.2.3 Models

- IBIS (http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MPC8536E&fpsp=1&tab=Design_Tools_Tab or http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MPC8535E&fpsp=1&tab=Design_Tools_Tab)
- BSDL (http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MPC8536E&fpsp=1&tab=Design_Tools_Tab or http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MPC8535E&fpsp=1&tab=Design_Tools_Tab)

- Flowtherm (http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MPC8536E&fpsp=1&tab=Design_Tools_Tab)

NOTE

To ensure first path success, Freescale strongly recommends to use the IBIS models for board level simulations, especially for SerDes and DDR characteristics. Use the BSDL files in board verification, and the Flotherm model for a strongly recommended thermal simulation. Especially without forced cooling or constant airflow, a thermal simulation should not be skipped.

1.3 Device Errata

The device errata document (*MPC8536ECE*) describes the latest fixes and workarounds for the MPC8536E. The errata document should be thoroughly researched prior to starting a design with the respective MPC8536E device.

1.4 Boot Sequencer Tool

The MPC8536E features the boot sequencer to allow configuration of any memory-mapped register before the completion of power-on reset (POR). The register data to be changed is stored in an I^2C EEPROM. The MPC8536E requires a particular data format for register changes as outlined in the *MPC8536ERM*. The boot sequencer tool (I2CBOOTSEQ) is a C-code file. When compiled and given a sample data file, it will generate the appropriate raw data format as outlined in the *MPC8536ERM*. The file that is generated is an S-record file that can be used to program the EEPROM.

1.5 UPM Programming Tool

The UPM programming tool (LBCUPMIBCG) features a GUI for a user-friendly programming interface. It allows programming of all three of the MPC8536E UPM machines. The GUI consists of a wave editor, a table editor, and a report generator. The user can edit the waveform or RAM array directly. At the end of programming, the report generator will print out the UPM RAM array that can be used in a C-program.

1.6 Available Training

Our third-party partners are part of an extensive Design Alliance Program. The current training partners can be found on our website under Design Alliance Program at www.freescale.com/alliances.

Training material from past Freescale Technology Forums are also available. These trainings modules are a valuable resource for understanding the MPC8536E. This material is available at our website listed on the back cover of this document.

1.7 Product Revisions

Table 2 lists the processor version register (PVR) and system version register (SVR) values for the various MPC8536E derivatives of silicon.

Table 2. MPC8536E PowerQUICC III Product Revisions

Device Number	Device Revision	e500 v2 Core Revision	Processor Version Register Value	System Version Register Value	Note
MPC8536E	1.0	3.0	0x8021_0030	0x803F_0090	With Security
MPC8536	1.0	3.0	0x8021_0030	0x8037_0090	Without Security
MPC8535E	1.0	3.0	0x8021_0030	0x803F_0190	With Security
MPC8535	1.0	3.0	0x8021_0030	0x8037_0190	Without Security
MPC8536E	1.1	3.0	0x8021_0030	0x803F_0091	With Security
MPC8536	1.1	3.0	0x8021_0030	0x8037_0091	Without Security
MPC8535E	1.1	3.0	0x8021_0030	0x803F_0191	With Security
MPC8535	1.1	3.0	0x8021_0030	0x8037_0191	Without Security
MPC8536E	1.2	3.0	0x8021_0030	0x803F_0092	With Security
MPC8536	1.2	3.0	0x8021_0030	0x8037_0092	Without Security
MPC8535E	1.2	3.0	0x8021_0030	0x803F_0192	With Security
MPC8535	1.2	3.0	0x8021_0030	0x8037_0192	Without Security

2 Power

This section provides design considerations for the MPC8536E power supplies and power sequencing. For information on AC and DC electrical specifications and thermal characteristics for the MPC8536E, refer to the *MPC8536E PowerQUICC III Integrated Processor Hardware Specifications* document.

2.1 Power Supplies

The MPC8536E has a core voltage V_{DD_core}, a platform voltage V_{DD_plat}, and SerDes voltages SV_{DD} and XV_{DD}, that operate at a lower voltage than the I/O voltages BV_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and TV_{DD}. The core voltage and platform voltage, 1.0 V (±5%), are supplied across V_{DD_core} or V_{DD_plat} and GND, respectively.

NOTE

V_{DD_core} is 1.1 V (±5%) for the 1500 MHz part number.

The I/O blocks are supplied with:

- 1.8 V (±5%) or 2.5 V (±5%) or 3.3 V (±5%) across BV_{DD} and GND
- 1.5 V (±5%) or 1.8 V (±5%) across GV_{DD} and GND
- 2.5 V (±5%) or 3.3 V (±5%) across LV_{DD} and GND

- 3.3 V (±5%) across OV_{DD} and GND
- 1.0 V (±5%) across SV_{DD} and GND
- 2.5 V (±5%) or 3.3 V (±5%) across TV_{DD} and GND
- 1.0 V (±5%) across XV_{DD} and GND

Both LV_{DD} and TV_{DD} are used to supply the eTSEC interfaces on the device: LV_{DD} manages eTSEC1 and TV_{DD} manages eTSEC3. For the respective eTSEC, LV_{DD}/TV_{DD} equals the following:

- 3.3 V or 2.5 V for GMII, MII, RMII, TBI, or FIFO modes of operation
- 2.5 V for RGMII or RTBI modes of operation

2.2 Power Consumption

Operating mode power dissipation numbers (typical) are provided in the *MPC8536E PowerQUICC III Integrated Processor Hardware Specifications* (MPC8536EEC). Typical and thermal numbers are provided in MPC8536EEC to assist in the thermal design for the device. If the targeted junction temperature (T_J) of the MPC8536E in the system is not one of these two temperatures, a linear extrapolation of these two typical dissipation values can be used to estimate the power dissipation at the targeted junction temperature. The maximum, provided at 105/90 °C, is intended to assist in the power supply design selection.

The MPC8536EEC includes Maximum, Thermal, Typical, Doze, Nap, Sleep, and Deep Sleep power numbers.

2.3 Power Sequencing

The MPC8536E requires its power rails to be applied in a specific sequence in order to ensure proper device operation. Per MPC8536EEC, the requirements for power up are as follows:

- V_{DD_plat}, V_{DD_core} (if POWER_EN is not used to control V_{DD_CORE}), AV_{DD_n}, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD}, $S2V_{DD}$, TV_{DD}, XV_{DD}, $X2V_{DD}$
- [Wait for POWER_EN to assert], then V_{DD_core} (if POWER_EN is used to control V_{DD_core})
- GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

The purpose of the sequence is to guarantee the state of the DDR signals at reset. In order to guarantee MCKE low during power up (as should be attempted per the JEDEC JESD79-2C specification), the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, then the sequencing of GV_{DD} is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD_core} supply, the I/Os associated with that I/O supply may drive a logic one or zero during power up, and extra current may be drawn by the device.

During the Deep Sleep state, the V_{DD} core supply is removed. But all other power supplies remain applied. Therefore, there is no requirement to apply the V_{DD} core supply before any other power rails when the silicon waking from Deep Sleep.

2.4 PLL Power Supply Filtering

Each of the PLLs is provided with power through independent power supply pins (AV_{DD_PLAT}, AV_{DD_CORE}, AV_{DD_DDR}, V_{DD_LBIU}, AV_{DD_PCI}, and AV_{DD_SRDS}, respectively). Preferably these voltages will be derived directly from V_{DD} through a low-frequency filter scheme.

While there are a number of ways to reliably provide power to the PLLs, the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 2, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range.
If the PCI is run in synchronous mode, no filter is required for AV_{DD}_PCI.

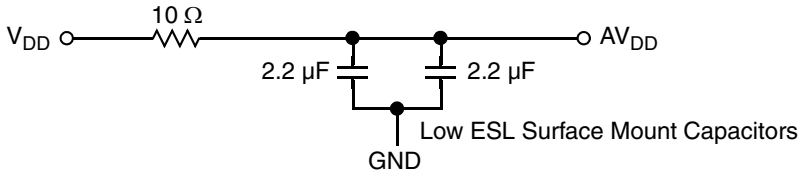
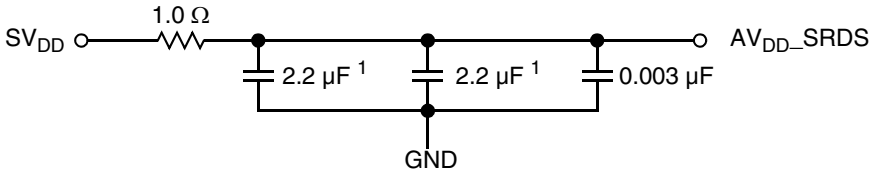


Figure 2. PLL Power Supply Filter Circuit

The AV_{DD}_SRDS*n* signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 3. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS*n* balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDS*n* balls. The 0.003-µF capacitor is closest to the balls, followed by the 1-µF capacitor, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. If the SerDes is not used, a filter for AV_{DD}_SRDS is not required.



1. An 0805 sized capacitor is recommended.
2. AVDD_SRDS should be a filtered version of SV_{DD}.
3. Signals on the SerDes interface are fed from the XV_{DD} power plane.

Figure 3. SerDes PLL Power Supply Filter

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits.

These filters are a necessary extension of the PLL circuitry and are to what the device is specified. Any deviation from the recommended filters are done at the customer's risk.

2.5 Power Supply Decoupling

The MPC8536E requires a clean, tightly regulated source of power. The system designer should place at least one decoupling capacitor at each V_{DD} and B/G/L/O/TV_{DD} pin of the device. These decoupling capacitors should have a value of 0.01 or 0.1 µF and receive their power from separate V_{DD}, B/G/L/O/TV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

In addition, several bulk storage capacitors should be distributed around the PCB to feed the V_{DD} and B/G/L/O/TV_{DD} planes, to enable quick recharging of the smaller chip capacitors.

The capacitors should be placed as close as possible to the processor. The capacitors need to be selected to work well with the power supply so as to be able to handle the MPC8536E dynamic load requirements. The customer should work closely with their power supply vendor to choose for the correct value and type of capacitors for good clean power.

If the SerDes is used, it requires a clean, tightly-regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver:

- The board should have at least 10 × 10 nF SMT ceramic chip capacitors as close as possible to the supply balls of the device.
- There should be a 1 µF ceramic chip capacitor from each SerDes supply (SV_{DD} and XV_{DD}) to the board ground plane on each side of the device.
- Between the device and any SerDes voltage regulator there should be a 10 µF, low ESR SMT tantalum chip capacitor and a 100 µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

2.6 Power Supplies Checklist

Table 3 provides a summary power supply checklist for the designer.

Table 3. Power Supply Checklist

Item	Description	Completed
1	All power supplies have a voltage tolerance no greater than 5% from the nominal value	
2	eTSEC supplies are chosen according to the mode of operation used	
3	Power supply selected is based on maximum power dissipation	
4	Thermal design is based on Thelma power dissipation	
5	Power-up sequence is less than 50 ms	
6	If POWER_EN is used to control V_{DD_CORE}, apply V_{DD_CORE} after POWER_EN asserts	
7	Power sequencing is understood and based on whether or not garbage data written to DDR is a concern	
8	Recommended PLL filter circuit is applied to AV_{DD}_PLAT, AV_{DD}_CORE, and AV_{DD}_LBIU	
9	If PCI is used in asynchonous mode, then the recommended PLL filter circuit is applied to AV_{DD}_PCI. However, If the PCI is used in synchronous mode, no filter is required for AV_{DD}_PCI.	
10	If SerDes is used, then the recommended PLL filter circuit is applied to AV_{DD}_SRDS. However, If the SerDes is not used, a filter for AV_{DD}_SRDS is not required	

Table 3. Power Supply Checklist

Item	Description	Completed
11	PLL filter circuits are placed as close to the respective AV_{DD} pin as possible	
12	Decoupling capacitors of 0.01 or 0.1 µF are placed at each V_{DD}, B/G/L/O/TV_{DD} pin	
13	Bulk capacitors are placed on each V_{DD}, B/G/L/O/TV_{DD} plane	
14	If SerDes is used, the recommended decoupling for S/XV_{DD} is used	

3 Power-on Reset and Reset Configurations

This section discusses power-on reset and reset configurations. A summary MPC8536E power-on reset (POR) and reset checklist is provided for the designer at the end of the section.

3.1 Configuration and Timing

Various device functions are initialized by sampling certain signals during the assertion of $\overline{\text{HRESET}}$. These POR inputs are either pulled high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while $\overline{\text{HRESET}}$ is asserted. $\overline{\text{HRESET}}$ must be asserted for a minimum on 100 µs. When $\overline{\text{HRESET}}$ de-asserts, the configuration pins are sampled and latched into registers and the pins then take on their normal output circuit characteristics.

Most of the configuration pins have an internally gated 20-kΩ pull-up resistor, enabled only during $\overline{\text{HRESET}}$. For those configurations in which the default state is desired, no external pull-up is required. Otherwise, a 4.7-kΩ pull-down resistor is recommended to pull the configuration pin to a valid logic low level. In the case where a configuration pin has no default, 4.7-kΩ pull-up or pull-down resistors are recommended for appropriate configuration of the pin.

An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device which drives the configuration signals to the MPC8536E when $\overline{\text{HRESET}}$ is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of $\overline{\text{HRESET}}$ (PLL configuration inputs must meet a 100-µs setup time to $\overline{\text{HRESET}}$), hold their values for at least 2 SYSCLK cycles after the de-assertion of $\overline{\text{HRESET}}$, and then release the pins to high impedance afterward for normal device operation.

3.2 Configuration Settings

The following table summarizes the customer configurable device settings. Refer to the *MPC8536ERM* for a more detailed description of each configuration option.

Table 4. User Configuration Options

Configuration Type	Functional Pins	Comments
Device	$\overline{\text{UART\_SOUT}}$[0:1]	Refer to Table 6 for POR and reset configurations
CCB clock PLL ratio	LA[28:31]	There is no default value for this PLL ratio; these signals must be pulled to the desired value. Refer to Section 5.1, “System PLL Ratio.”

Table 4. User Configuration Options (continued)

Configuration Type	Functional Pins	Comments
e500 core PLL ratio	LBCTL, LALE, LGPL2/LOE/LFRE	Default: 3.5:1 for this PLL ratio (e500 core:CCB clock). Refer to Section 5.2, "e500 Core PLL Ratio."
DDR PLL ratio	TSEC_1588_TRIG_OUT[0:1], TSEC_1588_CLK_OUT	There is no default value for this PLL ratio; these signals must be pulled to the desired value. Refer to Section 5.1, "System PLL Ratio."
System speed configuration	LGPL1/LFALE	Default value: 1. SYSCLK frequency is above 66 MHz. For the SYSCLK frequency is at or lower than 66 MHz, it should be low during HRESET. If this configuration is not set properly, behavior of the system may be unreliable.
Core speed configuration	LWE0/LBS0/LFWE	Default value: 1. Core frequency is above 800 MHz. For a low-speed operation, it should be low during HRESET. If this configuration is not set properly, behavior of the system may be unreliable.
Boot ROM location	TSEC1_TXD[7:4]	Default: Local bus GPCM (32-bit ROM)
Host/agent	LWE[1:3]/LBS[1:3]	Default: MPC8536E acts as the host processor/root complex on all interfaces.
SerDes1 I/O port selection	TSEC3_TXD[6:4]	Default: All three PCI Express ports active.
SerDes2 I/O port selection	TSEC1_TXD2,TSEC3_TXD2, TSEC_1588_PULSE_OUT1	Default: SerDes2 disabled. SATA1 and SATA2 disabled. eTSEC1 and eTSEC3 Ethernet interface does not use the SGMII interface
CPU boot	LA27	Default: e500 core is allowed to boot without waiting for configuration by an external master.
Boot sequencer	LGPL3/LFWP, LGPL5	Default: Boot sequencer is disabled. No I^2C ROM is accessed.
DDR SDRAM type	LGPL0/LFCLE	Default: DDR controller is configured for DDR2.
SerDes2 reference clock configuration	TSEC3_TXD3, TSEC_1588_PULSE_OUT2	SerDes2 expects a 100-MHz reference clock frequency for either SATA or SGMII functionality
eTSEC1 width	TSEC1_TX_ER	Default: eTSEC1 interface operates in standard width TBI, GMII, MII, or 8-bit FIFO mode.
eTSEC3 width	TSEC3_TX_ER	Default: eTSEC3 Ethernet interface operates in standard TBI, GMII, MII, or 8-bit FIFO mode.
eTSEC1 protocol	TSEC1_TXD[0:1]	Default: The eTSEC1 controller operates using the TBI protocol (or RTBI if configured in reduced mode).
eTSEC3 protocol	TSEC3_TXD[0:1]	Default: The eTSEC3 controller operates using the TBI protocol (or RTBI if configured in reduced mode).
PCI clock select	USB1_STP	Default: Synchronous mode. SYSCLK is used as the clock for the PCI interface.
PCI speed	USB2_STP	Default: PCI frequency above 33 MHz.
PCI I/O impedance	PCI1_GNT[1]	Default: 42 Ω I/O drivers are used on the PCI interface.
PCI arbiter	PCI1_GNT[2]	Default: The on-chip PCI arbiter is enabled.

Table 4. User Configuration Options (continued)

Configuration Type	Functional Pins	Comments
Memory debug	MSRCID[0]	Default: Debug information from the DDR SDRAM controller is driven on the MSRCID and MDVAL signals.
DDR debug configuration	MSRCID[1]	Default: Debug information is not driven on ECC pins. ECC pins function in their normal mode.
General purpose POR	LAD[0:31]	There is no default value for this general purpose POR.

3.3 Internal Test Modes

Several pins double as test mode enables. These test modes are for internal use only, and if enabled during reset may result in the MPC8536E not coming out of reset. Table 5 lists these pins and how they should be addressed during the reset sequence.

Table 5. Internal Test Mode Pins

Pin Group	Pins	Guideline for Reset
Debug	TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	Since these pins have an internal pullup enabled only at reset, they may be left floating if unconnected. Otherwise, they may need to be driven high (that is, by a PLD) if the device to which they are connected does not release to high impedance during reset.
	MSRCID[2]	
	MSRCID[3]	
	MSRCID[4	
	MDVAL	

Table 5. Internal Test Mode Pins (continued)

Pin Group	Pins	Guideline for Reset
Design for test	$\overline{\text{LSSD\_MODE}}$	These pins must be pulled to OV_{DD} via a 100 Ω–1 kΩ resistor.
	L1_TSTCLK	
	L2_TSTCLK	
	$\overline{\text{TEST\_SEL}}$	
eTSEC	EC_MDC	Since these pins have an internal pullup enabled only at reset, they may be left floating if unconnected. Otherwise, they may need to be driven high (that is, by a PLD) if the device to which they are connected does not release to high impedance during reset.
	TSEC1_TXD[3]	
	TSEC3_TXD[7]	
Power management	ASLEEP	
DUART	UART_SOUT[0:1]	
System control	$\overline{\text{HRESET\_REQ}}$	

3.4 Reset Checklist

Table 6 provides a summary MPC8536E POR and reset checklist for the designer.

Table 6. Checklist for POR and Reset Configurations

Item	Description	Completed
1	$\overline{\text{HRESET}}$ is asserted for a minimum of 100 μs.	
2	$\overline{\text{SRESET}}$ is asserted for a minimum of 3 SYSCLKs.	
3	MDVAL, UART_SOUT[0:1], EC_MDC,TSEC1_TXD[3], TSEC3_TXD[7], $\overline{\text{HRESET\_REQ}}$, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP—For proper state of these signals during reset, these pins can be left without any pulldowns, thus relying on the internal pullup to get the values to the require 2'b11.However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed.	
4	$\overline{\text{LSSD\_MODE}}$, L1_TSTCLK, L2_TSTCLK, $\overline{\text{TEST\_SEL}}$—These pins must be pulled to OV_{DD} via a 100 Ω–1 kΩ resistor.	
5	Configuration pins are either appropriately tied-off with a 4.7-kΩ resistor, or driven by an external device (meeting their required setup and hold times).	
6	PLL configurations are defined and meet the required setup and hold times.	
7	Valid SD_REF_CLK provided if SerDes1 is enabled. Valid SD2_REF_CLK provided if SerDes2 is enabled.	

4 Device Pins

This section discusses the recommended test points and provides a device pin map.

4.1 Recommended Test Points

For easier debug, it is highly recommended that the test points on the board include the following pins:

- CLK_OUT (This helps to verify the CCB clock.)
- TRIG_OUT/READY/$\overline{\text{QUIESCE}}$ (This helps to verify the end of the reset sequence.)
- ASLEEP (This helps to verify the end of the reset sequence.)
- SENSEVDD (This helps to verify power plane V_{DD}.)
- SENSEVSS (This helps to verify ground plane V_{SS}.)
- HRESET_REQ (This helps to verify proper boot sequencer functions and reset requests.)

4.2 Pin Map

Figure 4 provides a top view of the pin map of the device.

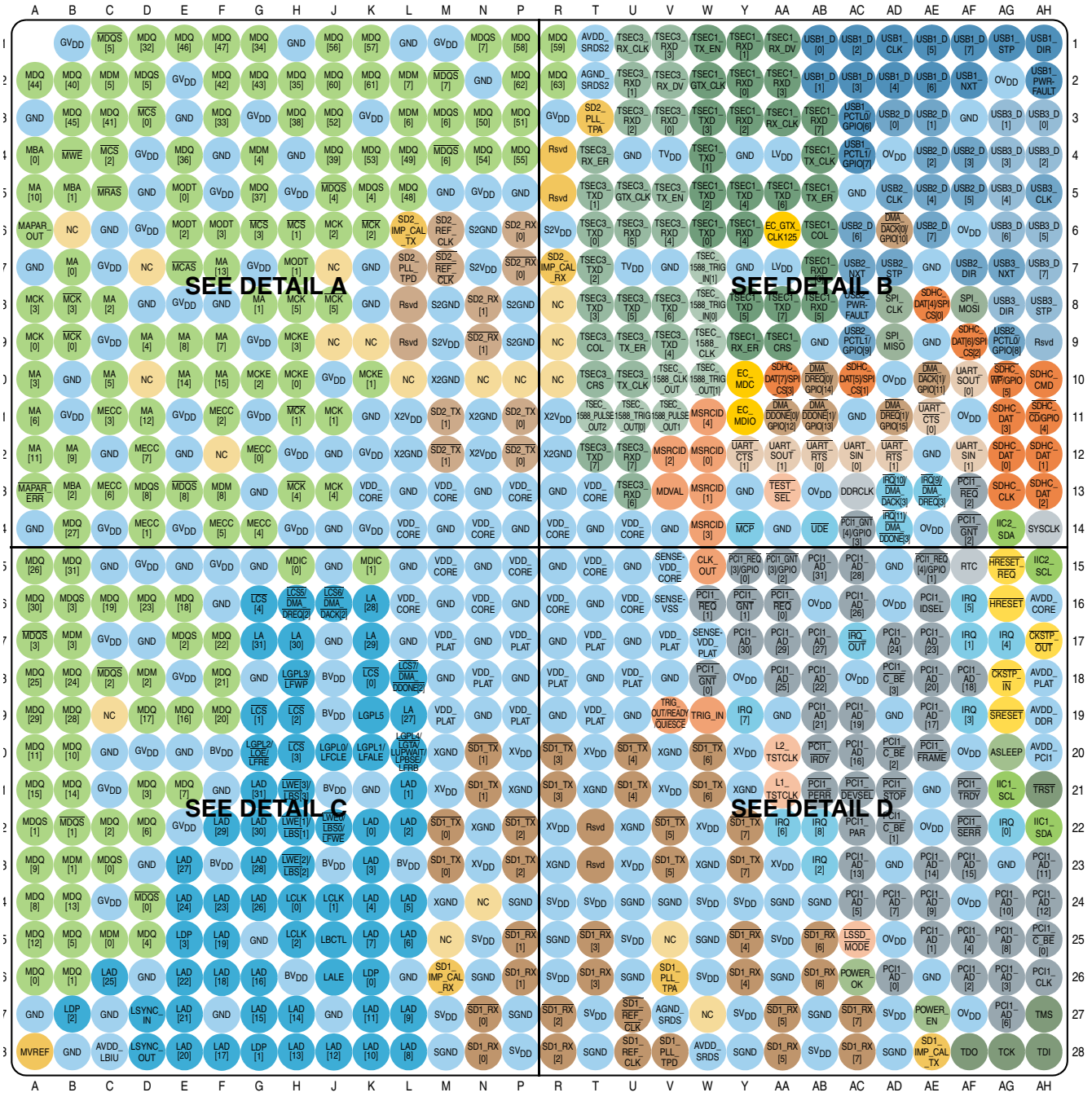
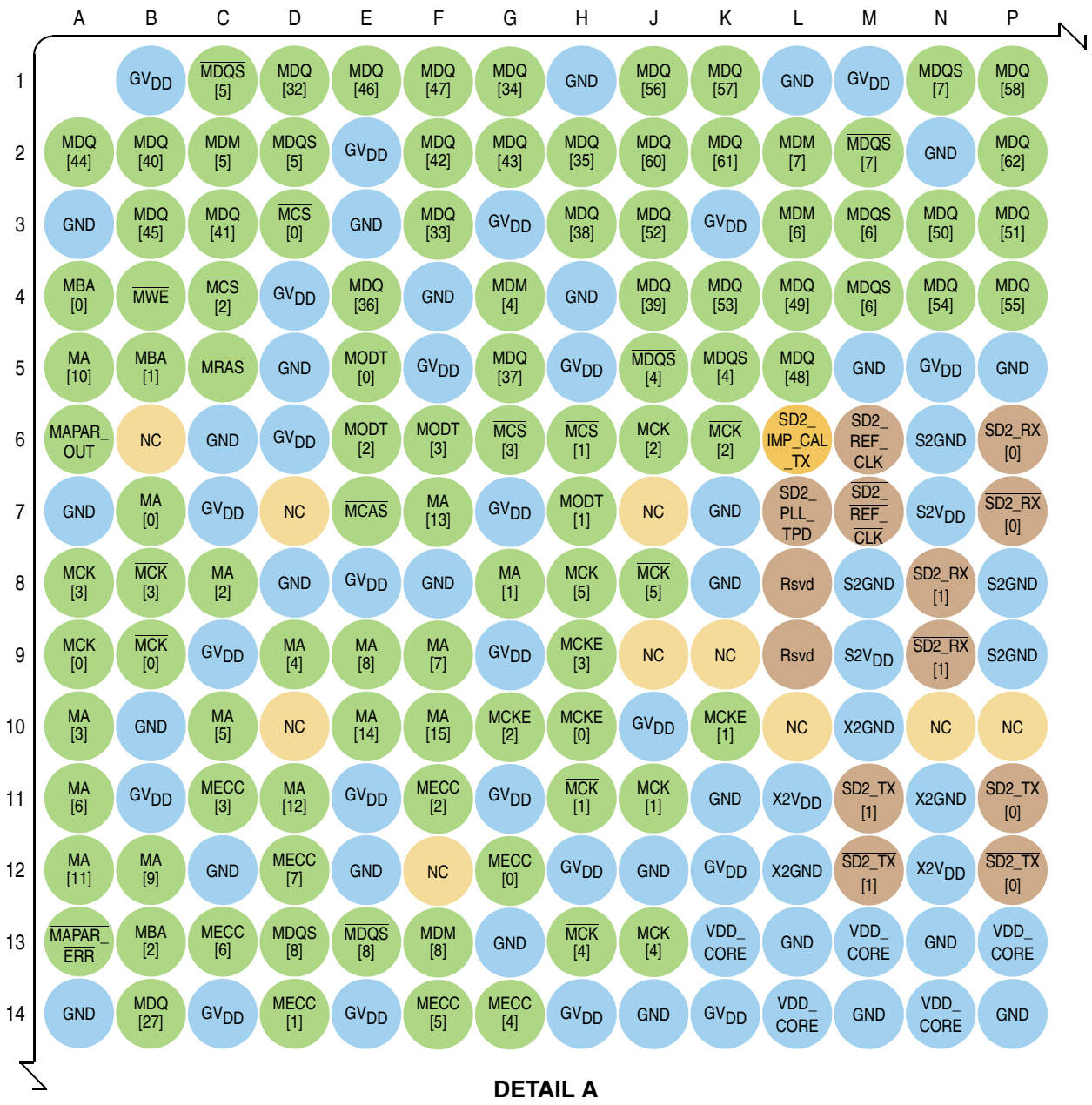
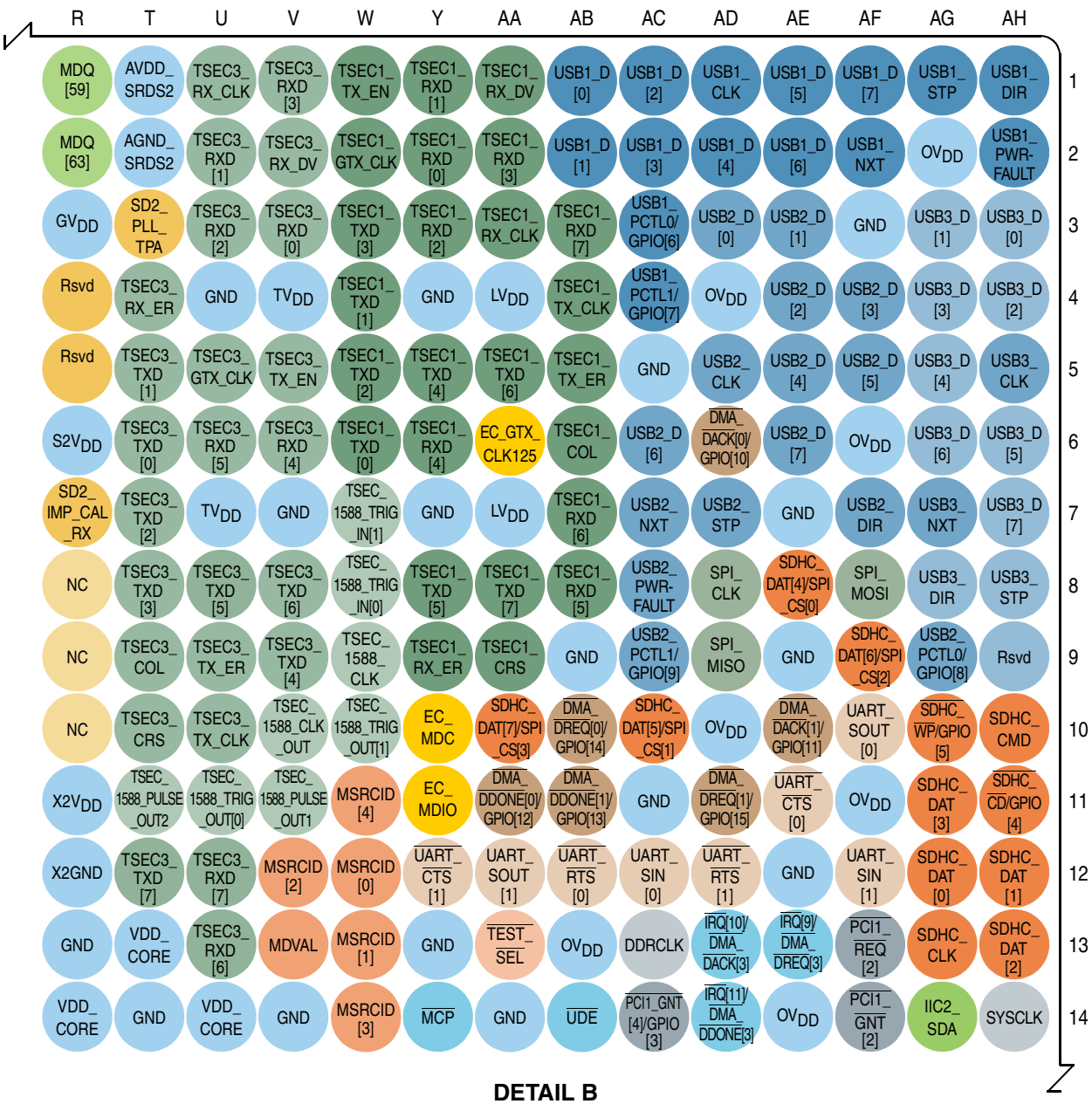


Figure 4. MPC8536E Pin Map Top View



DETAIL A

Figure 5. MPC8536E Pin Map Detail A



DETAIL B

Figure 6. MPC8536E Pin Map Detail B

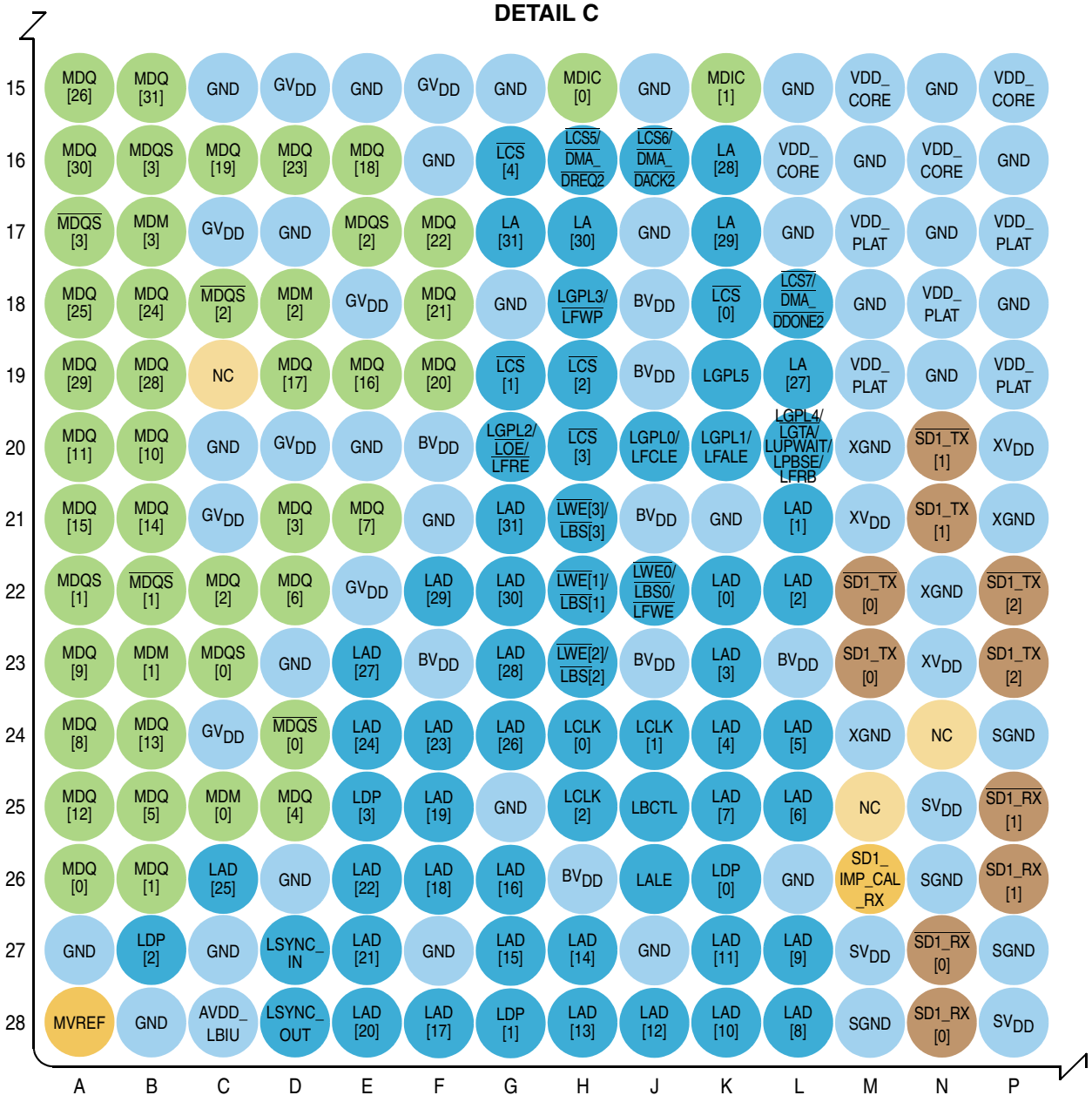


Figure 7. MPC8536E Pin Map Detail C

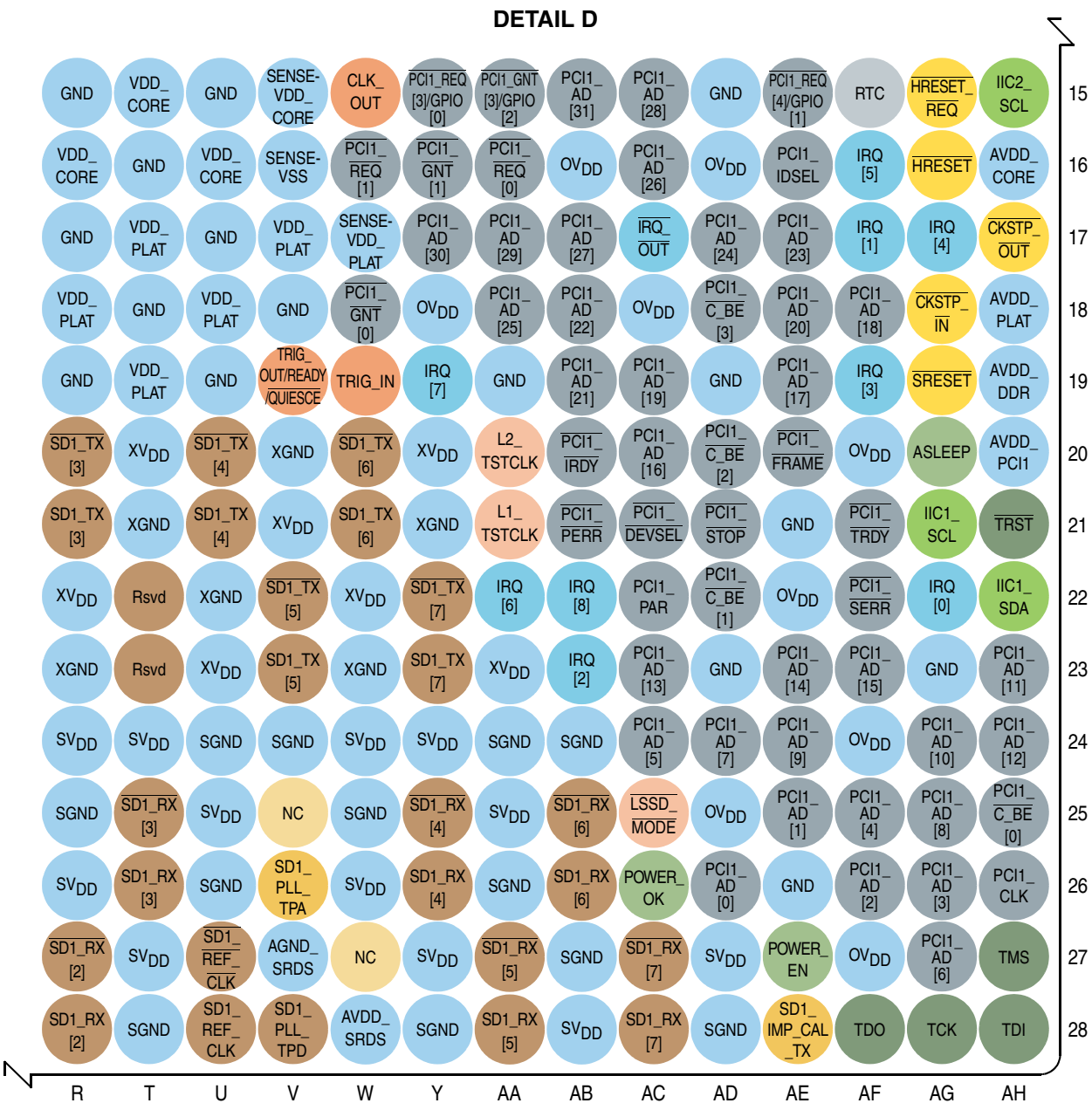


Figure 8. MPC8536E Pin Map Detail D

4.3 Pin Listings

A downloadable version of the pin list is available in the file AN3660SW.zip on freescale.com.

Table 7. Pin List—By Signal

Signal	Pin
AGND_SRDS	V27
AGND_SRDS2	T2

Table 7. Pin List—By Signal (continued)

Signal	Pin
ASLEEP	AG20
AVDD_CORE	AH16
AVDD_DDR	AH19
AVDD_LBIU	C28
AVDD_PCI1	AH20
AVDD_PLAT	AH18
AVDD_SRDS	W28
AVDD_SRDS2	T1
BVDD01	L23
BVDD02	J18
BVDD03	J23
BVDD04	J19
BVDD05	F20
BVDD06	F23
BVDD07	H26
BVDD08	J21
CKSTP_IN_B	AG18
CKSTP_OUT_B	AH17
CLK_OUT	W15
DDRCLK	AC13
EC_GTX_CLK125	AA6
EC_MDC	Y10
EC_MDIO	Y11
GND01	D5
GND02	AE7
GND03	F4
GND04	D26
GND05	D23
GND06	C12
GND07	C15
GND08	E20
GND09	D8
GND10	B10

Table 7. Pin List—By Signal (continued)

Signal	Pin
GND11	AF3
GND12	E3
GND13	J14
GND14	K21
GND15	F8
GND16	A3
GND17	F16
GND18	E12
GND19	E15
GND20	D17
GND21	L1
GND22	F21
GND23	H1
GND24	G13
GND25	G15
GND26	G18
GND27	C6
GND28	A14
GND29	A7
GND30	G25
GND31	H4
GND32	C20
GND33	J12
GND34	J15
GND35	J17
GND36	F27
GND37	M5
GND38	J27
GND39	K11
GND40	L26
GND41	K7
GND42	K8
GND43	T14

Table 7. Pin List—By Signal (continued)

Signal	Pin
GND44	V14
GND45	M16
GND46	M18
GND47	P14
GND48	N15
GND49	N17
GND50	N19
GND51	N2
GND52	P5
GND53	P16
GND54	P18
GND55	M14
GND56	R15
GND57	R17
GND58	R19
GND59	T16
GND60	T18
GND61	L17
GND62	U15
GND63	U17
GND64	U19
GND65	V18
GND66	C27
GND67	Y13
GND68	AE26
GND69	AA19
GND70	AE21
GND71	B28
GND72	AC11
GND73	AD19
GND74	AD23
GND75	L15
GND76	AD15

Table 7. Pin List—By Signal (continued)

Signal	Pin
GND77	AG23
GND78	AE9
GND79	A27
GND80	V7
GND81	Y7
GND82	AC5
GND83	U4
GND84	Y4
GND85	AE12
GND86	AB9
GND87	AA14
GND88	N13
GND89	R13
GND90	L13
GPIO00_PCI1_REQ3_B	Y15
GPIO01_PCI1_REQ4_B	AE15
GPIO02_PCI1_GNT3_B	AA15
GPIO03_PCI1_GNT4_B	AC14
GPIO06_USB1_PCTL0	AC3
GPIO07_USB1_PCTL1	AC4
GPIO08_USB2_PCTL0	AG9
GPIO09_USB2_PCTL1	AC9
GPIO10_DMA_DACK0_B	AD6
GPIO11_DMA_DACK1_B	AE10
GPIO12_DMA_DDONE0_B	AA11
GPIO13_DMA_DDONE1_B	AB11
GPIO14_DMA_DREQ0_B	AB10
GPIO15_DMA_DREQ1_B	AD11
GPIO4_SDHC_CD_B	AH11
GPIO5_SDHC_WP_B	AG10
GVDD01	B1
GVDD02	B11
GVDD03	C7

Table 7. Pin List—By Signal (continued)

Signal	Pin
GVDD04	C9
GVDD05	C14
GVDD06	C17
GVDD07	D4
GVDD08	D6
GVDD09	R3
GVDD10	D15
GVDD11	E2
GVDD12	E8
GVDD13	C24
GVDD14	E18
GVDD15	F5
GVDD16	E14
GVDD17	C21
GVDD18	G3
GVDD19	G7
GVDD20	G9
GVDD21	G11
GVDD22	H5
GVDD23	H12
GVDD24	E22
GVDD25	F15
GVDD26	J10
GVDD27	K3
GVDD28	K12
GVDD29	K14
GVDD30	H14
GVDD31	D20
GVDD32	E11
GVDD33	M1
GVDD34	N5
HRESET_B	AG16
HRESET_REQ_B	AG15

Table 7. Pin List—By Signal (continued)

Signal	Pin
IIC1_SCL	AG21
IIC1_SDA	AH22
IIC2_SCL	AH15
IIC2_SDA	AG14
IRQ_OUT_B	AC17
IRQ00	AG22
IRQ01	AF17
IRQ02	AB23
IRQ03	AF19
IRQ04	AG17
IRQ05	AF16
IRQ06	AA22
IRQ07	Y19
IRQ08	AB22
IRQ09_DMA_DREQ3_B	AE13
IRQ10_DMA_DACK3_B	AD13
IRQ11_DMA_DDONE3_B	AD14
L1_TSTCLK	AA21
L2_TSTCLK	AA20
LA27	L19
LA28	K16
LA29	K17
LA30	H17
LA31	G17
LAD00	K22
LAD01	L21
LAD02	L22
LAD03	K23
LAD04	K24
LAD05	L24
LAD06	L25
LAD07	K25
LAD08	L28

Table 7. Pin List—By Signal (continued)

Signal	Pin
LAD09	L27
LAD10	K28
LAD11	K27
LAD12	J28
LAD13	H28
LAD14	H27
LAD15	G27
LAD16	G26
LAD17	F28
LAD18	F26
LAD19	F25
LAD20	E28
LAD21	E27
LAD22	E26
LAD23	F24
LAD24	E24
LAD25	C26
LAD26	G24
LAD27	E23
LAD28	G23
LAD29	F22
LAD30	G22
LAD31	G21
LALE	J26
LBCTL	J25
LCLK0	H24
LCLK1	J24
LCLK2	H25
LCS0_B	K18
LCS1_B	G19
LCS2_B	H19
LCS3_B	H20
LCS4_B	G16

Table 7. Pin List—By Signal (continued)

Signal	Pin
LCS5_B_DMA_DREQ2_B	H16
LCS6_B_DMA_DACK2_B	J16
LCS7_B_DMA_DDONE2_B	L18
LDP0	K26
LDP1	G28
LDP2	B27
LDP3	E25
LGPL0_LFCLE	J20
LGPL1_LFALE	K20
LGPL2_LOE_B_LFRE_B	G20
LGPL3_LFWP_B	H18
LGPL4_LGTA_B_LUPWAIT_LPBSE_LFRB	L20
LGPL5	K19
LSSD_MODE_B	AC25
LSYNC_IN	D27
LSYNC_OUT	D28
LVDD1	AA7
LVDD2	AA4
LWE0_B_LBS0_B_LFWE_B	J22
LWE1_B_LBS1_B	H22
LWE2_B_LBS2_B	H23
LWE3_B_LBS3_B	H21
MA00	B7
MA01	G8
MA02	C8
MA03	A10
MA04	D9
MA05	C10
MA06	A11
MA07	F9
MA08	E9
MA09	B12
MA10	A5

Table 7. Pin List—By Signal (continued)

Signal	Pin
MA11	A12
MA12	D11
MA13	F7
MA14	E10
MA15	F10
MAPAR_ERR_B	A13
MAPAR_OUT	A6
MBA0	A4
MBA1	B5
MBA2	B13
MCAS_B	E7
MCK0	A9
MCK0_B	B9
MCK1	J11
MCK1_B	H11
MCK2	J6
MCK2_B	K6
MCK3	A8
MCK3_B	B8
MCK4	J13
MCK4_B	H13
MCK5	H8
MCK5_B	J8
MCKE0	H10
MCKE1	K10
MCKE2	G10
MCKE3	H9
MCP_B	Y14
MCS0_B	D3
MCS1_B	H6
MCS2_B	C4
MCS3_B	G6
MDIC0	H15

Table 7. Pin List—By Signal (continued)

Signal	Pin
MDIC1	K15
MDM0	C25
MDM1	B23
MDM2	D18
MDM3	B17
MDM4	G4
MDM5	C2
MDM6	L3
MDM7	L2
MDM8	F13
MDQ00	A26
MDQ01	B26
MDQ02	C22
MDQ03	D21
MDQ04	D25
MDQ05	B25
MDQ06	D22
MDQ07	E21
MDQ08	A24
MDQ09	A23
MDQ10	B20
MDQ11	A20
MDQ12	A25
MDQ13	B24
MDQ14	B21
MDQ15	A21
MDQ16	E19
MDQ17	D19
MDQ18	E16
MDQ19	C16
MDQ20	F19
MDQ21	F18
MDQ22	F17

Table 7. Pin List—By Signal (continued)

Signal	Pin
MDQ23	D16
MDQ24	B18
MDQ25	A18
MDQ26	A15
MDQ27	B14
MDQ28	B19
MDQ29	A19
MDQ30	A16
MDQ31	B15
MDQ32	D1
MDQ33	F3
MDQ34	G1
MDQ35	H2
MDQ36	E4
MDQ37	G5
MDQ38	H3
MDQ39	J4
MDQ40	B2
MDQ41	C3
MDQ42	F2
MDQ43	G2
MDQ44	A2
MDQ45	B3
MDQ46	E1
MDQ47	F1
MDQ48	L5
MDQ49	L4
MDQ50	N3
MDQ51	P3
MDQ52	J3
MDQ53	K4
MDQ54	N4
MDQ55	P4

Table 7. Pin List—By Signal (continued)

Signal	Pin
MDQ56	J1
MDQ57	K1
MDQ58	P1
MDQ59	R1
MDQ60	J2
MDQ61	K2
MDQ62	P2
MDQ63	R2
MDQS0	C23
MDQS0_B	D24
MDQS1	A22
MDQS1_B	B22
MDQS2	E17
MDQS2_B	C18
MDQS3	B16
MDQS3_B	A17
MDQS4	K5
MDQS4_B	J5
MDQS5	D2
MDQS5_B	C1
MDQS6	M3
MDQS6_B	M4
MDQS7	N1
MDQS7_B	M2
MDQS8	D13
MDQS8_B	E13
MDVAL	V13
MECC0	G12
MECC1	D14
MECC2	F11
MECC3	C11
MECC4	G14
MECC5	F14

Table 7. Pin List—By Signal (continued)

Signal	Pin
MECC6	C13
MECC7	D12
MODT0	E5
MODT1	H7
MODT2	E6
MODT3	F6
MRAS_B	C5
MSRCID0	W12
MSRCID1	W13
MSRCID2	V12
MSRCID3	W14
MSRCID4	W11
MVREF	A28
MWE_B	B4
NC01	C19
NC02	D7
NC03	D10
NC05	L10
NC06	R10
NC07	B6
NC08	F12
NC09	J7
NC10	P10
NC11	M25
NC12	W27
NC13	N24
NC14	N10
NC15	R8
NC16	J9
NC18	K9
NC19	V25
NC21	R9
OVDD01	Y18

Table 7. Pin List—By Signal (continued)

Signal	Pin
OVDD02	AG2
OVDD03	AD4
OVDD04	AB16
OVDD05	AF6
OVDD06	AC18
OVDD07	AB13
OVDD08	AD10
OVDD09	AE14
OVDD10	AD16
OVDD11	AD25
OVDD12	AF27
OVDD13	AE22
OVDD14	AF11
OVDD15	AF20
OVDD16	AF24
PCI1_AD00	AD26
PCI1_AD01	AE25
PCI1_AD02	AF26
PCI1_AD03	AG26
PCI1_AD04	AF25
PCI1_AD05	AC24
PCI1_AD06	AG27
PCI1_AD07	AD24
PCI1_AD08	AG25
PCI1_AD09	AE24
PCI1_AD10	AG24
PCI1_AD11	AH23
PCI1_AD12	AH24
PCI1_AD13	AC23
PCI1_AD14	AE23
PCI1_AD15	AF23
PCI1_AD16	AC20
PCI1_AD17	AE19

Table 7. Pin List—By Signal (continued)

Signal	Pin
PCI1_AD18	AF18
PCI1_AD19	AC19
PCI1_AD20	AE18
PCI1_AD21	AB19
PCI1_AD22	AB18
PCI1_AD23	AE17
PCI1_AD24	AD17
PCI1_AD25	AA18
PCI1_AD26	AC16
PCI1_AD27	AB17
PCI1_AD28	AC15
PCI1_AD29	AA17
PCI1_AD30	Y17
PCI1_AD31	AB15
PCI1_C_BE0_B	AH25
PCI1_C_BE1_B	AD22
PCI1_C_BE2_B	AD20
PCI1_C_BE3_B	AD18
PCI1_CLK	AH26
PCI1_DEVSEL_B	AC21
PCI1_FRAME_B	AE20
PCI1_GNT0_B	W18
PCI1_GNT1_B	Y16
PCI1_GNT2_B	AF14
PCI1_IDSEL	AE16
PCI1_IRDY_B	AB20
PCI1_PAR	AC22
PCI1_PERR_B	AB21
PCI1_REQ0_B	AA16
PCI1_REQ1_B	W16
PCI1_REQ2_B	AF13
PCI1_SERR_B	AF22
PCI1_STOP_B	AD21

Table 7. Pin List—By Signal (continued)

Signal	Pin
PCI1_TRDY_B	AF21
POWER_EN	AE27
POWER_OK	AC26
RTC	AF15
S2GND01	P8
S2GND02	P9
S2GND03	N6
S2GND04	M8
S2VDD01	R6
S2VDD02	N7
S2VDD03	M9
SD1_IMP_CAL_RX	M26
SD1_IMP_CAL_TX	AE28
SD1_PLL_TPA	V26
SD1_PLL_TPD	V28
SD1_REF_CLK	U28
SD1_REF_CLK_B	U27
SD1_RX0	N28
SD1_RX0_B	N27
SD1_RX1	P26
SD1_RX1_B	P25
SD1_RX2	R28
SD1_RX2_B	R27
SD1_RX3	T26
SD1_RX3_B	T25
SD1_RX4	Y26
SD1_RX4_B	Y25
SD1_RX5	AA28
SD1_RX5_B	AA27
SD1_RX6	AB26
SD1_RX6_B	AB25
SD1_RX7	AC28
SD1_RX7_B	AC27

Table 7. Pin List—By Signal (continued)

Signal	Pin
SD1_TST_CLK	T22
SD1_TST_CLK_B	T23
SD1_TX0	M23
SD1_TX0_B	M22
SD1_TX1	N21
SD1_TX1_B	N20
SD1_TX2	P23
SD1_TX2_B	P22
SD1_TX3	R21
SD1_TX3_B	R20
SD1_TX4	U21
SD1_TX4_B	U20
SD1_TX5	V23
SD1_TX5_B	V22
SD1_TX6	W21
SD1_TX6_B	W20
SD1_TX7	Y23
SD1_TX7_B	Y22
SD2_IMP_CAL_RX	R7
SD2_IMP_CAL_TX	L6
SD2_PLL_TPA	T3
SD2_PLL_TPD	L7
SD2_REF_CLK	M6
SD2_REF_CLK_B	M7
SD2_RX0	P6
SD2_RX0_B	P7
SD2_RX1	N8
SD2_RX1_B	N9
SD2_TST_CLK	L8
SD2_TST_CLK_B	L9
SD2_TX0	P11
SD2_TX0_B	P12
SD2_TX1	M11

Table 7. Pin List—By Signal (continued)

Signal	Pin
SD2_TX1_B	M12
SDHC_CLK	AG13
SDHC_CMD	AH10
SDHC_DAT0	AG12
SDHC_DAT1	AH12
SDHC_DAT2	AH13
SDHC_DAT3	AG11
SENSEVDD_CORE	V15
SENSEVDD_PLAT	W17
SENSEVSS	V16
SGND01	M28
SGND02	N26
SGND03	P24
SGND04	P27
SGND05	R25
SGND06	T28
SGND07	U24
SGND08	U26
SGND09	V24
SGND10	W25
SGND11	Y28
SGND12	AA24
SGND13	AA26
SGND14	AB24
SGND15	AB27
SGND16	AD28
SPI_CLK	AD8
SPI_CS0_SDHC_DAT4	AE8
SPI_CS1_SDHC_DAT5	AC10
SPI_CS2_SDHC_DAT6	AF9
SPI_CS3_SDHC_DAT7	AA10
SPI_MISO	AD9
SPI_MOSI	AF8

Table 7. Pin List—By Signal (continued)

Signal	Pin
SRESET_B	AG19
SVDD01	M27
SVDD02	N25
SVDD03	P28
SVDD04	R24
SVDD05	R26
SVDD06	T24
SVDD07	T27
SVDD08	U25
SVDD09	W24
SVDD10	W26
SVDD11	Y24
SVDD12	Y27
SVDD13	AA25
SVDD14	AB28
SVDD15	AD27
SYSCLK	AH14
TCK	AG28
TDI	AH28
TDO	AF28
Reserved	R4
Reserved	R5
TEST_SEL_B	AA13
TMS	AH27
TRIG_IN	W19
TRIG_OUT_READY_QUIESCE_B	V19
TRST_B	AH21
TSEC_1588_CLK	W9
TSEC_1588_CLK_OUT	V10
TSEC_1588_PULSE_OUT1	V11
TSEC_1588_PULSE_OUT2	T11
TSEC_1588_TRIG_IN0	W8
TSEC_1588_TRIG_IN1	W7

Table 7. Pin List—By Signal (continued)

Signal	Pin
TSEC_1588_TRIG_OUT0	U11
TSEC_1588_TRIG_OUT1	W10
TSEC1_COL	AB6
TSEC1_CRS	AA9
TSEC1_GTX_CLK	W2
TSEC1_RX_CLK	AA3
TSEC1_RX_DV	AA1
TSEC1_RX_ER	Y9
TSEC1_RXD0	Y2
TSEC1_RXD1	Y1
TSEC1_RXD2	Y3
TSEC1_RXD3	AA2
TSEC1_RXD4	Y6
TSEC1_RXD5	AB8
TSEC1_RXD6	AB7
TSEC1_RXD7	AB3
TSEC1_TX_CLK	AB4
TSEC1_TX_EN	W1
TSEC1_TX_ER	AB5
TSEC1_TXD0	W6
TSEC1_TXD1	W4
TSEC1_TXD2	W5
TSEC1_TXD3	W3
TSEC1_TXD4	Y5
TSEC1_TXD5	Y8
TSEC1_TXD6	AA5
TSEC1_TXD7	AA8
TSEC3_COL	T9
TSEC3_CRS	T10
TSEC3_GTX_CLK	U5
TSEC3_RX_CLK	U1
TSEC3_RX_DV	V2
TSEC3_RX_ER	T4

Table 7. Pin List—By Signal (continued)

Signal	Pin
TSEC3_RXD0	V3
TSEC3_RXD1	U2
TSEC3_RXD2	U3
TSEC3_RXD3	V1
TSEC3_RXD4	V6
TSEC3_RXD5	U6
TSEC3_RXD6	U13
TSEC3_RXD7	U12
TSEC3_TX_CLK	U10
TSEC3_TX_EN	V5
TSEC3_TX_ER	U9
TSEC3_TXD0	T6
TSEC3_TXD1	T5
TSEC3_TXD2	T7
TSEC3_TXD3	T8
TSEC3_TXD4	V9
TSEC3_TXD5	U8
TSEC3_TXD6	V8
TSEC3_TXD7	T12
TVDD1	V4
TVDD2	U7
UART_CTS0_B	AE11
UART_CTS1_B	Y12
UART_RTS0_B	AB12
UART_RTS1_B	AD12
UART_SIN0	AC12
UART_SIN1	AF12
UART_SOUT0	AF10
UART_SOUT1	AA12
UDE_B	AB14
USB1_CLK	AD1
USB1_D0	AB1
USB1_D1	AB2

Table 7. Pin List—By Signal (continued)

Signal	Pin
USB1_D2	AC1
USB1_D3	AC2
USB1_D4	AD2
USB1_D5	AE1
USB1_D6	AE2
USB1_D7	AF1
USB1_DIR	AH1
USB1_NXT	AF2
USB1_PWRFAULT	AH2
USB1_STP	AG1
USB2_CLK	AD5
USB2_D0	AD3
USB2_D1	AE3
USB2_D2	AE4
USB2_D3	AF4
USB2_D4	AE5
USB2_D5	AF5
USB2_D6	AC6
USB2_D7	AE6
USB2_DIR	AF7
USB2_NXT	AC7
USB2_PWRFAULT	AC8
USB2_STP	AD7
USB3_CLK	AH5
USB3_D0	AH3
USB3_D1	AG3
USB3_D2	AH4
USB3_D3	AG4
USB3_D4	AG5
USB3_D5	AH6
USB3_D6	AG6
USB3_D7	AH7
USB3_DIR	AG8

Table 7. Pin List—By Signal (continued)

Signal	Pin
USB3_NXT	AG7
USB3_PWRFAULT	AH9
USB3_STP	AH8
VDD_CORE01	P13
VDD_CORE02	U16
VDD_CORE03	L16
VDD_CORE04	M15
VDD_CORE05	N14
VDD_CORE06	R14
VDD_CORE07	P15
VDD_CORE08	N16
VDD_CORE09	M13
VDD_CORE10	U14
VDD_CORE11	T13
VDD_CORE12	L14
VDD_CORE13	T15
VDD_CORE14	R16
VDD_CORE15	K13
VDD_PLAT1	T19
VDD_PLAT10	M17
VDD_PLAT2	T17
VDD_PLAT3	V17
VDD_PLAT4	U18
VDD_PLAT5	R18
VDD_PLAT6	N18
VDD_PLAT7	M19
VDD_PLAT8	P19
VDD_PLAT9	P17
X2GND01	R12
X2GND02	M10
X2GND03	N11
X2GND04	L12
X2VDD01	R11

Table 7. Pin List—By Signal (continued)

Signal	Pin
X2VDD02	N12
X2VDD03	L11
XGND01	M20
XGND02	M24
XGND03	N22
XGND04	P21
XGND05	R23
XGND06	T21
XGND07	U22
XGND08	V20
XGND09	W23
XGND10	Y21
XVDD01	M21
XVDD02	N23
XVDD03	P20
XVDD04	R22
XVDD05	T20
XVDD06	U23
XVDD07	V21
XVDD08	W22
XVDD09	Y20
XVDD10	AA23

Table 8. Pin List—By Pin Number

Signal	Pin
MDQ44	A2
GND16	A3
MBA0	A4
MA10	A5
MAPAR_OUT	A6
GND29	A7
MCK3	A8
MCK0	A9
MA03	A10
MA06	A11
MA11	A12
MAPAR_ERR_B	A13
GND28	A14
MDQ26	A15
MDQ30	A16
MDQS3_B	A17
MDQ25	A18
MDQ29	A19
MDQ11	A20
MDQ15	A21
MDQS1	A22
MDQ09	A23
MDQ08	A24
MDQ12	A25
MDQ00	A26
GND79	A27
MVREF	A28
GVDD01	B1
MDQ40	B2
MDQ45	B3
MWE_B	B4
MBA1	B5
NC07	B6

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
MA00	B7
MCK3_B	B8
MCK0_B	B9
GND10	B10
GVDD02	B11
MA09	B12
MBA2	B13
MDQ27	B14
MDQ31	B15
MDQS3	B16
MDM3	B17
MDQ24	B18
MDQ28	B19
MDQ10	B20
MDQ14	B21
MDQS1_B	B22
MDM1	B23
MDQ13	B24
MDQ05	B25
MDQ01	B26
LDP2	B27
GND71	B28
MDQS5_B	C1
MDM5	C2
MDQ41	C3
MCS2_B	C4
MRAS_B	C5
GND27	C6
GVDD03	C7
MA02	C8
GVDD04	C9
MA05	C10
MECC3	C11

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
GND06	C12
MECC6	C13
GVDD05	C14
GND07	C15
MDQ19	C16
GVDD06	C17
MDQS2_B	C18
NC01	C19
GND32	C20
GVDD17	C21
MDQ02	C22
MDQS0	C23
GVDD13	C24
MDM0	C25
LAD25	C26
GND66	C27
AVDD_LBIU	C28
MDQ32	D1
MDQS5	D2
MCS0_B	D3
GVDD07	D4
GND01	D5
GVDD08	D6
NC02	D7
GND09	D8
MA04	D9
NC03	D10
MA12	D11
MECC7	D12
MDQS8	D13
MECC1	D14
GVDD10	D15
MDQ23	D16

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
GND20	D17
MDM2	D18
MDQ17	D19
GVDD31	D20
MDQ03	D21
MDQ06	D22
GND05	D23
MDQS0_B	D24
MDQ04	D25
GND04	D26
LSYNC_IN	D27
LSYNC_OUT	D28
MDQ46	E1
GVDD11	E2
GND12	E3
MDQ36	E4
MODT0	E5
MODT2	E6
MCAS_B	E7
GVDD12	E8
MA08	E9
MA14	E10
GVDD32	E11
GND18	E12
MDQS8_B	E13
GVDD16	E14
GND19	E15
MDQ18	E16
MDQS2	E17
GVDD14	E18
MDQ16	E19
GND08	E20
MDQ07	E21

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
GVDD24	E22
LAD27	E23
LAD24	E24
LDP3	E25
LAD22	E26
LAD21	E27
LAD20	E28
MDQ47	F1
MDQ42	F2
MDQ33	F3
GND03	F4
GVDD15	F5
MODT3	F6
MA13	F7
GND15	F8
MA07	F9
MA15	F10
MECC2	F11
NC08	F12
MDM8	F13
MECC5	F14
GVDD25	F15
GND17	F16
MDQ22	F17
MDQ21	F18
MDQ20	F19
BVDD05	F20
GND22	F21
LAD29	F22
BVDD06	F23
LAD23	F24
LAD19	F25
LAD18	F26

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
GND36	F27
LAD17	F28
MDQ34	G1
MDQ43	G2
GVDD18	G3
MDM4	G4
MDQ37	G5
MCS3_B	G6
GVDD19	G7
MA01	G8
GVDD20	G9
MCKE2	G10
GVDD21	G11
MECC0	G12
GND24	G13
MECC4	G14
GND25	G15
LCS4_B	G16
LA31	G17
GND26	G18
LCS1_B	G19
LGPL2_LOE_B_LFRE_B	G20
LAD31	G21
LAD30	G22
LAD28	G23
LAD26	G24
GND30	G25
LAD16	G26
LAD15	G27
LDP1	G28
GND23	H1
MDQ35	H2
MDQ38	H3

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
GND31	H4
GVDD22	H5
MCS1_B	H6
MODT1	H7
MCK5	H8
MCKE3	H9
MCKE0	H10
MCK1_B	H11
GVDD23	H12
MCK4_B	H13
GVDD30	H14
MDIC0	H15
LCS5_B_DMA_DREQ2_B	H16
LA30	H17
LGPL3_LFWP_B	H18
LCS2_B	H19
LCS3_B	H20
LWE3_B_LBS3_B	H21
LWE1_B_LBS1_B	H22
LWE2_B_LBS2_B	H23
LCLK0	H24
LCLK2	H25
BVDD07	H26
LAD14	H27
LAD13	H28
MDQ56	J1
MDQ60	J2
MDQ52	J3
MDQ39	J4
MDQS4_B	J5
MCK2	J6
NC09	J7
MCK5_B	J8

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
NC16	J9
GVDD26	J10
MCK1	J11
GND33	J12
MCK4	J13
GND13	J14
GND34	J15
LCS6_B_DMA_DACK2_B	J16
GND35	J17
BVDD02	J18
BVDD04	J19
LGPL0_LFCLE	J20
BVDD08	J21
LWE0_B_LBS0_B_LFWE_B	J22
BVDD03	J23
LCLK1	J24
LBCTL	J25
LALE	J26
GND38	J27
LAD12	J28
MDQ57	K1
MDQ61	K2
GVDD27	K3
MDQ53	K4
MDQS4	K5
MCK2_B	K6
GND41	K7
GND42	K8
NC18	K9
MCKE1	K10
GND39	K11
GVDD28	K12
VDD_CORE15	K13

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
GVDD29	K14
MDIC1	K15
LA28	K16
LA29	K17
LCS0_B	K18
LGPL5	K19
LGPL1_LFALE	K20
GND14	K21
LAD00	K22
LAD03	K23
LAD04	K24
LAD07	K25
LDP0	K26
LAD11	K27
LAD10	K28
GND21	L1
MDM7	L2
MDM6	L3
MDQ49	L4
MDQ48	L5
SD2_IMP_CAL_TX	L6
SD2_PLL_TPD	L7
SD2_TST_CLK	L8
SD2_TST_CLK_B	L9
NC05	L10
X2VDD03	L11
X2GND04	L12
GND90	L13
VDD_CORE12	L14
GND75	L15
VDD_CORE03	L16
GND61	L17
LCS7_B_DMA_DDONE2_B	L18

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
LA27	L19
LGPL4_LGTA_B_LUPWAIT_LPBSE_LFRB	L20
LAD01	L21
LAD02	L22
BVDD01	L23
LAD05	L24
LAD06	L25
GND40	L26
LAD09	L27
LAD08	L28
GVDD33	M1
MDQS7_B	M2
MDQS6	M3
MDQS6_B	M4
GND37	M5
SD2_REF_CLK	M6
SD2_REF_CLK_B	M7
S2GND04	M8
S2VDD03	M9
X2GND02	M10
SD2_TX1	M11
SD2_TX1_B	M12
VDD_CORE09	M13
GND55	M14
VDD_CORE04	M15
GND45	M16
VDD_PLAT10	M17
GND46	M18
VDD_PLAT7	M19
XGND01	M20
XVDD01	M21
SD1_TX0_B	M22
SD1_TX0	M23

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
XGND02	M24
NC11	M25
SD1_IMP_CAL_RX	M26
SVDD01	M27
SGND01	M28
MDQS7	N1
GND51	N2
MDQ50	N3
MDQ54	N4
GVDD34	N5
S2GND03	N6
S2VDD02	N7
SD2_RX1	N8
SD2_RX1_B	N9
NC14	N10
X2GND03	N11
X2VDD02	N12
GND88	N13
VDD_CORE05	N14
GND48	N15
VDD_CORE08	N16
GND49	N17
VDD_PLAT6	N18
GND50	N19
SD1_TX1_B	N20
SD1_TX1	N21
XGND03	N22
XVDD02	N23
NC13	N24
SVDD02	N25
SGND02	N26
SD1_RX0_B	N27
SD1_RX0	N28

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
MDQ58	P1
MDQ62	P2
MDQ51	P3
MDQ55	P4
GND52	P5
SD2_RX0	P6
SD2_RX0_B	P7
S2GND01	P8
S2GND02	P9
NC10	P10
SD2_TX0	P11
SD2_TX0_B	P12
VDD_CORE01	P13
GND47	P14
VDD_CORE07	P15
GND53	P16
VDD_PLAT9	P17
GND54	P18
VDD_PLAT8	P19
XVDD03	P20
XGND04	P21
SD1_TX2_B	P22
SD1_TX2	P23
SGND03	P24
SD1_RX1_B	P25
SD1_RX1	P26
SGND04	P27
SVDD03	P28
MDQ59	R1
MDQ63	R2
GVDD09	R3
Reserved	R4
Reserved	R5

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
S2VDD01	R6
SD2_IMP_CAL_RX	R7
NC15	R8
NC21	R9
NC06	R10
X2VDD01	R11
X2GND01	R12
GND89	R13
VDD_CORE06	R14
GND56	R15
VDD_CORE14	R16
GND57	R17
VDD_PLAT5	R18
GND58	R19
SD1_TX3_B	R20
SD1_TX3	R21
XVDD04	R22
XGND05	R23
SVDD04	R24
SGND05	R25
SVDD05	R26
SD1_RX2_B	R27
SD1_RX2	R28
AVDD_SRDS2	T1
AGND_SRDS2	T2
SD2_PLL_TPA	T3
TSEC3_RX_ER	T4
TSEC3_TXD1	T5
TSEC3_TXD0	T6
TSEC3_TXD2	T7
TSEC3_TXD3	T8
TSEC3_COL	T9
TSEC3_CRS	T10

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
TSEC_1588_PULSE_OUT2	T11
TSEC3_TXD7	T12
VDD_CORE11	T13
GND43	T14
VDD_CORE13	T15
GND59	T16
VDD_PLAT2	T17
GND60	T18
VDD_PLAT1	T19
XVDD05	T20
XGND06	T21
SD1_TST_CLK	T22
SD1_TST_CLK_B	T23
SVDD06	T24
SD1_RX3_B	T25
SD1_RX3	T26
SVDD07	T27
SGND06	T28
TSEC3_RX_CLK	U1
TSEC3_RXD1	U2
TSEC3_RXD2	U3
GND83	U4
TSEC3_GTX_CLK	U5
TSEC3_RXD5	U6
TVDD2	U7
TSEC3_TXD5	U8
TSEC3_TX_ER	U9
TSEC3_TX_CLK	U10
TSEC_1588_TRIG_OUT0	U11
TSEC3_RXD7	U12
TSEC3_RXD6	U13
VDD_CORE10	U14
GND62	U15

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
VDD_CORE02	U16
GND63	U17
VDD_PLAT4	U18
GND64	U19
SD1_TX4_B	U20
SD1_TX4	U21
XGND07	U22
XVDD06	U23
SGND07	U24
SVDD08	U25
SGND08	U26
SD1_REF_CLK_B	U27
SD1_REF_CLK	U28
TSEC3_RXD3	V1
TSEC3_RX_DV	V2
TSEC3_RXD0	V3
TVDD1	V4
TSEC3_TX_EN	V5
TSEC3_RXD4	V6
GND80	V7
TSEC3_TXD6	V8
TSEC3_TXD4	V9
TSEC_1588_CLK_OUT	V10
TSEC_1588_PULSE_OUT1	V11
MSRCID2	V12
MDVAL	V13
GND44	V14
SENSEVDD_CORE	V15
SENSEVSS	V16
VDD_PLAT3	V17
GND65	V18
TRIG_OUT_READY_QUIESCE_B	V19
XGND08	V20

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
XVDD07	V21
SD1_TX5_B	V22
SD1_TX5	V23
SGND09	V24
NC19	V25
SD1_PLL_TPA	V26
AGND_SRDS	V27
SD1_PLL_TPD	V28
TSEC1_TX_EN	W1
TSEC1_GTX_CLK	W2
TSEC1_TXD3	W3
TSEC1_TXD1	W4
TSEC1_TXD2	W5
TSEC1_TXD0	W6
TSEC_1588_TRIG_IN1	W7
TSEC_1588_TRIG_IN0	W8
TSEC_1588_CLK	W9
TSEC_1588_TRIG_OUT1	W10
MSRCID4	W11
MSRCID0	W12
MSRCID1	W13
MSRCID3	W14
CLK_OUT	W15
PCI1_REQ1_B	W16
SENSEVDD_PLAT	W17
PCI1_GNT0_B	W18
TRIG_IN	W19
SD1_TX6_B	W20
SD1_TX6	W21
XVDD08	W22
XGND09	W23
SVDD09	W24
SGND10	W25

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
SVDD10	W26
NC12	W27
AVDD_SRDS	W28
TSEC1_RXD1	Y1
TSEC1_RXD0	Y2
TSEC1_RXD2	Y3
GND84	Y4
TSEC1_TXD4	Y5
TSEC1_RXD4	Y6
GND81	Y7
TSEC1_TXD5	Y8
TSEC1_RX_ER	Y9
EC_MDC	Y10
EC_MDIO	Y11
UART_CTS1_B	Y12
GND67	Y13
MCP_B	Y14
GPIO00_PCI1_REQ3_B	Y15
PCI1_GNT1_B	Y16
PCI1_AD30	Y17
OVDD01	Y18
IRQ07	Y19
XVDD09	Y20
XGND10	Y21
SD1_TX7_B	Y22
SD1_TX7	Y23
SVDD11	Y24
SD1_RX4_B	Y25
SD1_RX4	Y26
SVDD12	Y27
SGND11	Y28
TSEC1_RX_DV	AA1
TSEC1_RXD3	AA2

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
TSEC1_RX_CLK	AA3
LVDD2	AA4
TSEC1_TXD6	AA5
EC_GTX_CLK125	AA6
LVDD1	AA7
TSEC1_TXD7	AA8
TSEC1_CRS	AA9
SPI_CS3_SDHC_DAT7	AA10
GPIO12_DMA_DDONE0_B	AA11
UART_SOUT1	AA12
TEST_SEL_B	AA13
GND87	AA14
GPIO02_PCI1_GNT3_B	AA15
PCI1_REQ0_B	AA16
PCI1_AD29	AA17
PCI1_AD25	AA18
GND69	AA19
L2_TSTCLK	AA20
L1_TSTCLK	AA21
IRQ06	AA22
XVDD10	AA23
SGND12	AA24
SVDD13	AA25
SGND13	AA26
SD1_RX5_B	AA27
SD1_RX5	AA28
USB1_D0	AB1
USB1_D1	AB2
TSEC1_RXD7	AB3
TSEC1_TX_CLK	AB4
TSEC1_TX_ER	AB5
TSEC1_COL	AB6
TSEC1_RXD6	AB7

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
TSEC1_RXD5	AB8
GND86	AB9
GPIO14_DMA_DREQ0_B	AB10
GPIO13_DMA_DDONE1_B	AB11
UART_RTS0_B	AB12
OVDD07	AB13
UDE_B	AB14
PCI1_AD31	AB15
OVDD04	AB16
PCI1_AD27	AB17
PCI1_AD22	AB18
PCI1_AD21	AB19
PCI1_IRDY_B	AB20
PCI1_PERR_B	AB21
IRQ08	AB22
IRQ02	AB23
SGND14	AB24
SD1_RX6_B	AB25
SD1_RX6	AB26
SGND15	AB27
SVDD14	AB28
USB1_D2	AC1
USB1_D3	AC2
GPIO06_USB1_PCTL0	AC3
GPIO07_USB1_PCTL1	AC4
GND82	AC5
USB2_D6	AC6
USB2_NXT	AC7
USB2_PWRFAULT	AC8
GPIO09_USB2_PCTL1	AC9
SPI_CS1_SDHC_DAT5	AC10
GND72	AC11
UART_SIN0	AC12

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
DDRCLK	AC13
GPIO03_PCI1_GNT4_B	AC14
PCI1_AD28	AC15
PCI1_AD26	AC16
IRQ_OUT_B	AC17
OVDD06	AC18
PCI1_AD19	AC19
PCI1_AD16	AC20
PCI1_DEVSEL_B	AC21
PCI1_PAR	AC22
PCI1_AD13	AC23
PCI1_AD05	AC24
LSSD_MODE_B	AC25
POWER_OK	AC26
SD1_RX7_B	AC27
SD1_RX7	AC28
USB1_CLK	AD1
USB1_D4	AD2
USB2_D0	AD3
OVDD03	AD4
USB2_CLK	AD5
GPIO10_DMA_DACK0_B	AD6
USB2_STP	AD7
SPI_CLK	AD8
SPI_MISO	AD9
OVDD08	AD10
GPIO15_DMA_DREQ1_B	AD11
UART_RTS1_B	AD12
IRQ10_DMA_DACK3_B	AD13
IRQ11_DMA_DDONE3_B	AD14
GND76	AD15
OVDD10	AD16
PCI1_AD24	AD17

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
PCI1_C_BE3_B	AD18
GND73	AD19
PCI1_C_BE2_B	AD20
PCI1_STOP_B	AD21
PCI1_C_BE1_B	AD22
GND74	AD23
PCI1_AD07	AD24
OVDD11	AD25
PCI1_AD00	AD26
SVDD15	AD27
SGND16	AD28
USB1_D5	AE1
USB1_D6	AE2
USB2_D1	AE3
USB2_D2	AE4
USB2_D4	AE5
USB2_D7	AE6
GND02	AE7
SPI_CS0_SDHC_DAT4	AE8
GND78	AE9
GPIO11_DMA_DACK1_B	AE10
UART_CTS0_B	AE11
GND85	AE12
IRQ09_DMA_DREQ3_B	AE13
OVDD09	AE14
GPIO01_PCI1_REQ4_B	AE15
PCI1_IDSEL	AE16
PCI1_AD23	AE17
PCI1_AD20	AE18
PCI1_AD17	AE19
PCI1_FRAME_B	AE20
GND70	AE21
OVDD13	AE22

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
PCI1_AD14	AE23
PCI1_AD09	AE24
PCI1_AD01	AE25
GND68	AE26
POWER_EN	AE27
SD1_IMP_CAL_TX	AE28
USB1_D7	AF1
USB1_NXT	AF2
GND11	AF3
USB2_D3	AF4
USB2_D5	AF5
OVDD05	AF6
USB2_DIR	AF7
SPI_MOSI	AF8
SPI_CS2_SDHC_DAT6	AF9
UART_SOUT0	AF10
OVDD14	AF11
UART_SIN1	AF12
PCI1_REQ2_B	AF13
PCI1_GNT2_B	AF14
RTC	AF15
IRQ05	AF16
IRQ01	AF17
PCI1_AD18	AF18
IRQ03	AF19
OVDD15	AF20
PCI1_TRDY_B	AF21
PCI1_SERR_B	AF22
PCI1_AD15	AF23
OVDD16	AF24
PCI1_AD04	AF25
PCI1_AD02	AF26
OVDD12	AF27

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
TDO	AF28
USB1_STP	AG1
OVDD02	AG2
USB3_D1	AG3
USB3_D3	AG4
USB3_D4	AG5
USB3_D6	AG6
USB3_NXT	AG7
USB3_DIR	AG8
GPIO08_USB2_PCTL0	AG9
GPIO5_SDHC_WP_B	AG10
SDHC_DAT3	AG11
SDHC_DAT0	AG12
SDHC_CLK	AG13
IIC2_SDA	AG14
HRESET_REQ_B	AG15
HRESET_B	AG16
IRQ04	AG17
CKSTP_IN_B	AG18
SRESET_B	AG19
ASLEEP	AG20
IIC1_SCL	AG21
IRQ00	AG22
GND77	AG23
PCI1_AD10	AG24
PCI1_AD08	AG25
PCI1_AD03	AG26
PCI1_AD06	AG27
TCK	AG28
USB1_DIR	AH1
USB1_PWRFAULT	AH2
USB3_D0	AH3
USB3_D2	AH4

Table 8. Pin List—By Pin Number (continued)

Signal	Pin
USB3_CLK	AH5
USB3_D5	AH6
USB3_D7	AH7
USB3_STP	AH8
USB3_PWRFAULT	AH9
SDHC_CMD	AH10
GPIO4_SDHC_CD_B	AH11
SDHC_DAT1	AH12
SDHC_DAT2	AH13
SYSCLK	AH14
IIC2_SCL	AH15
AVDD_CORE	AH16
CKSTP_OUT_B	AH17
AVDD_PLAT	AH18
AVDD_DDR	AH19
AVDD_PCI1	AH20
TRST_B	AH21
IIC1_SDA	AH22
PCI1_AD11	AH23
PCI1_AD12	AH24
PCI1_C_BE0_B	AH25
PCI1_CLK	AH26
TMS	AH27
TDI	AH28

5 Clocks

Figure 10 shows the internal distribution of clocks within the MPC8536E.

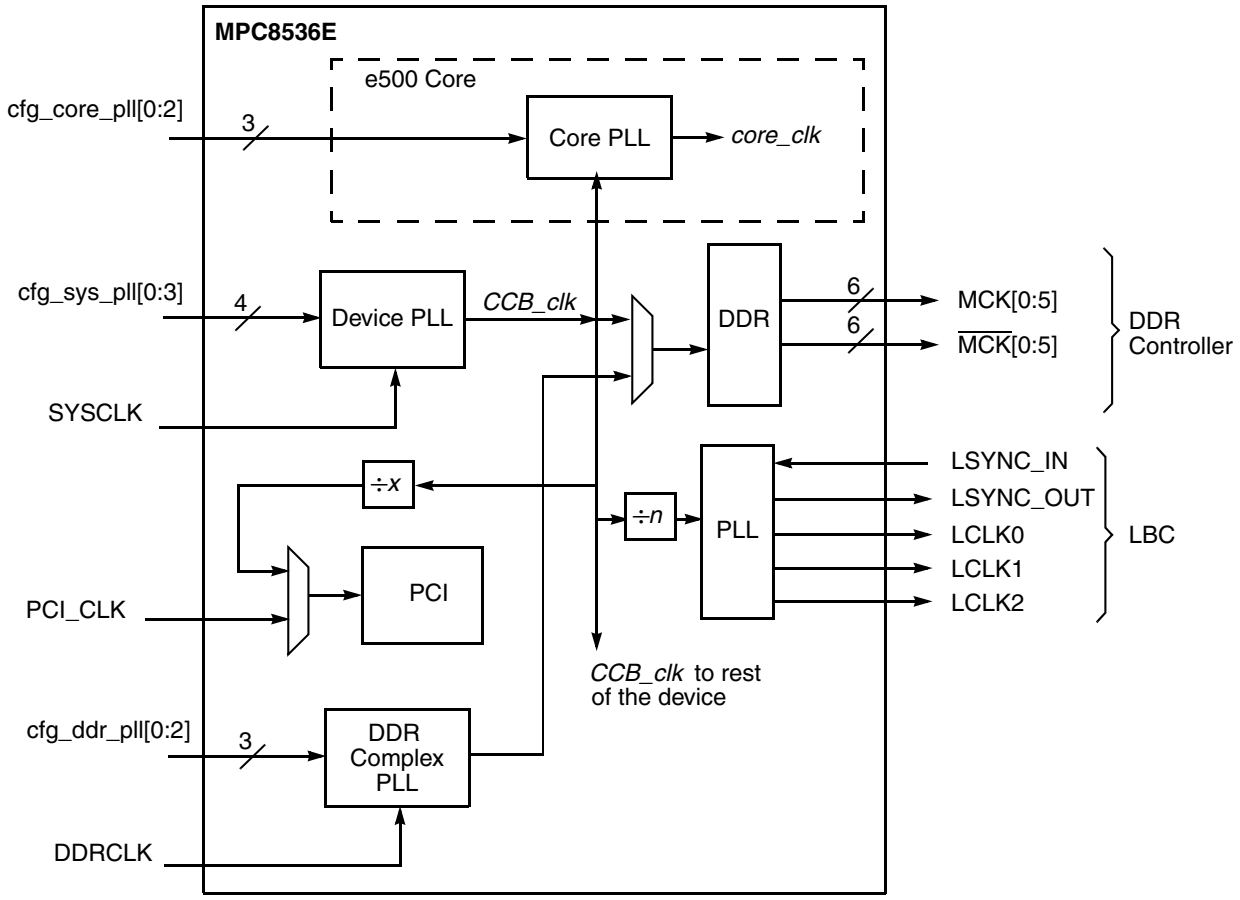


Figure 10. Clock Subsystem Block Diagram

The clock inputs for the MPC8536E are the SYSCLK, DDR_CLK, EC_GTX_CLK125, PCI1_CLK, RTC, SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$, and SD2_REF_CLK/SD2_REF_CLK. SYSCLK is the primary clock input to the device. DDRCLK is the reference clock used for the DDR interface when it is configured in asynchronous mode. The EC_GTX_CLK125 input is used by the eTSEC controller as a reference clock for gigabit Ethernet modes. The PCI1_CLK input are PCI clock input if the PCI controller is configured in asynchronous mode. SD1_REF_CLK/SD1_REF_CLK is the reference clock for the PCI Express interfaces, while SD2_REF_CLK/SD2_REF_CLK is the reference clock for the SGMII and SATA interfaces. Table 10 shows how the clock pins should be connected.

Disable the clocks that are not used via the DDRCLKDR register. By default, all clocks are operational, but not all clock signals are used in a given application. Therefore, disabling the unused clocks first lowers the power consumption and then lowers the unused switching activity in the part. DDRCLKDR is not a part of the memory controller register set; it is located in the global utility register section

Table 10. Clock Pin Recommendations

Pin Name	Pin Used	Pin Not Used
DDRCLK	If DDR is configured in asynchronous mode, connect to an input clock of 66–166 MHz.	Connect to GND through a 2–10 kΩ resistor.
EC_GTX_CLK125	If any of the eTSECs are used in gigabit mode, connect to a 125 MHz clock.	Pull high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively.
PCI1_CLK	If PCI1 is configured for PCI and asynchronous mode, connect to a 16–66 MHz clock. If PCI1 is configured for PCI-X and asynchronous mode, connect to a 66–133 MHz clock.	Pull high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
RTC	If used, connect to a clock that runs no greater than 1/4 the platform CCB_clk.	Pull high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
SD_REF_CLK/ SD_REF_CLK	If the SerDes1 is enabled at POR, connect to a clock at the frequency specified per the POR I/O port selection.	These pins must be connected to XGND.
SD2_REF_CLK/ SD2_REF_CLK	If the SerDes2 is enabled at POR, connect to a clock at the frequency specified per the POR I/O port selection.	These pins must be connected to X2GND.
SYSCLK	This must always be connected to an input clock of 33–133 MHz	

5.1 System PLL Ratio

The system PLL inputs, shown in Table 11, establish the clock ratio between the SYSCLK input and the platform clock used by the MPC8536E. Note that x8 PCI Express is only available at core complex bus (CCB) clock rates of 527 MHz and above.

Table 11. CCB Clock Ratio

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	16:1	1000	8:1
0001	Reserved	1001	9:1
0010	Reserved	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1
0101	5:1	1101	Reserved
0110	6:1	1110	Reserved
0111	Reserved	1111	Reserved

5.2 e500 Core PLL Ratio

Table 12 describes the e500 core clock PLL inputs that program the core PLL and establish the ratio between the e500 core clock and the e500 CCB clock.

Table 12. e500 Core to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1	100	2:1
001	9: 2 (4.5:1)	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

5.3 DDR PLL Ratio

The DDR memory controller can run in either synchronous or asynchronous mode depending on its configuration.

- When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. The memory buses are clocked at half the platform clock rate.
- When running in asynchronous mode, the memory bus is sourced from a separate PLL than the rest of the platform.

The DDR PLL ratio, shown in Table 13, establishes the ratio between the DDRCLK input and the DDR complex clock. The DDR complex clock is divided by two before being provided to the DDR interface. Since DDR data is transferred on both the rising and falling edges, the DDR data rate is equal to the DDR complex clock frequency.

Table 13. DDR Complex Clock PLL Ratio

Functional Signals	Reset Configuration Name	Value (Binary)	DDR Complex Clock:DDRCLK Ratio
TSEC_1588_TRIG_OUT[0:1], TSEC_1588_CLK_OUT Default (111)	cfg_ddr_pll[0:2]	000	3 : 1
		001	4 : 1
		010	6 : 1
		011	8 : 1
		100	10 : 1
		101	12 : 1
		110	Reserved
		111	Synchronous mode

5.4 System Speed Configuration

The SYSCLK speed configuration inputs, shown in Table 14, configure internal logic for proper operation with the SYSCLK clock frequencies in use. The default setting is appropriate for SYSCLK operating

above 66 MHz; for low speed operation (SYSCLK at or below 66 MHz) this POR configuration input should be low during HRESET. If this configuration is not set properly, behavior of the system may be unreliable.

Table 14. System Speed Configuration

Functional Signal	Reset Configuration Name	Value (Binary)	Meaning
LGPL1/LFALE Default (1)	cfg_sys_speed	0	SYSCLK frequency at or below 66 MHz
		1	SYSCLK frequency above 66 MHz

5.5 Core Speed Configuration

The core speed configuration inputs, shown in Table 15, configure internal logic for proper operation with the core clock frequencies in use. The default setting is appropriate for the core operating above 800 MHz; for low-speed operation (core at or below 800 MHz) this POR configuration input should be low during HRESET. If this configuration is not set properly, behavior of the system may be unreliable.

Table 15. Core Speed Configuration

Functional Signal	Reset Configuration Name	Value (Binary)	Meaning
LWE0/LBS0/LFWE Default (1)	cfg_core_speed	0	Core frequency at or below 800 MHz
		1	Core frequency above 800 MHz

6 DDR Interface

This section discusses the termination of DDR pins on the device. Table 16 shows how the DDR pins should be connected.

Table 16. DDR Pin Recommendations

Pin Name	Pin Used	Pin Not Used
MA[0:15]	Auto-precharge for DDR signaled on A10 when DDR_SDRAM_CFG[PCHB8] = 0. Auto-precharge for DDR signaled on A8 when DDR_SDRAM_CFG[PCHB8] = 1.	These pins may be left unconnected.
MBA[0:2]	—	
MCAS	—	
MCK/MCK[0:5]	—	Disable the clocks that are not used via the DDRCLKDR register
MCKE[0:3]	These pins are actively driven instead of being released to high impedance during reset.	These pins may be left unconnected
MCS[0:3]	—	

Table 16. DDR Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
MDIC[0:1]	When operating in DDR2 mode, connect MDIC[0] to ground through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor and connect MDIC[1] to GVDD through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect MDIC[0] to ground through an 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor and connect MDIC[1] to GVDD through an 20-Ω (full-strength mode) or 40-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.	
MDM[0:8]	—	These pins may be left unconnected.
MDQ[0:63]	—	These pins should be pulled low via a 2–10 kΩ resistor.
MECC[0:7]	—	
MDQS[0:8]	—	
$\overline{\text{MDQS[0:8]}}$		These pins should be pulled to GV_{DD} via a 2–10 kΩ resistor.
$\overline{\text{MAPAR\_ERR}}$		
MODT[0:3]	—	These pins may be left unconnected.
MRAS	—	
MAPAR_OUT	—	
MWE	—	

Note: Disable the clocks that are not used via the DDRCLKDR register. By default, all clocks are operational, but not all clock signals are used in a given application. Therefore, by disabling the unused clocks, it lowers the power consumption and lowers the unused switching activity in the part. DDRCLKDR is not a part of the memory controller register set; it is located in the global utility register section.

7 Debug and Test Interface

This section discusses the termination of debug and test pins on the device. Table 17 shows how the debug and test pins should be connected.

Table 17. Debug and Test Pin Recommendations

Pin Name	Pin Used	Pin Not Used
ASLEEP	This pin must not be pulled down during power-on reset.	This pin may be left unconnected.
CLK_OUT	This output is actively driven during reset rather than being released to high impedance during reset.	This pin may be left unconnected.
MDVAL	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	This pin must be left unconnected.

Table 17. Debug and Test Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
L1_TSTCLK	These signals must be pulled up via a 100–1000 Ω resistor to OV_{DD} for normal machine operation.	
L2_TSTCLK		
$\overline{\text{LSSD\_MODE}}$		
$\overline{\text{TEST\_SEL}}$		
MSRCID[0:1]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	This pin must be left unconnected.
MSRCID[2:4]	These pins must not be pulled down during power-on reset.	This pin must be left unconnected.
SD1_IMP_CAL_RX	This pin must be pulled down through a 200 Ω (±1%) resistor.	
SD1_IMP_CAL_TX	This pin must be pulled down through a 100 Ω (±1%) resistor.	
Pin T22, T23	Do not connect.	
SD1_PLL_TPD		
SD1_PLL_TPA		
SD2_IMP_CAL_RX	This pin must be pulled down through a 200 Ω (±1%) resistor.	
SD2_IMP_CAL_TX	This pin must be pulled down through a 100 Ω (±1%) resistor.	
Pin L8, L9	Do not connect.	
SD2_PLL_TPD		
SD2_PLL_TPA		
TRIG_IN	—	Tie low through a 2–10 kΩ resistor to GND.
TRIG_OUT/READY/ $\overline{\text{QUIESCE}}$	This pin must not be pulled down during power-on reset.	This pin must be left unconnected.

8 DMA Interface

This section discusses the termination of DMA pins on the device. Table 18 shows how the DMA pins should be connected.

Table 18. DMA Pin Recommendations

Pin Name	Pin Used	Pin Not Used
$\overline{\text{DMA\_DACK}}$[0:1]	—	These output pins may be left floating.
$\overline{\text{DMA\_DACK2}}$/$\overline{\text{LCS6}}$	—	If the local bus function of this pin is not used, this output pin may be left floating.
$\overline{\text{DMA\_DACK3}}$/IRQ10	—	Pull high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
$\overline{\text{DMA\_DREQ}}$[0:1]	—	Pull high through a 2–10 kΩ resistor to OV_{DD}.

Table 18. DMA Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
$\overline{\text{DMA\_DREQ2}}$/$\overline{\text{LCS5}}$	—	If the local bus function of this pin is not used, pull high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{DMA\_DREQ3}}$/IRQ9	—	Pull high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
$\overline{\text{DMA\_DDONE}}$[0:1]	—	These output pins may be left floating.
$\overline{\text{DMA\_DDONE2}}$/$\overline{\text{LCS7}}$	—	If the local bus function of this pin is not used, this output pin may be left floating.
$\overline{\text{DMA\_DDONE3}}$/IRQ11	—	Pull high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.

9 DUART Interface

This section discusses the termination of DUART pins on the device. Table 19 shows how the DUART pins should be connected.

Table 19. DUART Pin Recommendations

Pin Name	Pin Used	Pin Not Used
$\overline{\text{UART\_CTS}}$[0:1]	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{UART\_RTS}}$[0:1]	—	These output pins may be left floating.
UART_SIN[0:1]	—	Tie low through a 2–10 kΩ resistor to GND.
UART_SOUT[0:1]	This pin is a reset configuration pin that sets the device derivative. These pins may require 4.7 kΩ pull-up resistors.	

10 Ethernet Management Interface

This section discusses the termination of the Ethernet management pins on the device. Table 20 shows how the Ethernet management pins should be connected.

Table 20. Ethernet Management Pin Recommendations

Pin Name	Pin Used	Pin Not Used
EC_MDC	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
EC_MDIO	—	Tie high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.

11 eTSEC Interface

This section discusses the termination of the Ethernet pins on the device. Table 21 shows how the Ethernet pins should be connected.

Table 21. Ethernet Pin Recommendations

Pin Name	Pin Used	Pin Not Used
TSEC_1588_CLK	—	Tie low through a 2–10 kΩ resistor to GND.
TSEC_1588_TRIG_IN[0:1]	—	
TSEC_1588_TRIG_OUT[0:1]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
TSEC_1588_CLK_OUT		
TSEC_1588_PULSE_OUT1		
TSEC_1588_PULSE_OUT2		
TSEC1_COL	—	Tie low through a 2–10 kΩ resistor to GND.
TSEC3_COL	—	
TSEC1_CRS	—	
TSEC3_CRS	—	
TSEC1_GTX_CLK	—	These output pins may be left floating.
TSEC3_GTX_CLK	—	
TSEC1_RX_CLK	—	Tie high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively
TSEC3_RX_CLK	—	Tie high or low through a 2–10 kΩ resistor to TV_{DD} or GND, respectively.
TSEC1_RX_DV	—	Tie low through a 2–10 kΩ resistor to GND.
TSEC3_RX_DV	—	
TSEC1_RX_ER	—	
TSEC3_RX_ER	—	
TSEC1_RXD[7:0]	—	Tie high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively.
TSEC3_RXD[7:0]	—	Tie high or low through a 2–10 kΩ resistor to TV_{DD} or GND, respectively.
TSEC1_TX_CLK	—	Tie high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively
TSEC3_TX_CLK	—	Tie high or low through a 2–10 kΩ resistor to TV_{DD} or GND, respectively.
TSEC1_TX_EN	These pins require an external 4.7 kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven (during reset).	These output pins may be left floating.
TSEC3_TX_EN		

Table 21. Ethernet Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
TSEC1_TX_ER	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
TSEC3_TX_ER		
TSEC1_TXD[7:0]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
TSEC3_TXD[7:0]		

12 I²C Interface

This section discusses the termination of I²C pins on the device. Table 22 shows how the I²C pins should be connected.

Table 22. I²C Pin Recommendations

Pin Name	Pin Used	Pin Not Used
IIC1_SCL	Tie these open-drain signals high through a 1 kΩ resistor to OV_{DD}.	Tie high through a 2–10 kΩ resistor to OV_{DD}.
IIC2_SCL		
IIC1_SDA		
IIC2_SDA		

13 JTAG Interface

Correct operation of the JTAG interface requires that a group of system control pins be configured as demonstrated in Figure 12. Care must be taken to ensure that these pins are maintained at a valid de-asserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1™ specification, but it is provided on all processors built on Power Architecture™ technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources—such as voltage monitors, watchdog timers, power supply failures, or push-button switches—the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 12 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 11, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 11 is common to all known emulators.

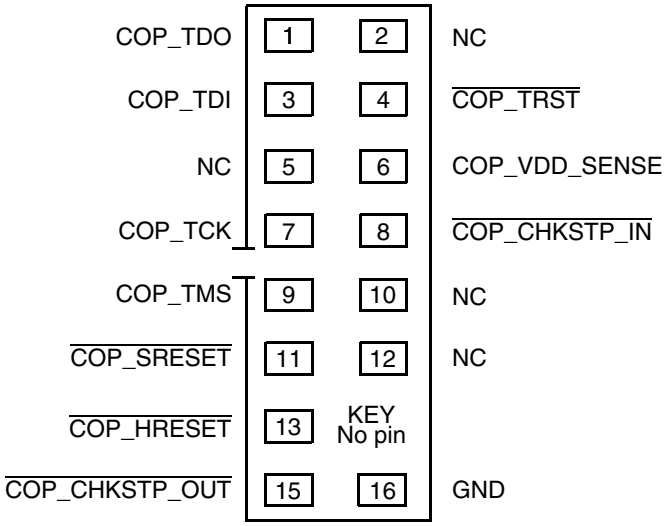
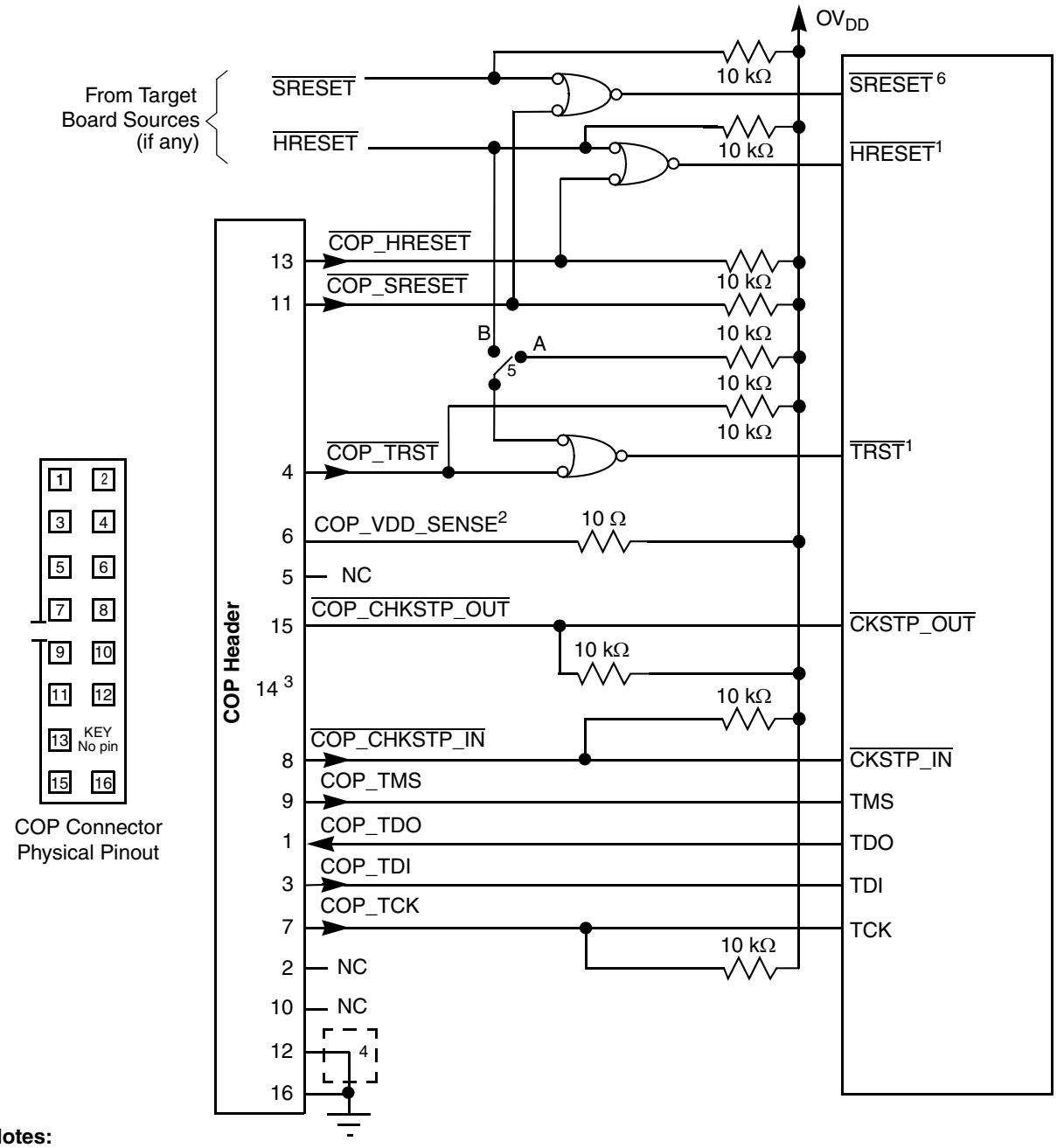


Figure 11. COP Connector Physical Pinout



Notes:

1. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown here.
2. Populate this with a 10-Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting SRESET causes a machine check interrupt to the e500 core.

Figure 12. JTAG Interface Connection

13.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 12. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pullup/pulldown is required for TDI, TMS, or TDO.

13.2 JTAG Pins

Table 23 shows how the JTAG pins should be connected.

Table 23. JTAG Pin Recommendations

Pin Name	Pin Used	Pin Not Used
TCK	If COP is used, connect as needed plus strap to OV_{DD} via 10K pullup. Connect to pin 7 of the COP connector	If COP is unused, tie TCK to OVDD through a 10-kΩ resistor. This prevents TCK from changing state and reading incorrect data into the device.
TDI	This pin has a weak internal pull-up P-FET that is always enabled. Connect to pin 3 of the COP connector	This pin may be left unconnected.
TDO	Connect to pin 1 of the COP connector	This pin may be left unconnected.
TMS	This pin has a weak internal pull-up P-FET that is always enabled. Connect to pin 9 of the COP connector	This pin may be left unconnected.
$\overline{\text{TRST}}$	This pin has a weak internal pullup P-FET that is always enabled. Connect to pin 4 of the COP connector and $\overline{\text{HRESET}}$ from the board	$\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω resistor.
VDD_SENSE	Connect to Pin 6 of the COP connector. Tie 10-Ω resistor to OVDD.	These pins may be left unconnected.
COP_CHKSTP_IN	Connect to Pin8 of the COP connector. Strap to OVDD via 10-kΩ resistor.	
$\overline{\text{COP\_SRESET}}$	Connect to Pin11 of the COP connector and $\overline{\text{SRESET}}$. Strap to OVDD via 10- kΩ resistor.	
$\overline{\text{COP\_HRESET}}$	Connect to Pin 13 of the COP connector and $\overline{\text{HRESET}}$. Strap to OVDD via 10-kΩ resistor.	
$\overline{\text{COP\_CHKSTP\_OUT}}$	Connect to Pin15 of the COP connector. Strap to OVDD via10-kΩ resistor.	

13.3 JTAG Checklist

Table 24 provides a summary POR and reset checklist for the designer.

Table 24. Checklist for JTAG

Item	Description	Completed
1.	Connect the JTAG pins to the COP header as shown in Figure 12.	

14 Enhanced Local Bus Controller

This section discusses the termination of the local bus pins on the device. Table 25 shows how the local bus pins should be connected.

Table 25. Local Bus Pin Recommendations

Pin Name	Pin Used	Pin Not Used
LA27	This pin is a reset configuration pin. It has a weak internal pullup P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LA[28:31]	This pin is a reset configuration pin that sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7 -kΩ pullup or pulldown resistors.	
LAD[0:31]	Note that the LSB for the address = LAD[24:31]; however, the MSB for the data is on LAD[0:7].	Tie high or low through a 2–10 kΩ resistor to BV_{DD} or GND, respectively, if the general purpose POR configuration is not used.
LALE	These pins are reset configuration pins that set the e500 core clock to CCB clock PLL ratio. These pins require 4.- kΩ pullup or pulldown resistors.	
LBCTL		
LCLK[0:2]	—	These output pins may be left floating.
$\overline{\text{LCS}}$[0:4]	—	
$\overline{\text{LCS5}}$/DMA_DREQ2	—	If the DMA functions of these pins are not used, these output pins may be left floating.
$\overline{\text{LCS6}}$/DMA_DACK2	—	
$\overline{\text{LCS7}}$/DMA_DDONE2	—	
LGPL0/LFCLE	This pin is a reset configuration pin. It has a weak internal pullup P-FET which is enabled only when the processor is in the reset state.	If the POR defaults are acceptable, these output pins may be left floating.
LGPL1/LFALE		
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	This pin is a reset configuration pin that sets the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pullup or pulldown resistors.	
LGPL3/$\overline{\text{LFWP}}$	This pin is a reset configuration pin. It has a weak internal pullup P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LGPL4/$\overline{\text{LGTA}}$/ LUPWAIT/LPBSE/LFRB	For systems that boot from local bus (GPCM)-controlled NOR flash or (FCM) controlled NAND flash, a 2–10 kΩ resistor pullup on LGPL4 is required.	This pin either needs to be pulled-up via a 2–10 kΩ resistor to BV_{DD} or needs to be reconfigured as LPBSE prior to boot-up.

Table 25. Local Bus Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
LGPL5	This pin is a reset configuration pin. It has a weak internal pullup P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LSYNC_IN LSYNC_OUT	LSYNC_IN needs to be connected via a trace to LSYNC_OUT of length equal to the longest LCK*n* signal used.	LSYNC_IN needs to be directly connected to LSYNC_OUT.
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/$\overline{\text{LFWE}}$ $\overline{\text{LWE[1:3]}}$/$\overline{\text{LBS[1:3]}}$	This pin is a reset configuration pin. It has a weak internal pullup P-FET which is enabled only when the processor is in the reset state.	If the POR defaults are acceptable, these output pins may be left floating.

15 PCI Interface

This section discusses the termination of PCI pins on the device.

15.1 Unrealized $\overline{\text{RST}}$ Pin

The MPC8536E does not implement for the PCI interface a specific RST pin separate from the rest of the device pins. Instead, the PCI $\overline{\text{RST}}$ is realized with the $\overline{\text{HRESET}}$ input.

15.2 PCI Pins

Table 26 shows how the PCI pins should be connected. Unless otherwise noted, unused inputs need be tied to their inactive state through a 2–10 kΩ resistor, and unused I/Os need be tied high or low through a 2–10 kΩ resistor to OV_{DD} and GND, respectively.

Table 26. PCI Pin Recommendations

Pin Name	Pin Used	Pin Not Used
PCI1_AD[31:0]	—	If PCI arbiter is enabled during POR, All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating. If PCI arbiter is disabled during POR, All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 1- kΩ resistor(s)
$\overline{\text{PCI1\_C\_BE[3:0]}}$	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
PCI1_CLK	If PCI1 is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI1_CLK, otherwise the processor will not boot up.	Tie high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively,
$\overline{\text{PCI1\_DEVSEL}}$ $\overline{\text{PCI1\_FRAME}}$	A weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.	
$\overline{\text{PCI1\_GNT0}}$	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.

Table 26. PCI Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
$\overline{\text{PCI1\_GNT}}$[4:3]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. When a PCI block is disabled, either the POR configuration pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI*n*_AD pins as 'No Connect' or terminated through 2–10 kΩ pullup resistors with the default of internal arbiter if the PCIn_AD pins are not connected to any other PCI device. The PCI block will drive the PCIn_AD pins if it is configured to be the PCI arbiter—through POR configuration pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.	If the POR defaults are acceptable, these output pins may be left floating.
$\overline{\text{PCI1\_GNT}}$[2:1]		If the POR defaults are acceptable, these output pins may be left floating.
PCI1_IDSEL	—	Tie low through a 2–10 kΩ resistor to GND.
$\overline{\text{PCI1\_IRDY}}$	A weak pull-up resistor (2–10 kΩ) need be placed on this pin to OV_{DD}.	
PCI1_PAR	—	Tie low through a 2–10 kΩ resistor to GND.
—	—	
$\overline{\text{PCI1\_PERR}}$	A weak pull-up resistor (2–10 kΩ) need be placed on this pin to OV_{DD}.	
$\overline{\text{PCI1\_REQ0}}$	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{PCI1\_REQ}}$[4:1]	—	
$\overline{\text{PCI1\_SERR}}$	A weak pull-up resistor (2–10 kΩ) need be placed on this pin to OV_{DD}.	
$\overline{\text{PCI1\_STOP}}$		
$\overline{\text{PCI1\_TRDY}}$		

16 PIC Interface

This section discusses the termination of programmable interrupt controller (PIC) pins on the device. Table 27 shows how the PIC pins should be connected.

Table 27. PIC Pin Recommendations

Pin Name	Pin Used	Pin Not Used
IRQ[0:8]	A weak pull-up or pull-down may be needed to the inactive state.	Tie high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively,
IRQ9/$\overline{\text{DMA\_DREQ3}}$		
IRQ10/$\overline{\text{DMA\_DACK3}}$		
IRQ11/$\overline{\text{DMA\_DDONE3}}$		

Table 27. PIC Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
$\overline{\text{IRQ\_OUT}}$	Pull high through a 2–10 kΩ resistor to OV_{DD}.	
$\overline{\text{MCP}}$		
$\overline{\text{UDE}}$		

17 USB Interface

The MPC8536E implements a dual-role (DR) USB module. It is a USB 2.0-compliant serial interface engine for implementing a USB interface. The USB DR module can act as a device or host controller. Table 28 shows how the USB pins should be connected.

NOTE

Reset for a USB PHY (Physical Layer Transceiver) should not be de-asserted prior to the HRESET de-assertion of the device. The device may drive USB_STP signal low during the reset sequence due to the POR configuration. If the reset for the PHY de-asserts before the de-assertion of the device HRESET, the USB_DIR signal may be driven low by the PHY and the PHY may mistakenly treat the data as valid since USB_STP is also driven low. This can cause the PHY to hang. The reset for the USB PHY can be connected to the device HRESET signal such that both are de-asserted at the same time.

NOTE

The USB PHY that connected to MPC8536 USB controller must comply with ULPI Specification Rev 1.1.

Table 28. Universal Serial Bus Pin Listing

Pin Name	Pin Used	Pin Not Used
USBx_D[0:7][1]	—	1 kΩ to GND
USBx_NXT[1]	—	1 kΩ to GND
USBx_DIR[1]	—	1 kΩ to GND
USBy_STP[2]	This pin is a reset configuration pin. It has a weak internal pullup P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
USB3_STP	—	1 kΩ to GND
USBx_PWRFAULT[1]	—	1 kΩ to GND
USBx_PCTL0[1]	—	Open
USBx_PCTL1[1]	—	Open

Table 28. Universal Serial Bus Pin Listing (continued)

Pin Name	Pin Used	Pin Not Used
USBx_CLK[1]	—	1 kΩ to GND

Notes:
1. The x value is 1, 2, or 3 corresponding to USB controller 1, 2, or 3, respectively.
2. The y value is 1 or 2 corresponding to USB controller 1 or 2, respectively.

18 eSDHC Interface

The enhanced SD host controller (eSDHC) provides an interface between the host system and SD/SDIO/MMC cards. Table 19 shows how the eSDHC pins should be connected.

Table 29. eSDHC Pin Listing

Pin Name	Pin Used	Pin Not Used
SDHC_CLK	33 Ω serial resistor must be provided for SDHC_CLK and placed close to MPC8536 device.	This output pin may be left floating
SDHC_CMD	10 k–100 kΩ to OV_{DD}	10 k–100 kΩ to OV_{DD}
SDHC_DAT[2:0]	10 k–100 kΩ to OV_{DD}	10 k–100 kΩ to OV_{DD}
SDHC_DAT[3]	10 k-100 k to OVDD is required during the normal operating conditions. Board should have a 160 K pull-down resistor if DAT3 is used for a SD card detection. In this case, the pull-up resistor should be disconnected during the identification phase. The pull-up resistor should be connected and the pull-down resistor should be switched out after the identification phase. Please check the application note for card detection provided by the SD organization for details.	10 k–100 kΩ to OV_{DD}
SDHC_DAT[4:7]	PMUXCR[SD_DATA] to be 1. 10 k–100 kΩ to OV_{DD}	10 k–100 kΩ to OV_{DD}
$\overline{\text{SDHC\_CD}}$	See the *MPC8536E PowerQUICC™ III Integrated Processor Family Reference Manual,* for more details about its polarity	2 k–10 kΩ to OV_{DD}
$\overline{\text{SDHC\_WP}}$	See the *MPC8536E PowerQUICC™ III Integrated Processor Family Reference Manual,* for more details about its polarity.	2 k–10 kΩ to OV_{DD}

19 eSPI

Table 30 lists the eSPI pins and the recommended connections.

Table 30. eSPI Pin Listing

Pin Name	If Used	If Not Used
SPIMOSI	As needed + 2 k–10 kΩ to OV_{DD}	2 k–10 kΩ to OV_{DD}
SPIMISO	As needed + 2 k–10 kΩ to OV_{DD}	2 k–10 kΩ to OV_{DD}

Table 30. eSPI Pin Listing (continued)

Pin Name	If Used	If Not Used
SPI_CLK	As needed + 2 k–10 kΩ to OV_{DD}	This output pin may be left floating
SPI_CS[0:3]	As needed + 2 k–10 kΩ to OV_{DD} (PMUXCR[SD_DATA] to be 0)	2 k–10 kΩ to OV_{DD}

20 SerDes Interface

This section discusses the termination of SerDes pins on the device. See *Motherboard/BIOS Compliance Checklist for the PCI Express Base 1.0a Specification* available from http://www.pci-sig.org for a list of PCB design recommendations for PCI Express interconnects.

Table 31 and Table 32 show how the SerDes pins should be connected. Note that SerDes must always have power applied to its supply pins. Also note that a valid clock input is required on SD_REF_CLK if SerDes is enabled. Failure to provide a reference clock for an enabled SerDes block prevents the device from completing POR sequence.

NOTE

Please check section “Guidelines for High-Speed Interface Termination” as well as “High Speed Serial Interfaces” of the *MPC8536EEC*.

Table 31. SerDes1 Pin Recommendations

Pin Name	Pin Used	Pin Not Used
SD1_PLL_TPD	Do not connect.	
SD1_PLL_TPA		
SD1_RX[0:7]	—	These pins must be connected to GND.
$\overline{\text{SD1\_RX}}$[0:7]		
SD1_TX[0:7]	—	These pins must be left unconnected.
$\overline{\text{SD1\_TX}}$[0:7]		
SD1_IMP_CAL_RX	This pin must be pulled down through a 200-Ω resistor.	
SD1_IMP_CAL_TX	This pin must be pulled down through a 100-Ω resistor.	
SD1_REF_CLK	If SerDes is enabled via POR configuration pins, connect to a clock at the frequency specified per the POR I/O Port	These pins must be connected to GND.
$\overline{\text{SD1\_REF\_CLK}}$		
Reserved (T22)	Do not connect.	
Reserved (T23)	Do not connect.	

Table 32. SerDes2 Pin Recommendations

Pin Name	Pin Used	Pin Not Used
SD2_PLL_TPD	Do not connect.	
SD2_PLL_TPA		
SD2_RX[0:3]	—	These pins must be connected to GND.
$\overline{\text{SD2\_RX[0:3]}}$	—	These pins must be connected to GND.
SD2_TX[0:3]	—	These pins must be left unconnected.
$\overline{\text{SD2\_TX[0:3]}}$		
SD2_IMP_CAL_RX	This pin must be pulled down through a 200-Ω resistor.	
SD2_IMP_CAL_TX	This pin must be pulled down through a 100-Ω resistor.	
SD2_REF_CLK	If SerDes is enabled via POR configuration pins, connect to a clock at the frequency specified per the POR I/O Port	These pins must be connected to GND.
SD2_REF_CLK		
Reserved (L8)	Do not connect.	
Reserved (L9)	Do not connect.	

21 System Control

This section discusses the termination of system control pins on the device. Table 33 shows how the system control pins should be connected.

Table 33. System Control Pin Recommendations

Pin Name	Pin Used	Pin Not Used
$\overline{\text{CKSTP\_IN}}$	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to pin 8 of the COP connector (refer to Figure 12).	Pull high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{CKSTP\_OUT}}$	Pull this open-drain signal high through a 2–10 kΩ resistor to OV_{DD}. Connect to pin 15 of the COP connector (refer to Figure 12).	Pull high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{HRESET}}$	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to c 13 of the COP connector (refer to Figure 12).	
$\overline{\text{HRESET\_REQ}}$	Pull high through a 2–10 kΩ resistor to OV_{DD}. This pin must not be pulled down during power-on reset.	This pin must not be pulled down during power-on reset.
$\overline{\text{SRESET}}$	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to pin 11 of the COP connector (refer to Figure 12).	Pull high through a 2–10 kΩ resistor to OV_{DD}.

22 Power Management Control

This section discusses the use and termination of POWER_OK and POWER_EN pins for the Power Management Control. Table 34 shows how the pins should be connected

Table 34. Power Management Control Pin Recommendations

Pin Name	Pin Used	Pin Not Used
POWER_OK	Directly connect to external power switch device	Pull high through a 2-10 kΩ resistor to OV_{DD}
POWER_EN		

23 Spare Configuration Pins

Several pins on the MPC8536E are marked per configuration as shown in Table 35. The spare pins are unused POR configuration pins. It is highly recommended that the customer provide the capability of setting these pins low (that is, pull-down resistor which is not currently stuffed) in order to support new configuration options should they arise between revisions.

Table 35. Reserved Pin Recommendations

Pin Name	Pin Number	Comment
EC_MDC	Y10	cfg_eng_use[0]
TSEC1_TXD[3]	W3	cfg_eng_use[1]
TSEC3_TXD[7]	T12	cfg_eng_use[2]

24 Power and Ground Signals

The MPC8536E has several power supplies. Table 36 describes each of the power supplies.

Table 36. Power and Ground Pin Recommendations

Pin	Comment
AV_{DD}_CORE	Power supply for e500 PLL. It should be the same as V_{DD}_CORE.
AV_{DD}_LBIU	Power supply for local bus PLL (1.0 V through a filter)
AV_{DD}_PCI1	Power supply for PCI1 PLL (1.0 V through a filter)
AV_{DD}_PLAT	Power supply for core complex bus PLL. (1.0 V through a filter)
AV_{DD}_DDR	Power supply for DDR PLL (1.0 V through a filter)
AV_{DD}_SRDS	Power supply for SerDes1 PLL (1.0 V through a filter)
AV_{DD}_SRDS2	Power supply for SerDes2 PLL (1.0 V through a filter)
BV_{DD}	Power supply for local bus I/Os (1.8 V, 2.5 V/3.3 V)
GND	Ground

Table 36. Power and Ground Pin Recommendations (continued)

Pin	Comment
GV_{DD}	Power supply for DDR I/Os (1.8 V / 1.5 V).
LV_{DD}	Power supply for TSEC1 I/Os (2.5 V / 3.3 V).
MVREF	DDR input reference voltage equal to approximately half of GV_{DD}
OV_{DD}	General I/O supply (3.3 V)
SENSEVDD_CORE	This pin is connected to the V_{DD}_CORE plane internally and may be used by the core power supply to improve tracking and regulation.
SENSEVDD_PLAT	This pin is connected to the V_{DD}_PLAT plane internally and may be used by the core power supply to improve tracking and regulation.
SENSEVSS	This pin is connected to the GND plane internally and may be used by the core power supply to improve tracking and regulation.
SV_{DD}	Power supply for SerDes1 transceivers (1.0 V)
$S2V_{DD}$	Power supply for SerDes2 transceivers (1.0 V)
XV_{DD}	Pad Power for SerDes1 transceivers (1.0 V)
$X2V_{DD}$	Pad Power for SerDes2 transceivers (1.0 V)
XGND	SerDes1 GND
X2GND	SerDes2 GND
AGND_SRDS	SerDes1 PLL GND
AGND_SRDS2	SerDes2 PLL GND
TV_{DD}	Power supply for TSEC3 I/Os (2.5 V/3.3 V)
V_{DD_CORE}	Power supply core(1.0 V/1.1 V)
V_{DD_PLAT}	Power supply platform logic (1.0 V)

25 Documentation History

Table 37 provides a revision history for this application note.

Table 37. Document Revision History

Rev. Number	Date	Substantive Change(s)
2	04/2014	• Modified Table 34, Power Management Control Pin Recommendations In Table 29: • Modified the description for SDHC_DAT3 • Added resistor requirement to the SDHC_CLK pin
1	01/2011	• Added MPC8535-related information. • Updated Section 1.2, “References.” • Added Rev 1.2 to Table 2, “MPC8536E PowerQUICC III Product Revisions.” • Replaced the table “Power Dissipation Estimated For Low-Power Modes,” with a note. • Updated Section 2.3, “Power Sequencing.” • Modified Table 3, “Power Supply Checklist.” • Modified Table 6, “Checklist for POR and Reset Configurations” • Updated pins AD13, AD14, AE13, and P2 in Figure 4–Figure 6, and Table 7–Table 8. • Added a paragraph about disabling the DDR clock to Section 5, “Clocks.” • Updated the beginning of Section 5.3, “DDR PLL Ratio.” • Updated description for MDIC and MCK and added a note in Table 16, “DDR Pin Recommendations.” • Modified description for UART_SOUT in Table 19, “DUART Pin Recommendations.” • Added IEEE1588 pins to Table 21, “Ethernet Pin Recommendations.” • Updated Table 23, “JTAG Pin Recommendations.” • Updated Table 25, “Local Bus Pin Recommendations,” regarding connections for LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE/LFRB. • Added two notes to Section 17, “USB Interface,” regarding to the reset PHY. • Updated Table 29, “eSDHC Pin Listing.” • Updated Table 30, “eSPI Pin Listing.” • Added a note and a paragraph to Section 20, “SerDes Interface.” • Updated Table 31, “SerDes1 Pin Recommendations.” • Updated Table 32, “SerDes2 Pin Recommendations” • Updated Table 35, “Reserved Pin Recommendations.” • Updated Table 36, “Power and Ground Pin Recommendations.”
0	02/2009	• Initial release.

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