Freescale Semiconductor
Application Note

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System Design Using the ColdFire MCF5208 Split Bus Architecture

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The MCF5208 implements a bus architecture scheme designed to allow for maximum flexibility of the external memory subsystem without adding extra pins to the chip. This document discusses the use of the split bus architecture implemented on the MCF5208, including an overview of the features and design considerations, as well as example block diagrams.

Contents

1 Overview

To allow for flexibility and ease of system migration and upgrades, the MCF5208 has been designed to work with several different types of SDRAM devices. The MCF5208 supports connection to single data rate (SDR) and double data rate (DDR) SDRAMs, as well as mobile DDR devices. This flexibility in memory selection is not without challenges though. The timing and signal routing requirements for a design incorporating DDR mean that using a shared data bus for SDRAM accesses and standard external access (flash, SRAM, peripherals, etc.) can make system design more complicated.

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To simplify the routing for DDR SDRAM, the MCF5208 implements a programmable split bus architecture. This bus architecture simplifies system design using DDR memory while keeping pin count and cost low. A shared address bus is used for SDRAM and FlexBus accesses, but the data bus can be configured as a shared 32-bit SDRAM and FlexBus bus (similar to the way many previous ColdFire devices, such as the MCF5282 operate), or as two separate 16-bit data buses where the upper 16-bits of the bus are used exclusively for SDRAM controller cycles and the lower 16-bits of the data bus are dedicated to the FlexBus.

1.1 Split Bus Features

The split bus architecture includes the following features:

- Full 32-bit bus mode
  - 32-bit data port for FlexBus cycles (D[31:0])
  - 32-bit data port for SDRAM cycles (D[31:0])
- Split 16-bit bus mode
  - Dedicated 16-bit data port for FlexBus cycles (D[15:0])
  - Dedicated 16-bit data port for SDRAM cycles (D[31:16] used as SD_D[31:16])
- Address bus is always shared for FlexBus and SDRAM (A[23:0])
- Operating mode is selectable at reset using DRAMSEL pin

1.2 Bus Mode Selection

The state of the DRAMSEL pins is sampled at reset to select between the two modes. The 32-bit bus mode is recommended for systems using SDR SDRAM or no SDRAM. If DDR is used, then the split 16-bit bus option must be selected. The operating mode selected at reset determines the available port sizes for FlexBus accesses. If the 32-bit bus mode is selected, then the FlexBus supports 32-, 16-, and 8-bit port sizes. If the split 16-bit bus mode is used, then the FlexBus supports 16- and 8-bit port sizes. Programming a chip select control register (CSCR*n*) for a 32-bit port size while in split bus mode results in undefined behavior.

When DRAMSEL is high, the 32-bit bus mode is selected. D[31:0] switches dynamically between SDRAM and FlexBus accesses as needed. When DRAMSEL is low, the 16-bit bus mode is used. In 16-bit bus mode, the upper half of the data bus (D[31:16]) is dedicated to SDRAMC accesses, while the lower half of the data bus (D[15:0]) is used for FlexBus accesses. Because the routing and timing on the data signals is critical for DDR system design, the dedicated 16-bit SDRAM data port means that lines are not shared between DDR and memory or peripherals on the FlexBus. Therefore, data lines for the DDR can be routed point-to-point. This makes it much easier to keep trace lengths short, match the trace lengths, and minimize bus loading.

2 System Examples

The following sections include example block diagrams for two systems—one using the bus in 32-bit mode with SDR SDRAM and one using the bus in 16-bit mode with DDR SDRAM. For more information on the SDRAM and FlexBus control signals and bus timing, please refer to the *MCF5208 Reference Manual* and the *MCF5208 Hardware Specification*.

2.1 SDR SDRAM Example

Figure 1 shows the block diagram for an MCF5208 system using 32-bit wide SDR SDRAM (such as Micron MT48LC4M32B2) and flash (such as Spansion AM29LV160D).

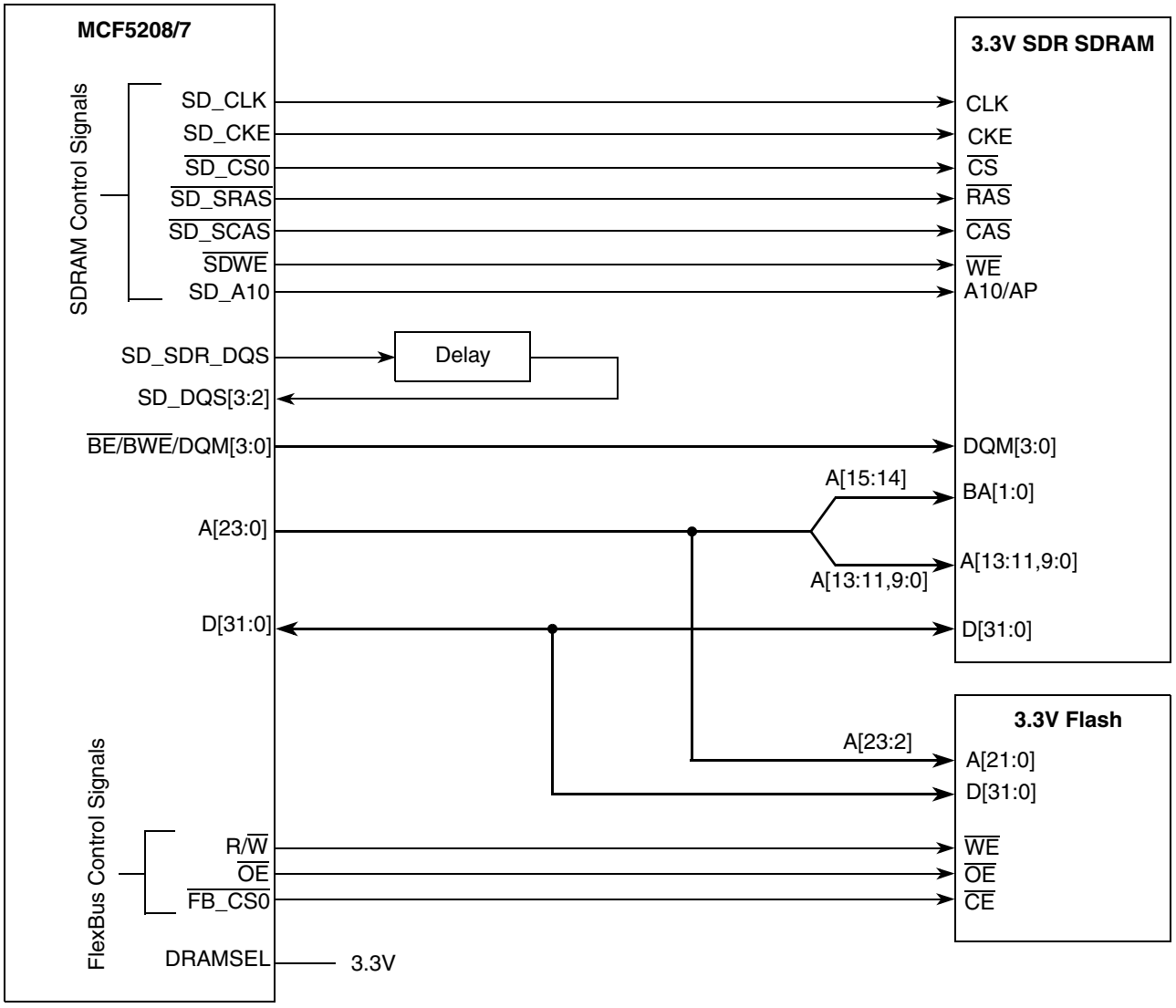

Figure 1. Example 3.3V, 32-bit SDR SDRAM System

In this diagram, DRAMSEL is pulled high through a resistor to enable the full 32-bit shared bus mode. Because SDR SDRAM is being used, the SD_VDD supply should be powered at 3.3V. Therefore, the address, data, SDRAM control signals, and FlexBus control signals are all powered off the 3.3V supply.

The address bus is connected to the SDRAM and flash devices. Because the bus is operating in 32-bit shared bus mode, the data bus is shared between both devices.

Figure 1 shows the address line connections for the maximum size memories that can be supported. If all of the external address lines are used, the MCF5208 can address up to 16 MBytes of flash connected to FB_CS0. If less memory is connected, then fewer address lines are needed. The maximum SDR SDRAM configuration is also shown (up to 256 MBytes per chip select). If a smaller SDRAM is used in a system, then less address lines are connected.

Most of the SDRAM control signal connections are fairly straightforward; however, the SD_SDR_DQS is used differently than the other control signals. The SDRAMC uses the SD_DQS[3:2] signals to determine when read data can be latched for SDRAM accesses. Because SDR memories do not provide DQS outputs, the SDRAMC provides the SD_SDR_DQS output that is routed back into the controller as SD_DQS[3:2]. The SD_SDR_DQS signal should be routed such that the valid data from the SDRAM reaches the MCF5208 at the same time or before the SD_SDR_DQS reaches the SD_DQS[3:2] inputs. When routing SD_SDR_DQS, the outbound trace length should be matched to the SD_CLK trace length. This aligns SD_SDR_DQS to the SD_CLK as if the memory had generated the DQS pulse. The inbound trace should be routed along the data path. This should synchronize the SD_DQS[3:2] so that the data is latched in the middle of the data valid window.

2.2 DDR SDRAM Example

Figure 2 shows the block diagram for an MCF5208 system using 16-bit wide DDR SDRAM (such as Micron MT46V8M16) and flash (such as Spansion AM29DBB160G).

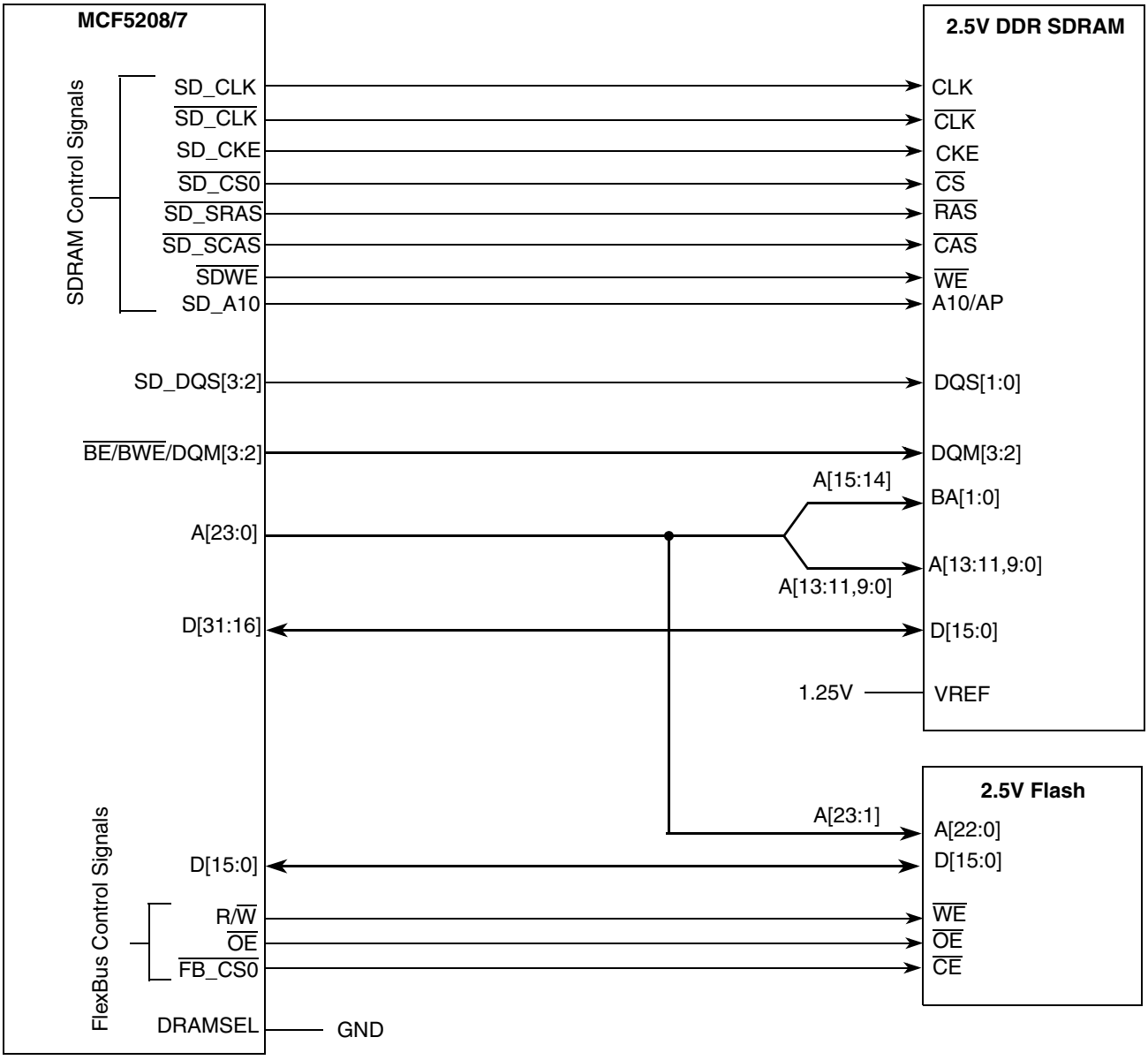

Figure 2. Example 2.5V, 16-bit DDR SDRAM System

In this diagram, DRAMSEL is pulled low through a resistor to enable the 16-bit split bus mode. Because DDR SDRAM is being used, the SD_VDD supply should be powered at 2.5V. Therefore, the address, data, SDRAM control signals, and FlexBus control signals are all powered off the 2.5V supply. The address bus is connected to the SDRAM and flash devices, but the data bus is not shared. The upper half of the data bus (D[31:16]) is a dedicated 16-bit port for the DDR SDRAM. While the lower half of the data bus (D[15:0]) is used for FlexBus accesses.

As in the SDR example, Figure 2 shows the address line connections for the maximum size memories that can be supported. The change in port size does not impact the maximum memory configurations. Up to 16 MBytes of memory can be connected to one of the FlexBus chip selects, and up to 256 Mbytes of DDR

SDRAM can be connected to the SDRAMC chip select signals. If smaller memories are used, then less address lines should be connected to the memories.

Care should be taken when routing the control, data, and address signals to the DDR SDRAM. Unlike most DDR designs, the MCF5208 does not require the use of parallel termination resistors for the DDR signals. Refer to the *MCF5208 Reference Manual* for more information on DDR layout recommendations.

2.3 Mobile DDR SDRAM Example

Figure 3 shows the block diagram for an MCF5208 system using 16-bit wide mobile DDR SDRAM (such as Micron MT46H8M16LF) and flash (such as Spansion AM29BDS640G).

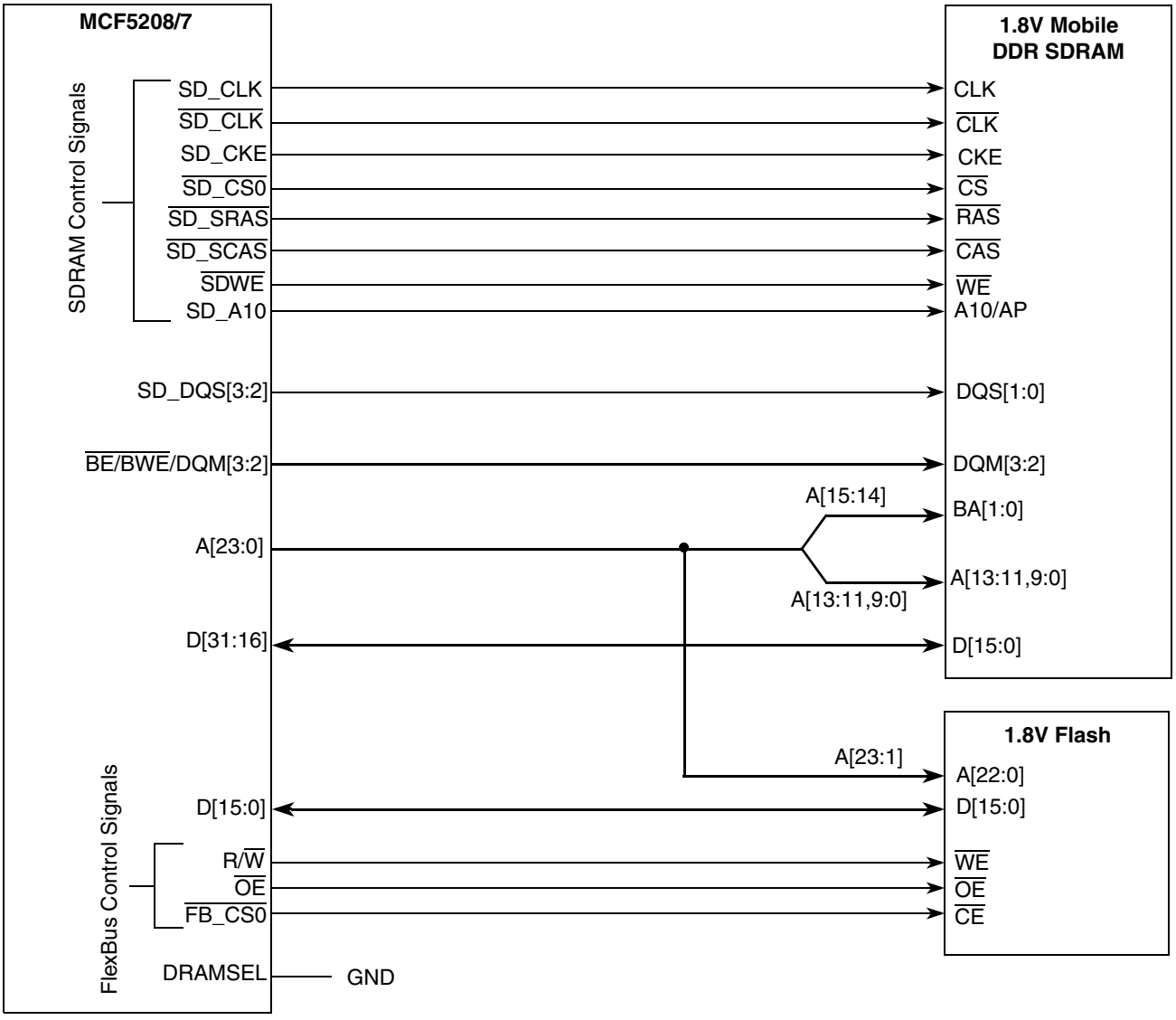

Figure 3. Example 1.8V, 16-bit Mobile DDR SDRAM System

The connections used for a mobile DDR system are largely the same as those used for regular 2.5V DDR SDRAM. The only differences are that the voltage supply is 1.8V instead of 2.5V, and mobile DDR does not require a VREF input. In Figure 3, because mobile DDR SDRAM is being used, the SD_VDD supply should be powered at 1.8V. Therefore, the address, data, SDRAM control signals, and FlexBus control signals are all powered off the 1.8V supply. The address bus is connected to the SDRAM and flash devices, but the data bus is not shared. The upper half of the data bus (D[31:16]) is a dedicated 16-bit port for the DDR SDRAM, while the lower half of the data bus (D[15:0]) is used for FlexBus accesses.

2.4 Using SDR SDRAM in Split Bus Mode

Although the shared 32-bit bus mode is the recommended mode when using SDR SDRAM, some SDR-based designs can benefit from using the split bus mode. If a system uses a 16-bit data port for SDR SDRAM, then using the split bus mode can help to simplify signal routing. The data bus connections would be the same as shown in Section 2.2, “DDR SDRAM Example.” The layout benefits are similar to those for DDR systems. The point-to-point routing for data signals helps to reduce loading on the data lines and allows for shorter trace lengths. The higher transfer rates for DDR SDRAM make these issues critical for DDR based designs, but SDR based designs can benefit from the reduced loading and simpler routing as well. However, because the address bus is shared in all configurations, using the split bus mode does not allow for concurrent accesses to SDRAM and memories connected to FlexBus chip selects. Therefore, the advantage of using the split bus mode is simplified data bus routing, not an increase in bus bandwidth.

3 Summary

The MCF5208 split data bus allows for flexibility and ease of use for a variety of SDRAM memory devices. Using a 32-bit port with SDR SDRAM allows for maximum bus throughput when a shared bus is practical. The option for a dedicated 16-bit data port for DDR SDRAM allows for the same throughput of an SDR based system with simplified data bus routing.

4 References

Table 1. References

Freescale Document Number	Title	Revision
MCF5208RM	MCF5208 Microprocessor Reference Manual	0
MCF5208EC	MCF5208 Integrated Microprocessor Hardware Specifications	0

5 Document Revision History

Table 2 provides a revision history for this application note.

Table 2. Document Revision History

Rev. No.	Substantive Change(s)	Date of Release
0	Official release	May 2005
1	Corrected the maximum amount of flash memory per chip (was 32 MBytes, is 16 MBytes).	February 2007

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