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EIM Asynchronous Timing Parameters

MC9328MX1, MC9328MXL, and MC9328MXS

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1 Abstract

This document provides a detailed overview of the i.MX applications processor's External Interface Module (EIM), specifically analyzing the asynchronous timing parameter bit settings of the EIM chip-select control register. This analysis provides the user a better understanding of how these bits are used and how they affect the timing parameters of several of the EIM's control signals, to better enable the system design in interfacing the i.MX processor's EIM to external memories and peripherals. An overview of the EIM and its chip-select control registers is provided, followed by several example waveforms to illustrate how changing these bit settings affects the asynchronous timing parameters of the external control signals. The aim of this document is to supplement the EIM information provided in the i.MX reference manuals and data sheets.

This document applies to the following i.MX devices, collectively called i.MX throughout:

- MC9328MX1
- MC9328MXL
- MC9328MXS

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2 Overview of the i.MX EIM

The i.MX is an application processor targeted for low power, portable applications. Part of the rich feature set of the i.MX includes the on-chip External Interface Module (EIM). The EIM may be used to interfacing the i.MX to external memory such as SRAM and NOR Flash (asynchronous, synchronous/burst, and page mode styles), as well as interfacing to external peripheral devices such as the ST16C2552 Dual UART chip. The i.MX EIM includes these distinctive features:

- Six chip selects for external devices: $\overline{CS}$[0], covering a range of 32 Mbyte, and $\overline{CS}$[1]–$\overline{CS}$[5], covering a range of 16 Mbyte each
- Selectable protection for each chip select
- Reset programmable data port size for $\overline{CS}$[0]
- Programmable data port size for each chip select
- Address suppression during burst mode operations
- Synchronous burst mode support for burst flash devices
- Programmable wait-state generator for each chip select
- Supports big endian and little endian modes of operation

2.1 EIM Interface Signals

The EIM interface signals provide communication and control pathways between external devices and the i.MX processor.

The Table 1 summarizes each of these signals and their use. This document covers the following adjustable control signals: $\overline{CS}$[5:0], $\overline{EB}$[3:0], $\overline{OE}$, and R/$\overline{W}$, where the signals BCLK, $\overline{LBA}$, and $\overline{ECB}$ are specific to the burst and page style interfaces and will not be covered here. However, both BCLK and $\overline{LBA}$ are shown in the example waveforms for illustrative purposes. For more information on these signals please refer to the EIM section of the i.MX reference manual.

Table 1. EIM Interface Signals

i.MX EIM Pin Name	Function	Direction
D[31:0]	External 32-bit data bus.	Input/Output
A[24:0]	External address bus.	Output
$\overline{CS}$[5:0]	Active low external chip selects.	Output
DTACK	External input data acknowledge signal for $\overline{CS}$[5].	Input
$\overline{EB}$[3:0]	Active low external enable bytes signals. $\overline{EB}$[0] controls D[31:24], $\overline{EB}$[1] controls D[23:16], $\overline{EB}$[2] controls D[15:8], and $\overline{EB}$[3] controls D[7:0].	Output
OE	Active low output enable for external data bus.	Output
R/$\overline{W}$	Indicates whether external access is a read (high) or write (low) cycle. The assertion timing of this signal for write accesses is not configurable. Though it can be connected to the write enable of memories and other devices, for those devices that require any timing delay of the write enable assertion/de-assertion times, the user may use one the of EB[3:0] signals as their timing may be affected by the WEA and WEN bit settings (see Section 2.2, “i.MX EIM Register Overview.”)	Output

Table 1. EIM Interface Signals (continued)

i.MX EIM Pin Name	Function	Direction
BCLK	Clock for external synchronous memories (such as burst flash). May be programmed to run continuously as a reference clock.	Output
LBA	Active low signal sent to flash device causing the external device to latch the address.	Output
ECB	Input signal identifies when to end an external burst access (as in the case for burst flash).	Input

In this document, some signals may be denoted differently in text then in the example waveforms. For example, the EIM read/write signal, R/$\overline{W}$, is denoted as R/$\overline{W}$ in the text, but in the waveform examples, it may be denoted simply as RW. In other instances, the EIM enable byte signals, $\overline{EB}$[3:0], may simply be referred to as $\overline{EB}$, or in the case of the example waveforms, the enable byte is denoted as EB3 for simplicity.

2.2 i.MX EIM Register Overview

The EIM module includes thirteen user-accessible 32-bit registers. There is a common register called the EIM Configuration Register that contains control bits that configure the EIM for certain operation modes. The other twelve registers are pairs of control registers for each chip select. The layout of the control register is slightly different for the $\overline{CS}$[0] register output because $\overline{CS}$[0] does not support the programmable output function Pin Assert (PA), bit 1. Also, the DSIZ the bits of $\overline{CS}$[0] register are configurable upon reset, since $\overline{CS}$[0] is a bootable chip select. The settings of these DSIZ bits are determined by the setting of the BOOT[3:0] signals on reset. Refer to the i.MX reference manual for more details. These registers are accessible only in supervisor mode with word (32-bit) reads and writes.

The 64 bits of control are divided into two registers, Chip Select Upper Control Register and Chip Select Lower Control Register.

- Bits [63:32] are located in Chip Select Upper Control Register.
- Bits [31:0] are located in Chip Select Lower Control Register.

Though the reference manual provides these chip select control register bit definitions, this document attempts to provide more detail to these bit settings along with references to the external waveforms given later in the document. This document concentrates solely on the asynchronous bit timings, specifically the following bit settings: CNC (bits 47 and 46), WSC (bits 45 through 40), WWS (bits 38 through 36), EDC (bits 35 through 32), OEA (bits 31 through 28), OEN (bits 27 through 24), WEA (bits 23 through 20), WEN (bits 19 through 16), and CSA (bits 15 through 12). The bit settings not covered in detail in this document are related to the synchronous and page mode timings, specifically the following bits: BCD, BCS, PSZ, PME, SYNC, and DOL, although a description of these bits is provided in Table 1.

CS0U	Chip Select 0 Upper Control Register	0x00220000
CS1U	Chip Select 1 Upper Control Register	0x00220008
CS2U	Chip Select 2 Upper Control Register	0x00220010
CS3U	Chip Select 3 Upper Control Register	0x00220018
CS4U	Chip Select 4 Upper Control Register	0x00220020
CS5U	Chip Select 5 Upper Control Register	0x00220028

BIT	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
	DTACK_SEL[1]		BCD		BCS				PSZ		PME	SYNC	DOL			
TYPE	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
CS0U	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CS1–5U	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESET	0x0000 (CS0U) 0X0000 (CS1–5U)															

BIT	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
	CNC		WSC							WWS			EDC			
TYPE	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw
CS0U	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0
CS1–5U	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESET	0x3E00 (CS0U) 0x0000 (CS1–5U)															

[1]—Bit 63 of CS5U register is defined as DTACK_SEL. Bit 63 is reserved for CS0U, CS1U, CS2U, CS3U, CS4U.

CS0L	Chip Select 0 Lower Control Register	0x00220004
CS1L	Chip Select 1 Lower Control Register	0x0022000C
CS2L	Chip Select 2 Lower Control Register	0x00220014
CS3L	Chip Select 3 Lower Control Register	0x0022001C
CS4L	Chip Select 4 Lower Control Register	0x00220024
CS5L	Chip Select 5 Lower Control Register	0x0022002C

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OEA				OEN				WEA				WEN			
TYPE	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
CS0L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CS1–5L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESET	0x0000 (CS0L) 0x0000 (CS1–5L)															

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CSA				EBC	DSZ				SP		WP			PA[2]	CSEN
TYPE	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	r	rw	r	r	rw	rw
CS0L	0	0	0	0	1	*	*	*	0	0	0	0	0	0	0	1
CS1–5L	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
RESET	0x0*01[1] (CS0L) 0x0802 (CS1–5L)															

[1]—The DSIZ bits are configurable upon reset, dependent upon the BOOT[3:0] signal settings.
[2]—PA for $\overline{CS}$[1] to $\overline{CS}$[5] only, and “rw”. Reserved for $\overline{CS}$[0] (read only).

Table 2. Chip Select Control Registers Description

Name	Description	Settings
Reserved/ **DTACK_ SEL** Bit 63	**Reserved**—This bit is reserved and should read 0 for CS0–CS4. **DTACK_SEL**—This bit is used to select the functionality of the $\overline{\text{DTACK}}$ input signal for $\overline{\text{CS}}$[5]. To select the $\overline{\text{DTACK}}$ functionality on $\overline{\text{CS}}$[5], the WSC bits for $\overline{\text{CS}}$[5] must be set to 111111. **Note:** Due to current chip errata, DTACK_SEL can only be set to 1 for Compact Flash/PCMCIA functionality and requires the use of an external D flip-flop or other mechanism to extend the OE negation (assertion) time until the $\overline{\text{CS}}$[5] cycle is completed. Refer to the latest chip errata found at *www.freescale.com/imx*	Reserved for CS0–CS4 CS5: 0 = Reserved 1 = Compact Flash/PCMCIA wait function
Reserved Bit 62	Reserved—This bit is reserved and should read 0.	
BCD Bits 61–60	**Burst Clock Divisor**—Contains the value used to program the burst clock divisor and is used for synchronous (burst) style interfaces. Refer to the i.MX reference manual for more information on the burst clock divisors. When the **BCM** bit is set (BCM = 1) in the EIM configuration register, **BCD** is ignored. **BCD** is cleared by a hardware reset.	00 = Divisor is 1 01 = Divisor is 2 10 = Divisor is 3 11 = Divisor is 4
BCS Bits 59–56	**Burst Clock Start**—Determines the number of half cycles after $\overline{\text{LBA}}$ assertion before the first rising edge of BCLK is seen. A value of 0 results in a half clock delay, not an immediate assertion. This is used in conjunction with synchronous (burst) style interfaces. When the **BCM** bit is set (**BCM** = 1) in the WEIM configuration register, this overrides the **BCS** bits. **BCS** is cleared by a hardware reset.	0000 = 1 half cycle before BCLK 0001 = 2 half cycles before BCLK ... 1111 = 16 half cycles before BCLK
PSZ Bits 55–54	**Page Size**—Indicates the number of words (where “word” is defined by the port size or DSIZ bits) in a page in memory. This ensures that the WEIM does not burst pass a page boundary when the **PME** bit is set. This is used in conjunction with page-mode style interfaces. **PSZ** is cleared by a hardware reset.	00 = 4 words in a page 01 = 8 words in a page 10 = 16 words in a page 11 = 32 words in a page
PME Bit 53	**Page Mode Emulation**—Enables/Disables page mode emulation in burst mode. When **PME** is set, the external address asserts for each piece of data requested. Additionally, the $\overline{\text{LBA}}$ and BCLK signals behave as they do when an asynchronous access is performed. This is used in conjunction with page-mode style interfaces. **PME** is cleared by a hardware reset.	0 = Disables page mode emulation 1 = Enables page mode emulation
SYNC Bit 52	**Synchronous Burst Mode Enable**—Enables/Disables synchronous burst mode. When enabled, the EIM is capable of interfacing to burstable (synchronous) flash devices through additional burst control signals: BCLK, $\overline{\text{LBA}}$, and $\overline{\text{ECB}}$. The sequencing of these additional I/Os is controlled by other EIM configuration register bit settings as defined below. This is used in conjunction with synchronous (burst) style interfaces. **SYNC** is cleared by a hardware reset.	0 = Disables synchronous burst mode 1 = Enables synchronous burst mode

Table 2. Chip Select Control Registers Description (continued)

Name	Description	Settings
DOL Bits 51–48	**Data Output Length**—Specifies the expected number of system clock (HCLK) cycles required for burst read data to be valid on the data bus before it is latched by the EIM. The reset value specifies that burst data is held for a minimum of two system clock periods. As system clock frequencies increase, it may become necessary to delay sampling the data for multiple system clock periods in order to meet burst flash max frequency specifications and/or EIM data setup time requirements. **DOL** has no effect on EIM data latching when SYNC = 0. This is used in conjunction with synchronous (burst) style interfaces. **DOL** is cleared by a hardware reset.	0000 = 2 system clock delay 0001 = 2 system clock delay 0010 = 3 system clock delay 0011 = 4 system clock delay ... 1111 = 16 system clock delay
CNC Bits 47–46	**Chip Select Negation Clock Cycles**—Specifies the minimum number of system clock (HCLK) cycles a chip select must remain de-asserted after it is de-asserted. The **CNC** will only affect the chip select de-assertion once the chip select has de-asserted, in other words, for external back-to-back accesses where the chip select does not de-assert (in instances where it stays asserted), **CNC** has no affect. An example of how the **CNC** bit setting affects the chip select de-assertion time can be seen in Figure 16, Figure 17, and Figure 18. **CNC** has no effect on write accesses when any **CSA** bit is set. **CNC** is cleared by a hardware reset.	00 = Minimum de-assertion is 0 clock cycle 01 = Minimum de-assertion is 1 clock cycle 10 = Minimum de-assertion is 2 clock cycles 11 = Minimum de-assertion is 3 clock cycles
WSC Bits 45–40	**Wait State Control**— For **SYNC** = 0: **WSC** programs the number of wait-states for an access to the external device connected to the chip select. When the WWS (Write Wait State) bit settings are cleared, setting: **WSC** = 000000 results in 2 system clock (HCLK) transfers **WSC** = 000001 results in 2 system clock (HCLK) transfers **WSC** = 001110 results in 15 system clock (HCLK) transfers **WSC** = 111110 results in 63 system clock (HCLK) transfers **WSC** = 111111 is not available (reserved) for $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$, but it is available (the external $\overline{DTACK}$) for $\overline{CS5}$. As can also be seen from the external waveform diagrams in Section 3, “EIM External Bus Asynchronous Waveform Examples,” the **WSC** setting also dictates how many system clock (HCLK) cycles an address is held on the external address bus. This is best seen on those waveforms that depict back-to-back accesses, rather than for single external accesses, where the address will normally be held on the address bus after the transaction has completed when there is no immediate external transaction that follows. For **SYNC** = 1: **WSC** programs the number of system clock cycles required for the initial access of a burst sequence initiated by the EIM to an external burst device. Refer to the i.MX reference manual for more details. **WSC** is set to 111110 by a hardware reset for $\overline{CS0}$. **WSC** is cleared by a hardware reset for $\overline{CS1}$–$\overline{CS5}$. **Note: WSC** bits should be configured to more than one wait states. The i.MX does not support zero wait state (1 clock cycle) accesses.	000000 = 1 wait state delay (2 system clock (HCLK) cycle transfers) 000001 = 1 wait state delay (2 system clock (HCLK) cycle transfers) 000002 = 2 wait state delay (3 system clock (HCLK) cycle transfers) 000003 = 3 wait state delay (4 system clock (HCLK) cycle transfers) ... 111110 = 62 wait state delay (63 system clock (HCLK) cycle transfers) 111111 = not available (reserved) for $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$, but it is available (the external $\overline{DTACK}$) for $\overline{CS5}$ **Note:** Depending on the WWS setting, more wait states may be added for write cycles. Refer to the WWS bit setting definition for more details.

Table 2. Chip Select Control Registers Description (continued)

Name	Description	Settings
Reserved Bit 39	Reserved—This bit is reserved and should read 0.	
WWS Bits 38–36	**Write Wait State**—Determines whether additional wait-states are required for write cycles. This is useful for writing to memories that require additional data setup time. This setting basically adds wait states to what is programmed in the WSC setting for write access. An example of how the **WWS** bit setting affects write cycle timing can be seen in Figure 26, Figure 27, and Figure 28. **WWS** is cleared by a hardware reset.	
EDC Bits 35–32	**Extra Dead Cycles**—Determines whether idle cycles (HCLK cycles) are inserted after a read cycle for back-to-back external transfers to eliminate data bus contention. This is useful for slow memory and peripherals that use long $\overline{CS}$ or $\overline{OE}$ to output data three-state times. Idle cycles are not inserted for back-to-back external reads from the same chip select. In other words, idle cycles are only inserted for back-to-back transactions from separate chip selects. An example of how the **EDC** bit setting affects the idle cycle timing between chip select accesses can be seen in Figure 22, Figure 23, Figure 24, and Figure 25. **EDC** is cleared by a hardware reset.	0000 = 0 Idle (HCLK) Cycles Inserted between the end of a read from one chip select to the start of an access on another chip select 0001 = 1 Idle (HCLK) Cycle Inserted between the end of a read from one chip select to the start of an access on another chip select ... 1111 = 15 Idle (HCLK) Cycles Inserted between the end of a read from one chip select to the start of an access on another chip select
OEA Bits 31–28	**$\overline{OE}$ Assert**—Determines when $\overline{OE}$ is asserted during read cycles. For **SYNC** = 0: **OEA** determines the number of half clocks (half HCLK cycles) before $\overline{OE}$ asserts during a read cycle. The $\overline{OE}$ assertion time is referenced from when the read address is placed on the address bus (it can also be referenced from when chip select asserts). See the **OEA** bit settings for more details. Also, examples of how the **OEA** bit setting affects the $\overline{OE}$ assertion time during read accesses can be seen in Figure 4, Figure 5, Figure 6, Figure 31, and Figure 32. For **SYNC** = 1: After the initial burst access, $\overline{OE}$ is asserted continuously for subsequent burst accesses, and is not affected by **OEA** (see burst read timing diagrams for more detail). The behavior of $\overline{OE}$ on the initial burst access is the same as when **SYNC** = 0. When the **EBC** bit in the corresponding register is clear, the $\overline{EB}$[3:0] outputs are similarly affected. **OEA** does not affect the cycle length. **OEA** is cleared by a hardware reset.	0000 = $\overline{OE}$ is asserted 0 half clocks (HCLK cycles) after the assertion of chip select (or after the address is placed on the bus) 0001 = $\overline{OE}$ is asserted 1 half clock (HCLK cycles) after the assertion of chip select (or after the address is placed on the bus) ... 1111 = $\overline{OE}$ is asserted 15 half clocks (HCLK cycles) after the assertion of chip select (or after the address is placed on the bus)

Table 2. Chip Select Control Registers Description (continued)

Name	Description	Settings
OEN Bits 27–24	**$\overline{\text{OE}}$ De-assert**—Determines when $\overline{\text{OE}}$ is de-asserted during a read cycle. See the **OEN** bit settings for more details. Also, examples of how the **OEN** bit setting affects the $\overline{\text{OE}}$ de-assertion time during read accesses can be seen in Figure 7, Figure 8, Figure 9, Figure 31, and Figure 32. When **EBC** in the corresponding register is clear, the $\overline{\text{EB}}$[3:0] outputs are similarly affected. Setting the SYNC bit (SYNC = 1) overrides **OEN** and $\overline{\text{OE}}$ negates at the end of a read access and no sooner. **OEN** does not affect the cycle length. **OEN** is cleared by a hardware reset. **Note:** Programming the OEA and OEN bits such that the total assertion time of $\overline{\text{OE}}$ is one half HCLK cycle is not allowed, and will result in no assertion of the $\overline{\text{OE}}$ signal.	0000 = $\overline{\text{OE}}$ is de-asserted 0 half clocks (HCLK cycles) before end of access (before the chip select is de-asserted) 0001 = $\overline{\text{OE}}$ is de-asserted 1 half clock (HCLK cycles) before end of access (before the chip select is de-asserted) ... 1111 = $\overline{\text{OE}}$ is de-asserted 15 half clocks (HCLK cycles) before end of access (before the chip select is de-asserted)
WEA Bits 23–20	**$\overline{\text{EB}}$[3:0] Assert**—Determines when $\overline{\text{EB}}$[3:0] is asserted during write cycles. This is useful to meet data setup time requirements for slow memories. **WEA** determines the number of half clocks (half HCLK cycles) before $\overline{\text{EB}}$[3:0] asserts during a write cycle. The $\overline{\text{EB}}$[3:0] assertion time is referenced from when the write address is placed on the address bus or when the R/$\overline{\text{W}}$ signal asserts (it can also be referenced from when chip select asserts, however, in the case of writes, the chip select assertion time may also be affected by the CSA bit setting). See the **WEA** bit settings for more details. Also, examples of how the **WEA** bit setting affects the $\overline{\text{EB}}$[3:0] assertion time during write accesses can be seen in Figure 10, Figure 11, Figure 12, Figure 27, Figure 28, Figure 29, and Figure 30. **WEA** does not affect the cycle length. **WEA** is cleared by a hardware reset.	0000 = $\overline{\text{EB}}$[3:0] is asserted 0 half clocks (HCLK cycles) after the address is placed on the bus 0001 = $\overline{\text{EB}}$[3:0] is asserted 1 half clock (HCLK cycles) after the address is placed on the bus ... 1111 = $\overline{\text{EB}}$[3:0] is asserted 15 half clocks (HCLK cycles) after the address is placed on the bus
WEN Bits 19–16	**$\overline{\text{EB}}$[3:0] De-assertion During Write**—Determines when $\overline{\text{EB}}$[3:0] outputs are de-asserted during a write cycle. This is useful to meet data hold time requirements for slow memories. See the **WEN** bit settings for more details. Also, examples of how the **WEN** bit setting affects the $\overline{\text{EB}}$[3:0] de-assertion time during write accesses can be seen in Figure 13, Figure 14, Figure 15, Figure 28, Figure 29 and Figure 30. **WEN** does not affect the cycle length. **WEN** is cleared by a hardware reset. **Note:** Programming the WEA and WEN bits such that the total assertion time of $\overline{\text{EB}}$[3:0] is one half HCLK cycle is not allowed, and will result in no assertion of the $\overline{\text{EB}}$[3:0] signal	0000 = $\overline{\text{EB}}$[3:0] is de-asserted 0 half clocks (HCLK cycles) before end of access (or before the de-assertion of R/$\overline{\text{W}}$) 0001 = $\overline{\text{EB}}$[3:0] is de-asserted 1 half clock (HCLK cycles) before end of access (or before the de-assertion of R/$\overline{\text{W}}$) ... 1111 = $\overline{\text{EB}}$[3:0] is de-asserted 15 half clocks (HCLK cycles) before end of access (or before the de-assertion of R/$\overline{\text{W}}$)

Table 2. Chip Select Control Registers Description (continued)

Name	Description	Settings
CSA Bits 15–12	**Chip Select Assert**—Determines when the chip select is asserted and de-asserted for devices that require additional address setup time and additional address/data hold times. **CSA** affects only external writes, and is ignored on external reads. The chip select assertion/de-assertion times may be referenced from the assertion and de-assertion of the R/$\overline{W}$ signal or for back-to-back external writes, the chip select assertion/de-assertion time may be referenced to when the write address is placed and removed from the external address bus. See the **CSA** bit settings for more details. Also, examples of how the **CSA** bit setting affects the chip select assertion and de-assertion time during write accesses can be seen in Figure 19, Figure 20, Figure 21, and Figure 33. **CSA** pre-empts the CNC bit setting. **CSA** does not affect the cycle length. **CSA** is cleared by a hardware reset.	0000 = Asserts 0 HCLK cycles after address is placed on bus and de-asserts 0 HCLK cycles before end of access (or before address is removed from bus for back-to-back accesses) 0001 = Asserts 1 HCLK cycles after address is placed on bus and de-asserts 1 HCLK cycles before end of access (or before address is removed from bus for back-to-back accesses) ... 1111 = Asserts 15 HCLK cycles after address is placed on bus and de-asserts 15 HCLK cycles before end of access (or before address is removed from bus for back-to-back accesses)
EBC Bit 11	**Enable Byte Control**—Indicates the access types that assert the enable byte outputs ($\overline{EB}$[3:0]). **EBC** is set by a hardware reset.	0 = Both read and write accesses assert the $\overline{EB}$[3:0] outputs, thus configuring the access as byte enables 1 = Only write accesses assert the $\overline{EB}$[3:0] outputs, thus configuring the access as byte write enables; the $\overline{EB}$[3:0] outputs are configured as byte write enables for accesses to dual x16 or quad x8 memories
DSZ Bits 10–8	**Data Port Size**—Defines the width of the external device's data port as shown in the table, **DSZ** Bit Encoding, to the right. At hardware reset, the value of **DSZ** is 101 for $\overline{CS1}$– $\overline{CS5}$. For $\overline{CS0}$, **DSZ** is based on the value of the external BOOT[3:0] signals.	000 = 8-bit port, resides on D[31:24] pins 001 = 8-bit port, resides on D[23:16] pins 010 = 8-bit port, resides on D[15:8] pins 011 = 8-bit port, resides on D[7:0] pins 100 = 16-bit port, resides on D[31:16] pins 101 = 16-bit port, resides on D[15:0] pins 11x = 32-bit port
Reserved Bit 7	Reserved—This bit is reserved and should read 0.	
SP Bit 6	**Supervisor Protect**—Prevents accesses to the address range defined by the corresponding chip select when the access is attempted in the User mode of ARM920T core operation. **SP** is cleared by a hardware reset.	0 = User mode accesses are allowed in the range of chip select 1 = User mode accesses are prohibited; attempts to access an address mapped by this chip select in User mode results in a $\overline{TEA}$ to the ARM920T core and no assertion of the chip select output
Reserved Bit 5	Reserved—This bit is reserved and should read 0.	
WP Bit 4	**Write Protect**—Prevents writes to the address range defined by the corresponding chip select. **WP** is cleared by a hardware reset.	0 = Writes are allowed in the range of chip select 1 = Writes are prohibited; attempts to write to an address mapped by this chip select result in a $\overline{TEA}$ to the ARM920T core and no assertion of the chip select output

Table 2. Chip Select Control Registers Description (continued)

Name	Description	Settings
Reserved Bits 3–2	Reserved—These bits are reserved and should read 0.	
PA Bit 1	**Pin Assert—**Controls the chip select pin when it is operating as a programmable output pin (when the CSEN bit is clear). PA is not available (reserved) for CS0. PA is set by a hardware reset for CS1–CS5.	0 = Brings the chip select output to logic-low 1 = Brings the chip select output to logic-high
CSEN Bit 0	**Chip Select Enable**—Controls the operation of the chip select pin. Except for $\overline{CS0}$, **CSEN** is cleared by reset, disabling the chip select output pin. When enabled, the PA control bit is ignored. **CSEN** in the CS0 control register is set at reset to allow $\overline{CS0}$ to select from an external boot ROM. **CSEN** is set by a hardware reset for $\overline{CS0}$. **CSEN** is cleared by a hardware reset for $\overline{CS1}$–$\overline{CS5}$.	0 = Chip select function is disabled; attempts to access an address mapped by this chip select results in an error and no assertion of the chip select output When disabled, the pin is a general purpose output controlled by the value of PA control bit. When **CSEN** in the CS0 control register is clear, $\overline{CS0}$ is inactive. 1 = Chip select is enabled, and is asserted when presented with a valid AHB access.

Table 3. Chip Select Wait State and Burst Delay Encoding

WSC [5:0]	Number of Wait-States					
	WWS = 0		WWS = 1		WWS = 7	
	Read Access	Write Access	Read Access	Write Access	Read Access	Write Access
000000	1	1	1	1	1	7
000001	1	1	1	2	1	8
000010	2	2	2	3	2	9
000011	3	3	3	4	3	10
...	–	–	–	–	–	–
110111	55	55	55	56	55	62
111000	56	56	56	57	56	63
111001	57	57	57	58	57	63
111010	58	58	58	59	58	63
111011	59	59	59	60	59	63
111100	60	60	60	61	60	63
111101	61	61	61	62	61	63
111110	62	62	62	63	62	63
111111	Reserved or External DTACK	Reserved or External DTACK	Reserved or External DTACK	Reserved or External DTACK	Reserved or External DTACK	Reserved or External DTACK

Note: WSC = 111111 is not available (reserved) for $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$, but it is available (the external DTACK) for $\overline{CS5}$.

EIM	EIM Configuration Register												Addr 0x00220030			
BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0x0000															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														BCM		
TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	rw	r	r
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0x0000															

Table 4. EIM Configuration Register Description

Name	Description	Settings
Reserved Bits 31– 3	Reserved—These bits are reserved and should read 0.	
BCM Bit 2	**Burst Clock Mode**—Selects the burst clock mode of operation. BCM is cleared by a hardware reset.	0 = The burst clock runs only when accessing a chip select range with the SYNC bit set; when the burst clock is not running it remains in a logic 0 state; when the burst clock is running it is configured by the BCD and BCS bits in the chip select control register. 1 = The burst clock runs all the time (independent of chip select accesses). The burst clock (BCLK) runs at the same frequency as the system clock (HCLK).
Reserved Bits 1–0	Reserved—These bits are reserved and should read 0.	

2.3 Hardware Set-Up for Waveform Capture

The next section, Section 3, “EIM External Bus Asynchronous Waveform Examples,” provides several example waveforms captured on an HP16702A logic analyzer. The waveforms were generated using an i.MX chip along with an internal-use-only evaluation board (EVB), used mainly for silicon validation. The code used to generate the waveforms was stored in the i.MX1 internal RAM to minimize external bus transactions and to ensure that only the desired external bus transactions were captured (as opposed to inadvertently capturing instruction or data fetches). The code basically consists of setting up the EIM chip select control register and performing either a read or write operation. Each of the example waveforms provides the chip select control register settings.

3 EIM External Bus Asynchronous Waveform Examples

Figure 1 through Figure 33 timing diagrams show the EIM waveforms for different chip select control register bit settings for either read or write accesses. Each of the timings diagrams are actual waveforms captured on an HP16702A logic analyzer to illustrate how varying the bit settings affect the asynchronous timings of the EIM. In each waveform example, the BCM bit in the EIM Configuration Register is set, forcing the burst clock (BCLK) to run all the time, to help in analyzing the timing details of each waveform and to provide a point of reference. The burst clock (BCLK) follows the timing of the internal system clock (HCLK), in that the frequency of the system clock (HCLK) is mirrored on the external burst clock (BCLK) output. Also note that for illustrative purposes and to minimize cluttering the waveform examples, only one of the enable byte signals, $\overline{EB3}$, is shown as it asserts for 32-bit accesses and for 16-bit accesses when DSIZ is set for 101. Hence the choice of which data port D[31:16] or D[15:0] to use during 16-bit accesses is arbitrary, thus the data port D[15:0] was chosen as it would force the assertion of the enable byte signal $\overline{EB3}$. Finally, $\overline{CS}$[1] is used as the example chip select for most of the examples waveforms, however, all the chip selects should follow the same timing, thus the use of $\overline{CS}$[1] is completely arbitrary.

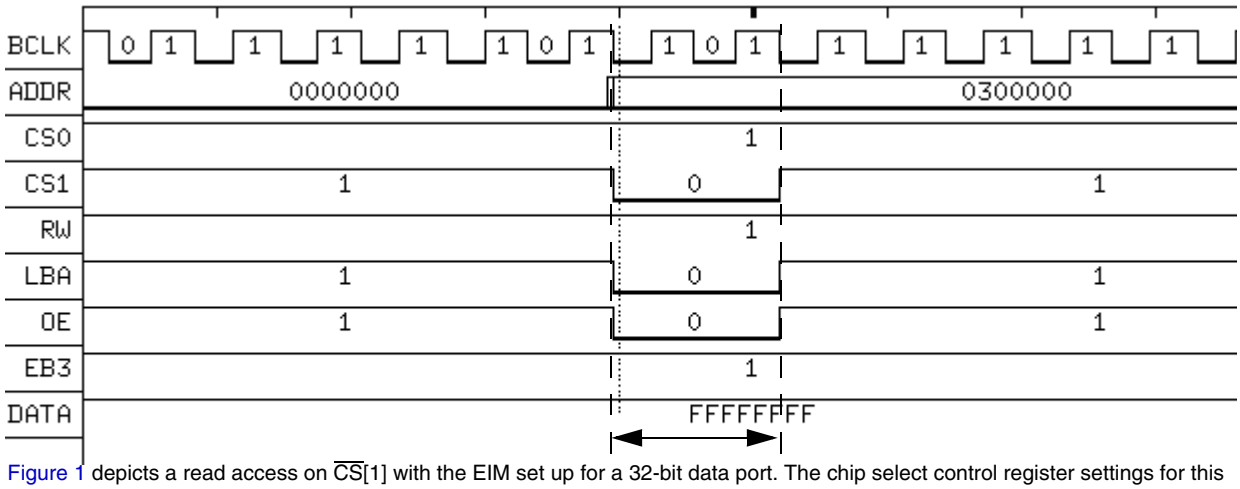

Figure 1 depicts a read access on $\overline{CS}$[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000100
CS1L = 0x00000E01
The Wait State Control (WCS) bits are set to 1 wait state, and as can be seen the in the diagram, the total access time is 2 clock cycles (from when the address is placed on the bus). Also in this example, the EBC bit is set indicating that the $\overline{EB}$ signal only asserts for write accesses.

Figure 1. WSC=1, EBC=1 (Read)

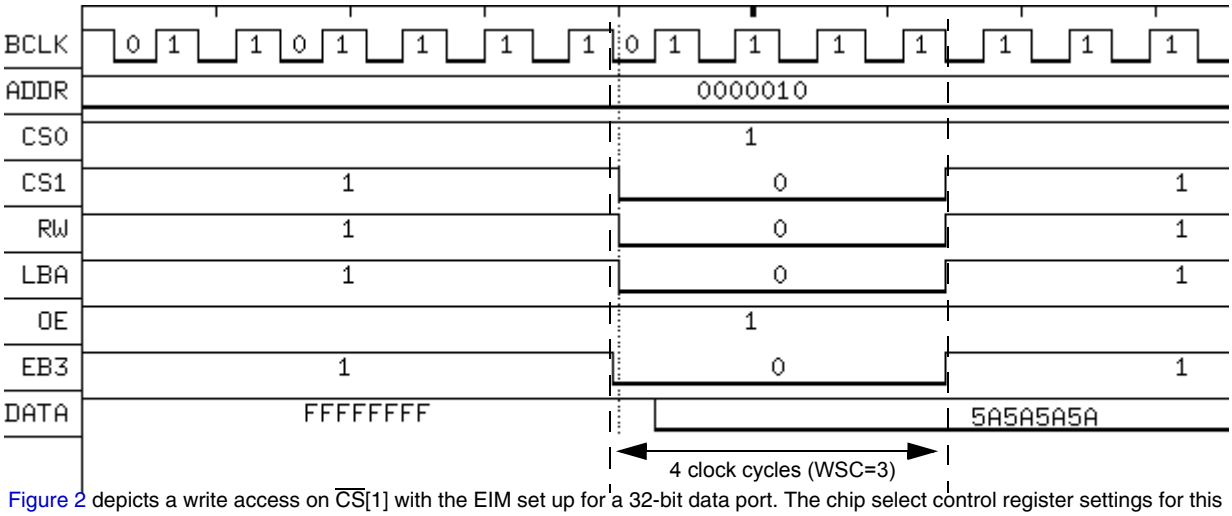

Figure 2 depicts a write access on $\overline{CS}$[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000300
CS1L = 0x00000E01
The Wait State Control (WCS) bits are set to 3 wait states, and as can be seen the in the diagram, the total access time is 4 clock cycles (from when the address is placed on the bus). Also in this example, the EBC bit is set indicating that the $\overline{EB}$ signal only

Figure 2. WSC=3, EBC=1 (Write)

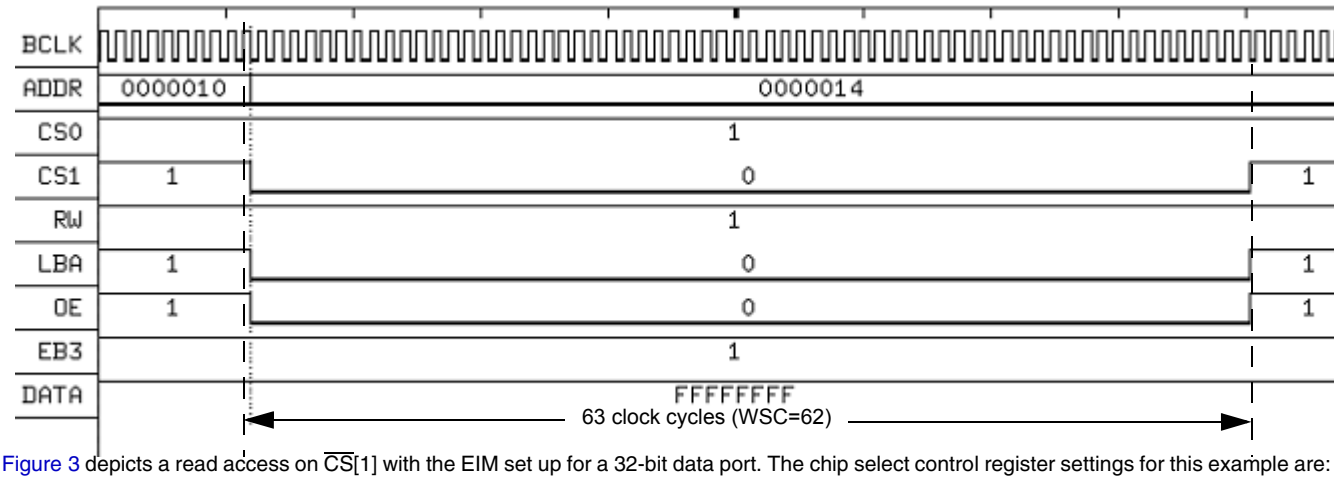

Figure 3 depicts a read access on $\overline{CS}$[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x0000FE00
CS1L = 0x00000E01
The Wait State Control (WCS) bits are set to 62 wait states, and as can be seen the in the diagram, the total access time is 63 clock cycles (from when the address is placed on the bus). Also in this example, the EBC bit is set indicating that the $\overline{EB}$ signal only asserts for write accesses.

Figure 3. WSC=62, EBC=1 (Read)

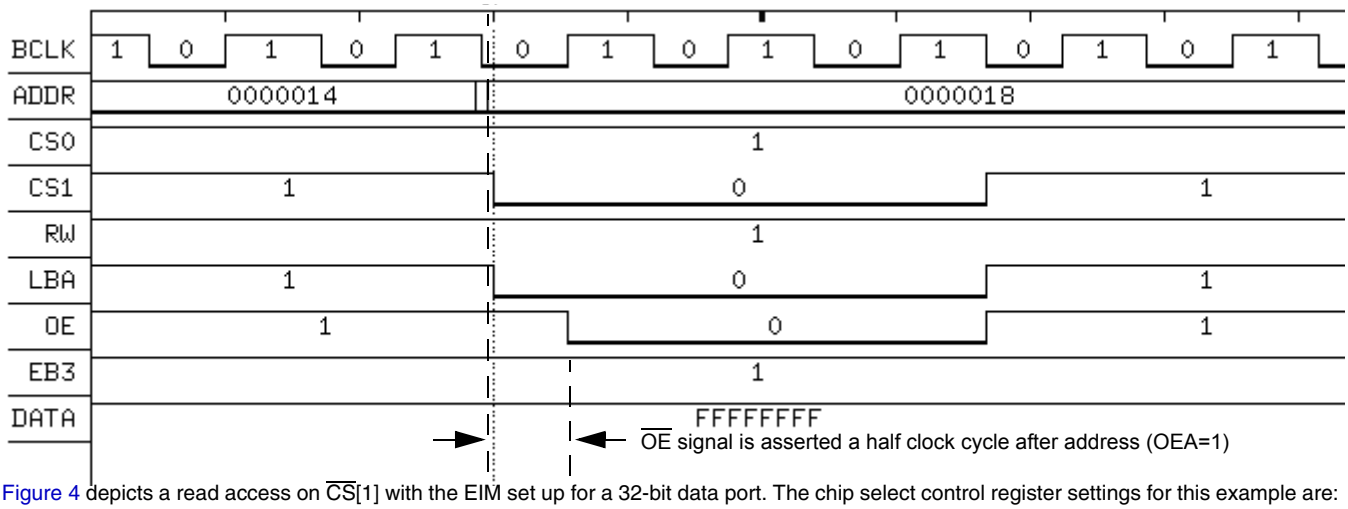

Figure 4 depicts a read access on $\overline{CS}$[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000200
CS1L = 0x10000E01
The Wait State Control (WCS) bits are set to 2 wait states and the OEA bits are set to 1, indicating a half clock cycle delay from when the address is placed on the bus to the assertion of the $\overline{OE}$ signal. Also in this example, the EBC bit is set indicating that the $\overline{EB}$ signal only asserts for write accesses.

Figure 4. WSC=2, OEA=1, EBC=1 (Read)

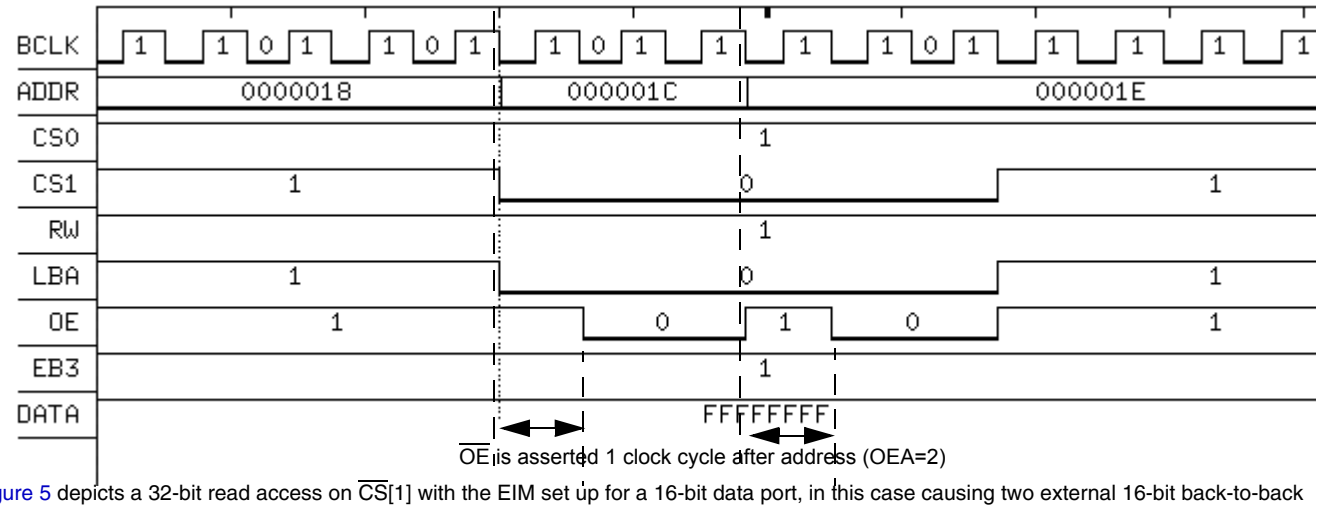

Figure 5 depicts a 32-bit read access on $\overline{CS}$[1] with the EIM set up for a 16-bit data port, in this case causing two external 16-bit back-to-back accesses. The chip select control register settings for this example are:
CS1U = 0x00000200
CS1L = 0x20000D01
The Wait State Control (WCS) bits are set to 2 wait states and the OEA bits are set to 2, indicating a 1 clock cycle delay (2 half clock cycles) from when the address is placed on the bus to the assertion of the $\overline{OE}$ signal. Also in this example, the EBC bit is set indicating that the $\overline{EB}$ signal only asserts for write accesses.

Figure 5. WSC=2, OEA=2, EBC=1, DSIZ= 101 (Read)

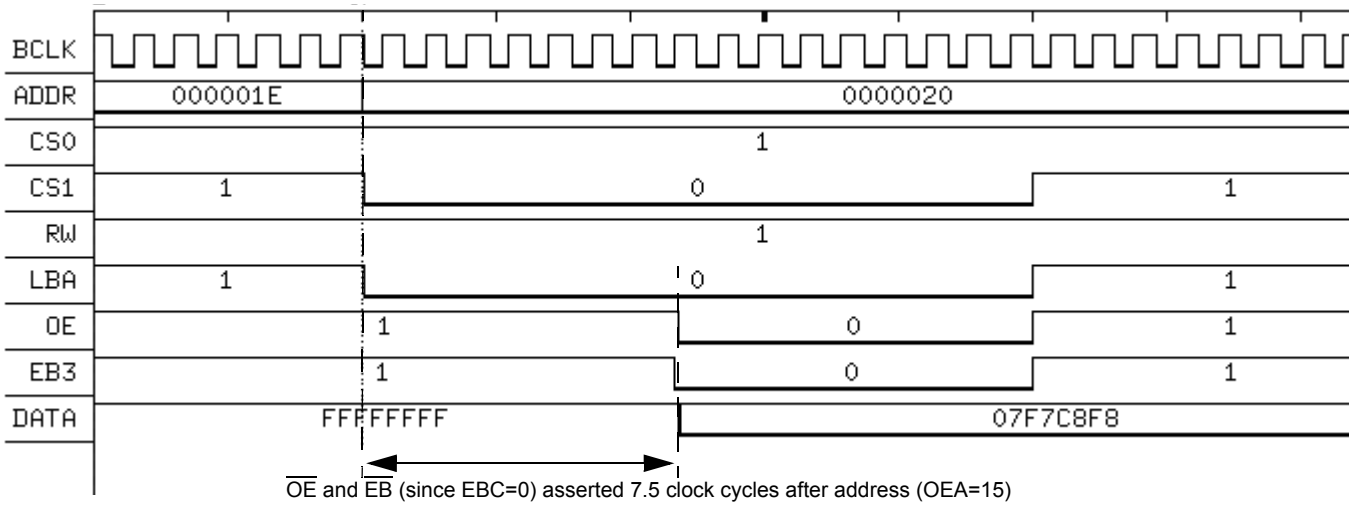

Figure 6 depicts a read access on CS[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000F00
CS1L = 0xF0000601
The Wait State Control (WCS) bits are set to 15 wait states and the OEA bits are set to 15, indicating a 7.5 clock cycle delay from when the address is placed on the bus to the assertion of the OE signal. Also in this example, the EBC bit is cleared indicating that the EB signal asserts for write and read accesses, as seen above.

Figure 6. WSC=15, OEA=15, EBC=0 (Read)

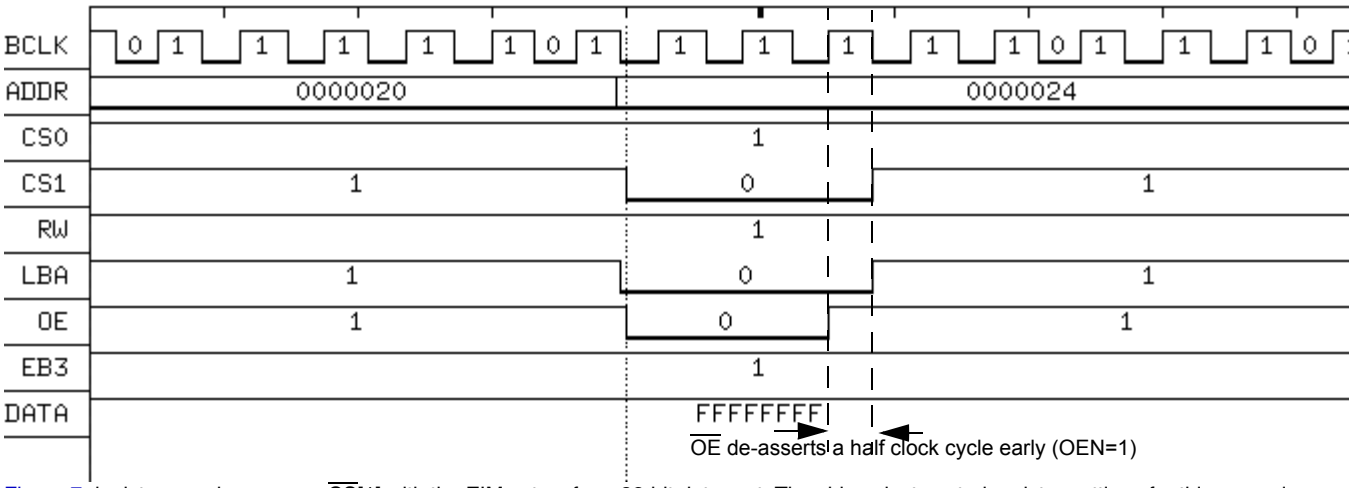

Figure 7 depicts a read access on CS[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000200
CS1L = 0x01000E01
The Wait State Control (WCS) bits are set to 2 wait states and the OEN bits are set to 1, indicating that the OE signal de-asserts a half clock cycle before the de-assertion of the chip select (or in the case of back-to-back read accesses, it will de-assert one half clock cycle before the associated read address is removed from the bus). Also in this example, the EBC bit is set indicating that the EB signal only asserts for write accesses.

Figure 7. WSC=2, OEN=1, EBC=1 (Read)

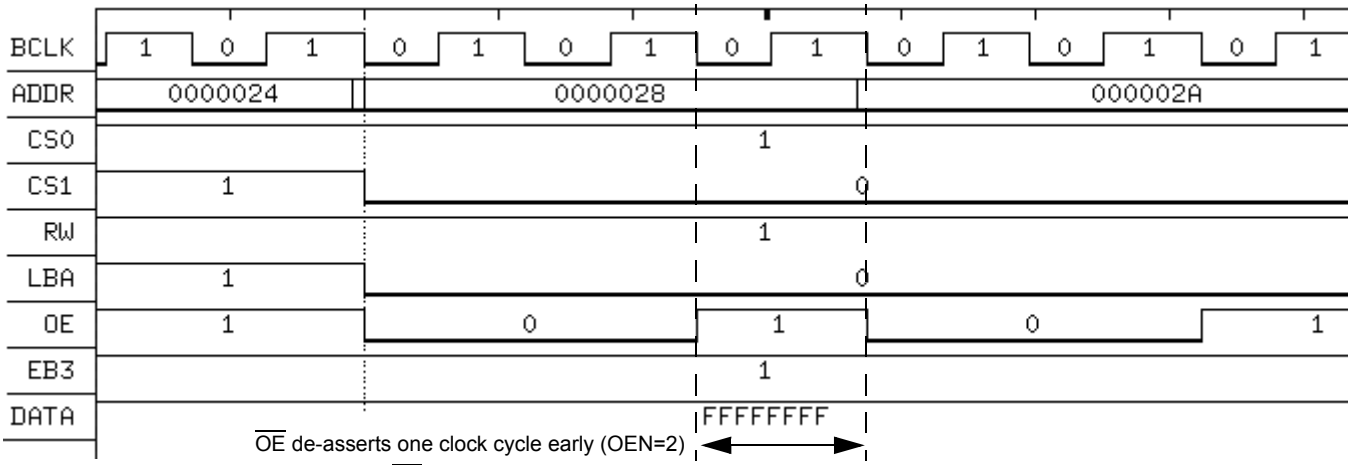

Figure 8 depicts a 32-bit read access on $\overline{CS}$[1] with the EIM set up for a 16-bit data port, in this case causing two external 16-bit back-to-back accesses. The chip select control register settings for this example are:
CS1U = 0x00000200
CS1L = 0x02000D01
The Wait State Control (WCS) bits are set to 2 wait states and the OEN bits are set to 2, indicating that the $\overline{OE}$ signal de-asserts a one clock cycle before the de-assertion of the chip select, or for back-to-back read accesses as seen here, it will de-assert one clock cycle before the associated read address is removed from the bus and before the placement of the next address. Also in this example, the EBC bit is set indicating that the $\overline{EB}$ signal only asserts for write accesses.

Figure 8. WSC=2, OEN=2, EBC=1, DSZ= 101 (Read)

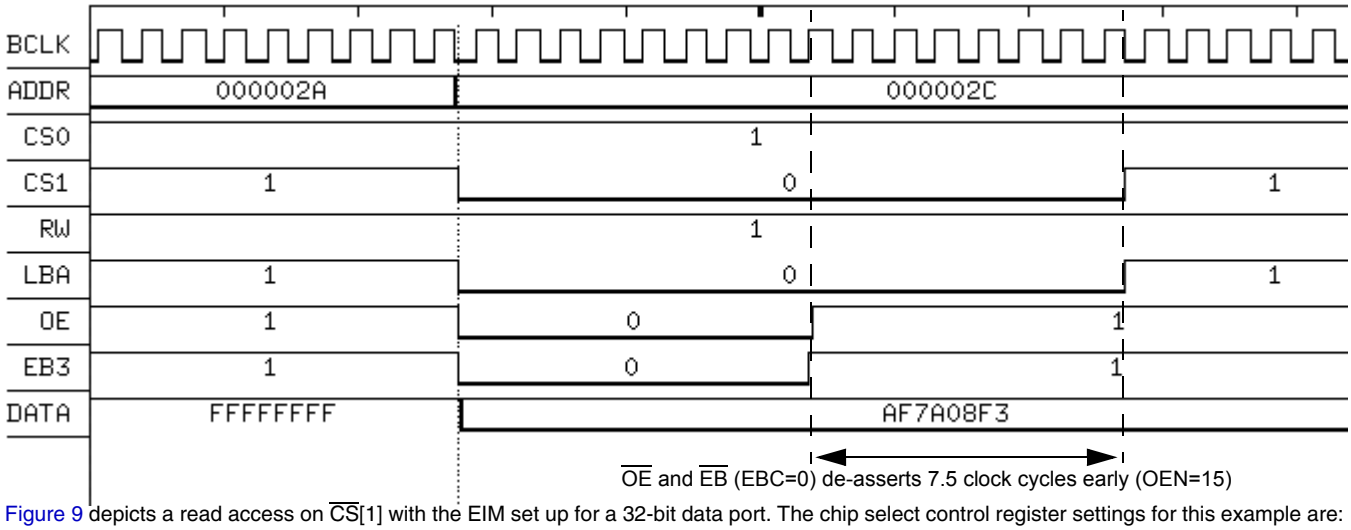

Figure 9 depicts a read access on $\overline{CS}$[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000F00
CS1L = 0x0F000601
The Wait State Control (WCS) bits are set to 15 wait states and the OEN bits are set to 15, indicating that the $\overline{OE}$ signal de-asserts a 7.5 clock cycles before the de-assertion of the chip select (or in the case of back-to-back read accesses, it will de-assert 7.5 clock cycles before the associated read address is removed from the bus). Also in this example, the EBC bit is cleared indicating that the $\overline{EB}$ signal asserts for write and read accesses.

Figure 9. WSC=15, OEN=15, EBC=0 (Read)

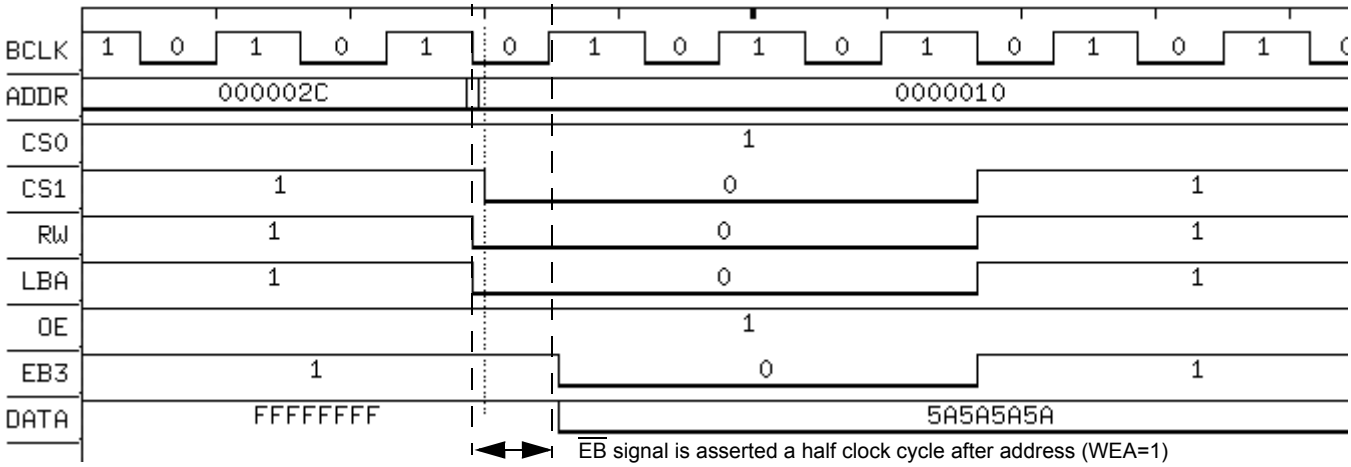

Figure 10 depicts a write access on CS[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000200
CS1L = 0x00100E01
The Wait State Control (WCS) bits are set to 2 wait states and the WEA bits are set to 1, indicating a half clock cycle delay from when the address is placed on the bus to the assertion of the EB signal. Also in this example, the EBC bit is set indicating that the EB signal only asserts for write accesses. Note in this example that the placement of the data onto the bus is coincidental with the assertion of the EB signal. For write cycles, due to the internal timings of the EIM, the data is normally placed on the bus a half clock cycle after the placement of the address, regardless of the WEA setting.

Figure 10. WSC=2, WEA=1, EBC=1 (Write)

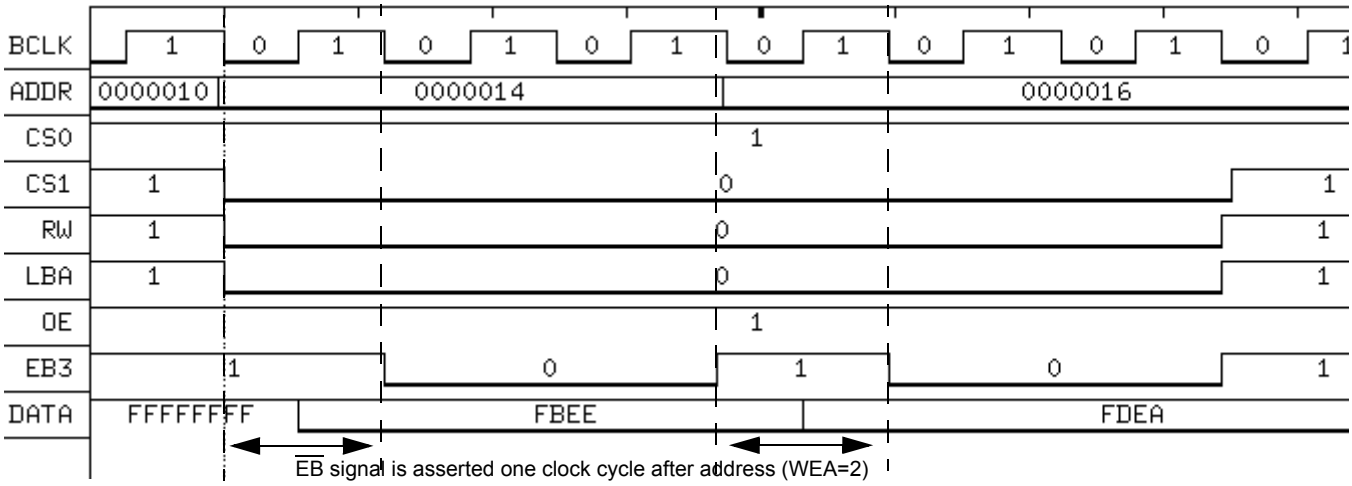

Figure 11 depicts a 32-bit write access on CS[1] with the EIM set up for a 16-bit data port, in this case causing two external 16-bit back-to-back accesses. The chip select control register settings for this example are:
CS1U = 0x00000200
CS1L = 0x00200D01
The Wait State Control (WCS) bits are set to 2 wait states and the WEA bits are set to 2, indicating a clock cycle delay from when the address is placed on the bus to the assertion of the EB signal. Also in this example, the EBC bit is set indicating that the EB signal only asserts for write accesses.

Figure 11. WSC=2, WEA=2, EBC=1, DSIZ= 101 (Write)

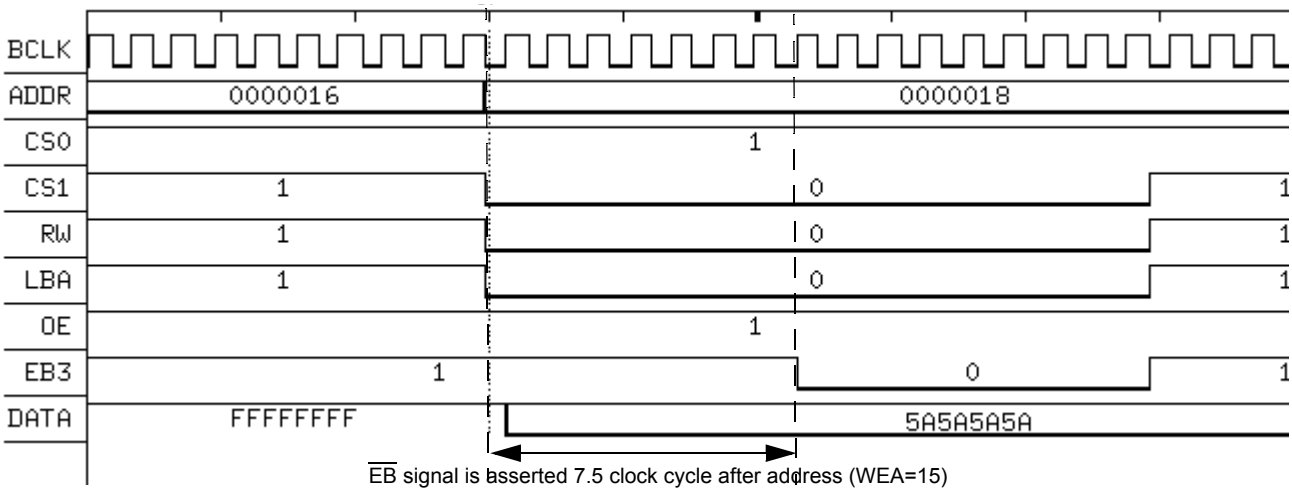

Figure 12 depicts a write access on CS[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000F00
CS1L = 0x00F00E01
The Wait State Control (WCS) bits are set to 15 wait states and the WEA bits are set to 15, indicating a 7.5 clock cycle delay from when the address is placed on the bus to the assertion of the EB signal. Also in this example, the EBC bit is set indicating that the EB signal only asserts for write accesses.

Figure 12. WSC=15, WEA=15, EBC=1 (Write)

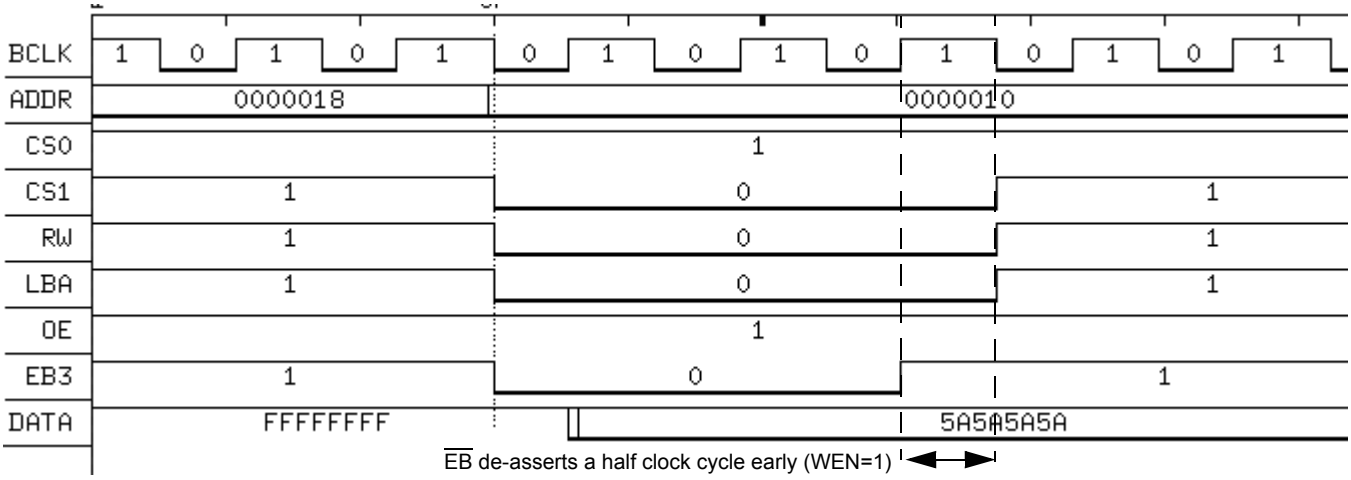

Figure 13 depicts a write access on CS[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000200
CS1L = 0x00010E01
The Wait State Control (WCS) bits are set to 2 wait states and the WEN bits are set to 1, indicating that the EB signal de-asserts a half clock cycle before the de-assertion of the chip select (or in the case of back-to-back write accesses, it will de-assert one half clock cycle before the associated write address is removed from the bus). Also in this example, the EBC bit is set indicating that the EB signal only asserts for write accesses.

Figure 13. WSC=2, WEN=1, EBC=1 (Write)

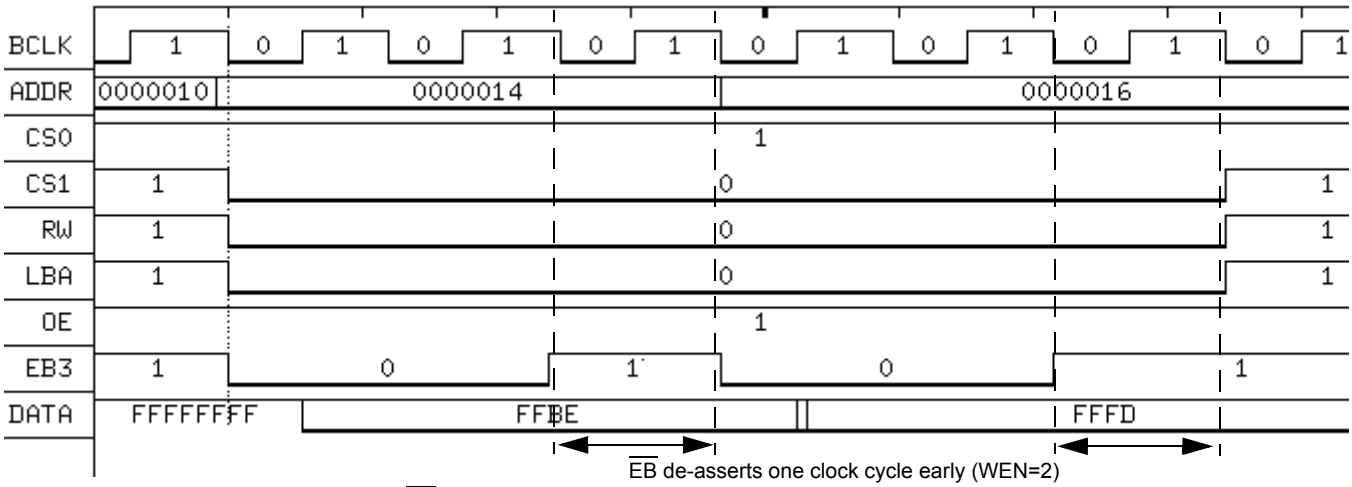

Figure 14 depicts a 32-bit write access on $\overline{CS}$[1] with the EIM set up for a 16-bit data port, in this case causing two external 16-bit back-to-back accesses. The chip select control register settings for this example are:
CS1U = 0x00000200
CS1L = 0x00020D01
The Wait State Control (WCS) bits are set to 2 wait states and the WEN bits are set to 2, indicating that the $\overline{EB}$ signal de-asserts a one clock cycle before the de-assertion of the chip select, or for back-to-back read accesses as seen here, it will de-assert one clock cycle before the associated write address is removed from the bus and before the placement of the next address. Also in this example, the EBC bit is set indicating that the $\overline{EB}$ signal only asserts for write accesses.

Figure 14. WSC=2, WEN=2, EBC=1, DSIZ= 101 (Write)

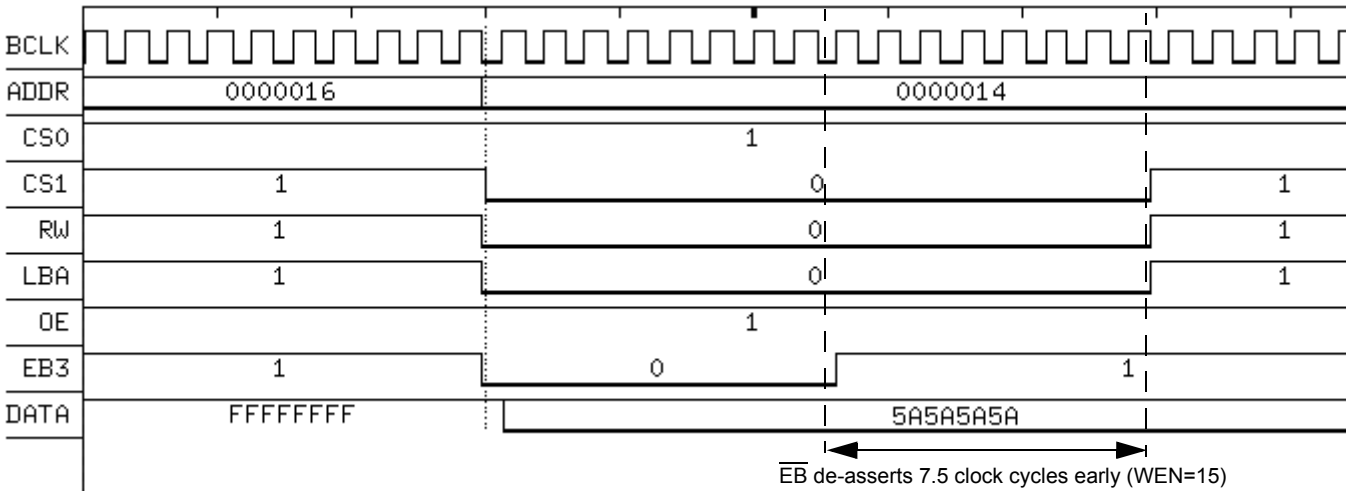

Figure 15 depicts a write access on $\overline{CS}$[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000F00
CS1L = 0x000F0E01
The Wait State Control (WCS) bits are set to 15 wait states and the WEN bits are set to 15, indicating that the $\overline{EB}$ signal de-asserts a 7.5 clock cycles before the de-assertion of the chip select (or in the case of back-to-back write accesses, it will de-assert 7.5 clock cycles before the associated write address is removed from the bus). Also in this example, the EBC bit is set indicating that the $\overline{EB}$ signal only asserts for write accesses.

Figure 15. WSC=15, WEN=15, EBC=1 (Write)

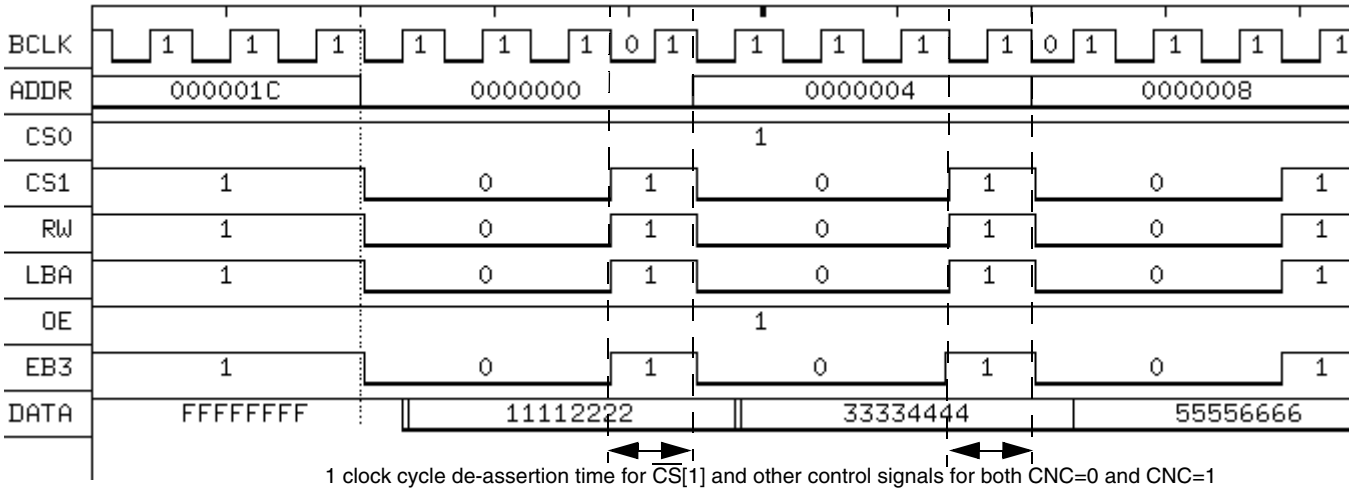

Figure 16 depicts several back-to-back write accesses on CS[1] with the EIM set up for a 32-bit data port. The back-to-back write accesses are achieved by issuing a Store Multiple command (STM). The chip select control register settings for this example are:
CS1U = 0x00000200
CS1L = 0x00000E01
The Wait State Control (WCS) bits are set to 2 and for this example, CNC is set to 0. This figure shows that even though CNC is set to 0, there is still a one clock cycle turn around time from one write cycle to another, due mainly to internal transactions between the EIM and the internal AHB bus. This can be seen above, where the chip select and other control signals are de-asserted for one clock cycle from one write to another. For a CNC setting of 1, this waveform would look the same. The following two example waveforms show the effect changing the CNC bits (to 2 and 3) have on the de-assertion time of the chip select and other control signals.

Figure 16. WSC=2, CNC=0, EBC=1 (Write)

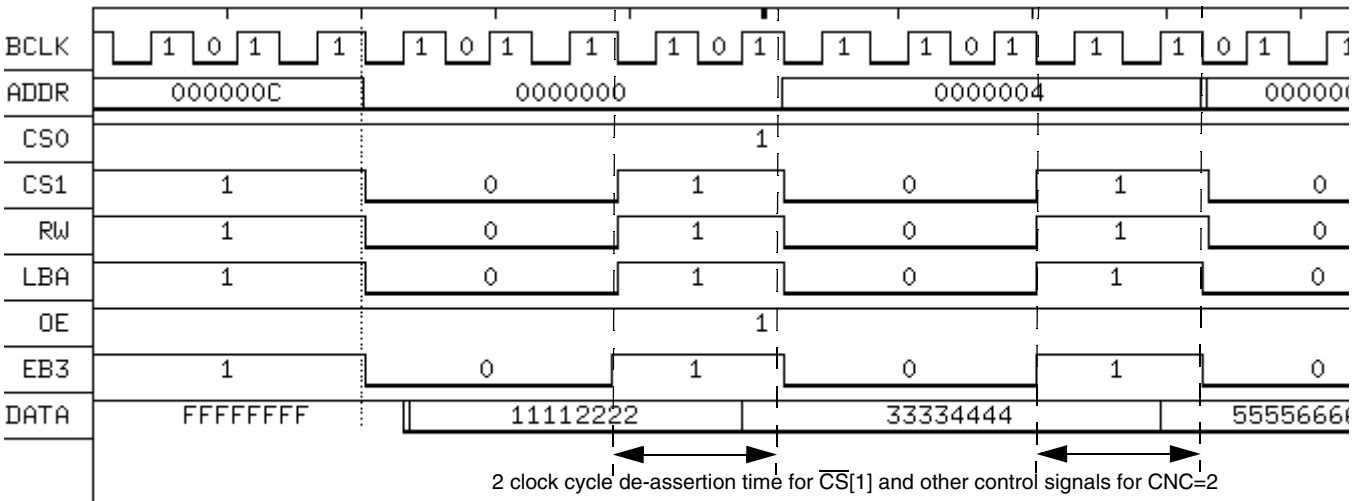

Figure 17 depicts several back-to-back write accesses on CS[1] with the EIM set up for a 32-bit data port. The back-to-back write accesses are achieved by issuing a Store Multiple command (STM). The chip select control register settings for this example are:
CS1U = 0x00008200
CS1L = 0x00000E01
The Wait State Control (WCS) bits are set to 2 and for this example, CNC is set to 2. This figure shows that with CNC set to 2, the de-assertion time for the chip select signal and other control signals is stretched out to 2 clock cycles.

Figure 17. WSC=2, CNC=2, EBC=1 (Write)

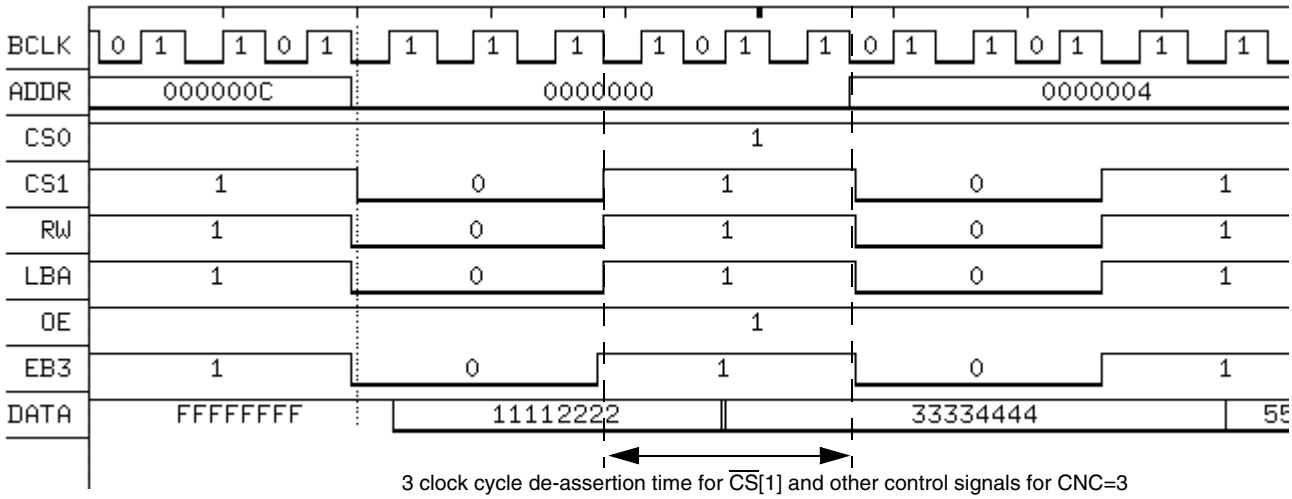

Figure 18 depicts several back-to-back write accesses on CS[1] with the EIM set up for a 32-bit data port. The back-to-back write accesses are achieved by issuing a Store Multiple command (STM). The chip select control register settings for this example are:
CS1U = 0x0000C200
CS1L = 0x00000E01
The Wait State Control (WCS) bits are set to 2 and for this example, CNC is set to 3. This figure shows that with CNC set to 3, the de-assertion time for the chip select signal and other control signals is stretched out to 3 clock cycles.

Figure 18. WSC=2, CNC=3, EBC=1 (Write)

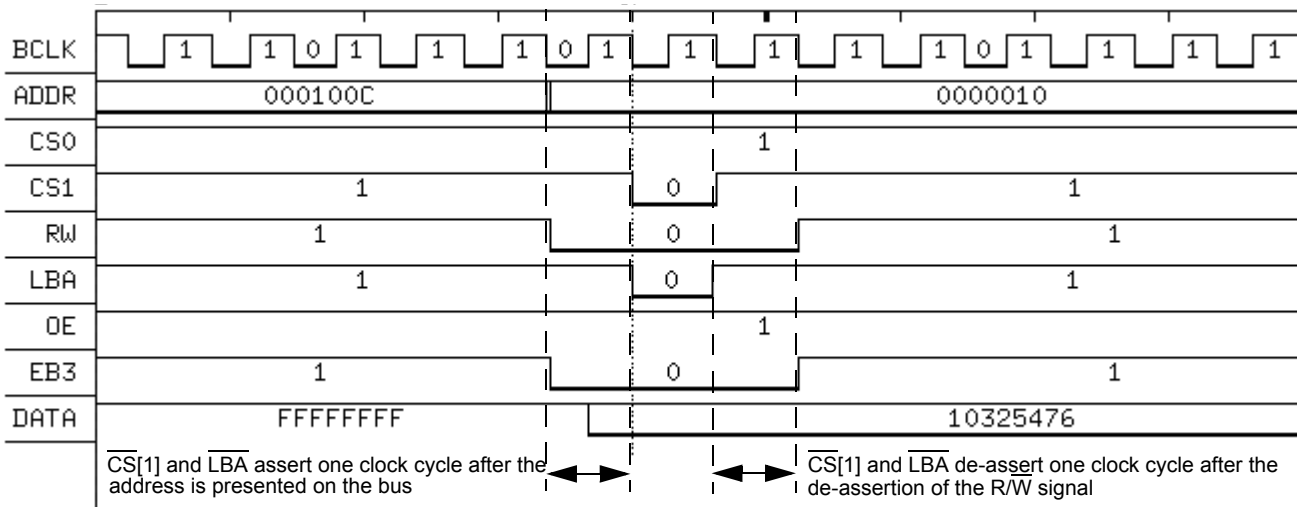

Figure 19 depicts a write access on CS[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000200
CS1L = 0x00001E01
The Wait State Control (WCS) bits are set to 2 and for this example, CSA is set to 1. This figure shows that with CSA set to 1, the chip select signal CS[1] asserts one clock cycle after the address is presented on the bus (or relative to the assertion of the R/W signal) and de-asserts one clock cycle before the de-assertion of the R/W signal. Adjusting the CSA bit setting affects write cycles only. Furthermore, this figure illustrates that the signal LBA follows the CS[1] signal.

Figure 19. WSC=2, CSA=1, EBC=1 (Write)

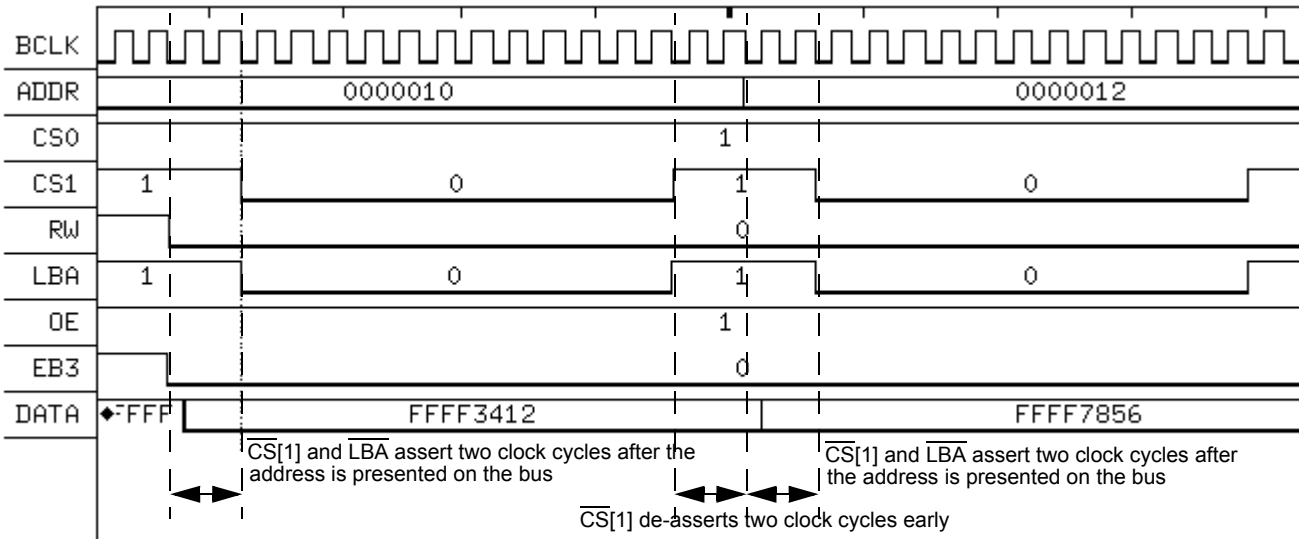

Figure 20 depicts a 32-bit write access on CS[1] with the EIM set up for a 16-bit data port, in this case causing two external back-to-back 16-bit accesses. The chip select control register settings for this example are:
CS1U = 0x00000F00
CS1L = 0x00002D01
The Wait State Control (WCS) bits are set to 15 and for this example, CSA is set to 2. This figure shows that with CSA set to 2, the chip select signal CS[1] asserts two clock cycles after the address is presented on the bus (or relative to the assertion of the R/W signal) and de-asserts two clock cycles before the next address is placed on the bus. Adjusting the CSA bit setting affects write cycles only. Furthermore, this figure illustrates that the signal LBA follows the CS[1] signal.

Figure 20. WSC=15, CSA=2, EBC=1, DSIZ= 101 (Write)

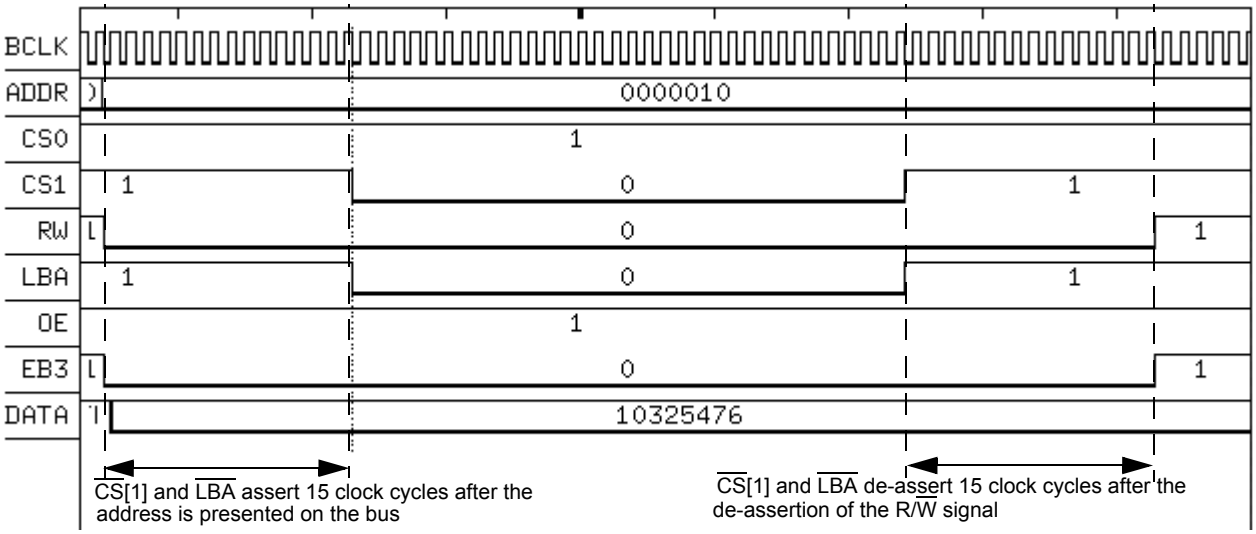

Figure 21 depicts a write access on CS[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00003E00
CS1L = 0x0000FE01
The Wait State Control (WCS) bits are set to 62 and for this example, CSA is set to 15. This figure shows that with CSA set to 15, the chip select signal CS[1] asserts fifteen clock cycles after the address is presented on the bus (or relative to the assertion of the R/W signal) and de-asserts fifteen clock cycles before the de-assertion of the R/W signal. Adjusting the CSA bit setting affects write cycles only. Furthermore, this figure illustrates that the signal LBA follows the CS[1] signal.

Figure 21. WSC=62, CSA=15, EBC=1 (Write)

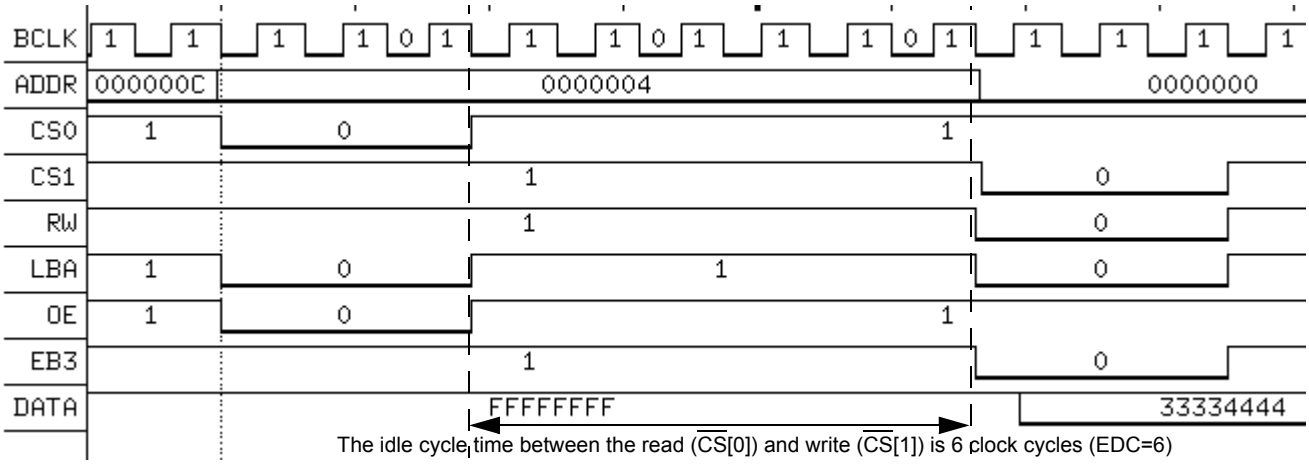

Figure 22 gives an example of varying the Extra Dead Cycle (EDC), depicts a read access on $\overline{CS}$[0] followed by a write access from $\overline{CS}$[1]. The setting of the EDC bits determine the number of idle cycles inserted after a read cycle for back-to-back transfers. The chip select 0 and chip select 1 control register settings for this example are:

CS0U = 0x00000206
CS0L = 0x00000E01
CS1U = 0x00000200
CS1L = 0x00000E01

The Wait State Control (WCS) bits for both chip selects are set to 2 and for this example, EDC is set to 6 for $\overline{CS}$[0]. That means that 6 idle cycles are inserted after the read cycle performed by $\overline{CS}$[0] before the write access takes place on $\overline{CS}$[1], where EDC only inserts idle cycles for transfers taking between two different chip selects.

To minimize amount of external transfers, the instructions that were used to perform these accesses were stored in internal RAM (using the i.MX1 chip), and to minimize the time between transfers, the I cache was enabled. However, it was found that the minimum idle time between the transfers was 6 clock cycles, meaning that if the EDC bits were set to anything less than 6, the idle cycles will still remain at 6 clock cycles. However, increasing the EDC time will summarily increase the idle cycle time between the two transfers as seen in the following examples.

Figure 22. $\overline{CS}$[0]: WSC=2, EDC=6, EBC=1 (Read). $\overline{CS}$[1]: WSC=2, EBC=1 (Write)

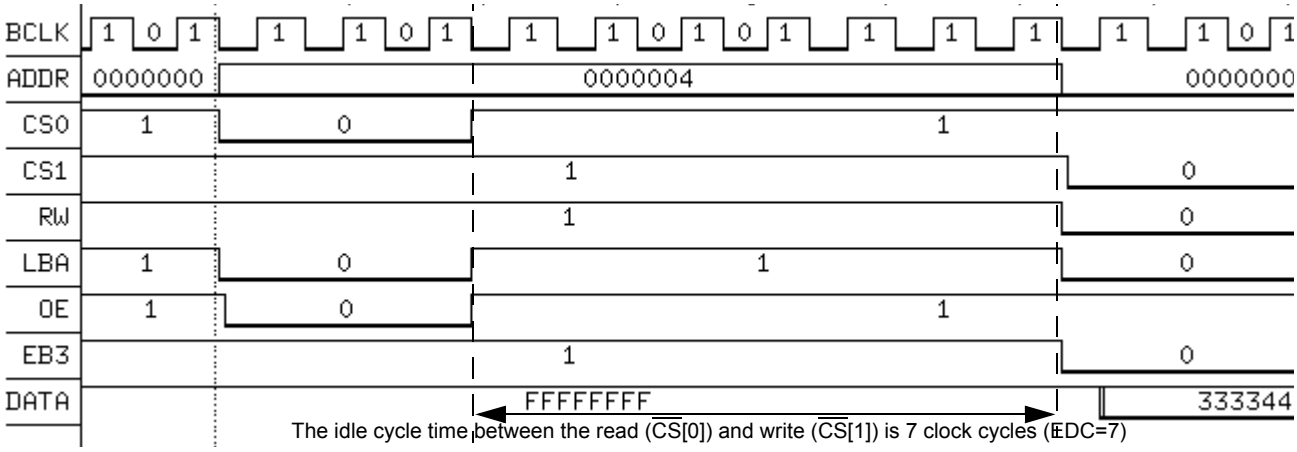

Figure 23 gives an example of varying the Extra Dead Cycle (EDC), depicts a read access on $\overline{CS}$[0] followed by a write access from $\overline{CS}$[1]. The setting of the EDC bits determine the number of idle cycles inserted after a read cycle for back-to-back transfers. The chip select 0 and chip select 1 control register settings for this example are:

CS0U = 0x00000207
CS0L = 0x00000E01
CS1U = 0x00000200
CS1L = 0x00000E01

The Wait State Control (WCS) bits for both chip selects are set to 2 and for this example, EDC is set to 7 for $\overline{CS}$[0]. That means that 7 idle cycles are inserted after the read cycle performed by $\overline{CS}$[0] before the write access takes place on $\overline{CS}$[1], where EDC only inserts idle cycles for transfers taking between two different chip selects.

Figure 23. $\overline{CS}$[0]: WSC=2, EDC=7, EBC=1 (Read). $\overline{CS}$[1]: WSC=2, EBC=1 (Write)

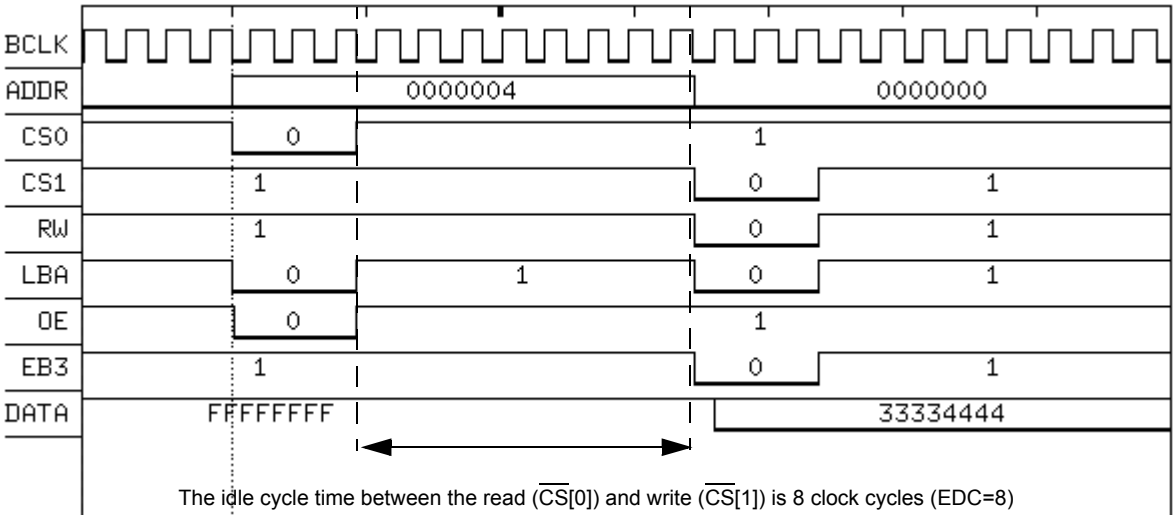

Figure 24 gives an example of varying the Extra Dead Cycle (EDC), depicts a read access on CS[0] followed by a write access from CS[1]. The setting of the EDC bits determine the number of idle cycles inserted after a read cycle for back-to-back transfers. The chip select 0 and chip select 1 control register settings for this example are:

CS0U = 0x00000208
CS0L = 0x00000E01
CS1U = 0x00000200
CS1L = 0x00000E01

The Wait State Control (WCS) bits for both chip selects are set to 2 and for this example, EDC is set to 8 for CS[0]. That means that 8 idle cycles are inserted after the read cycle performed by CS[0] before the write access takes place on CS[1], where EDC only inserts idle cycles for transfers taking between two different chip selects.

Figure 24. CS[0]: WSC=2, EDC=8, EBC=1 (Read). CS[1]: WSC=2, EBC=1 (Write)

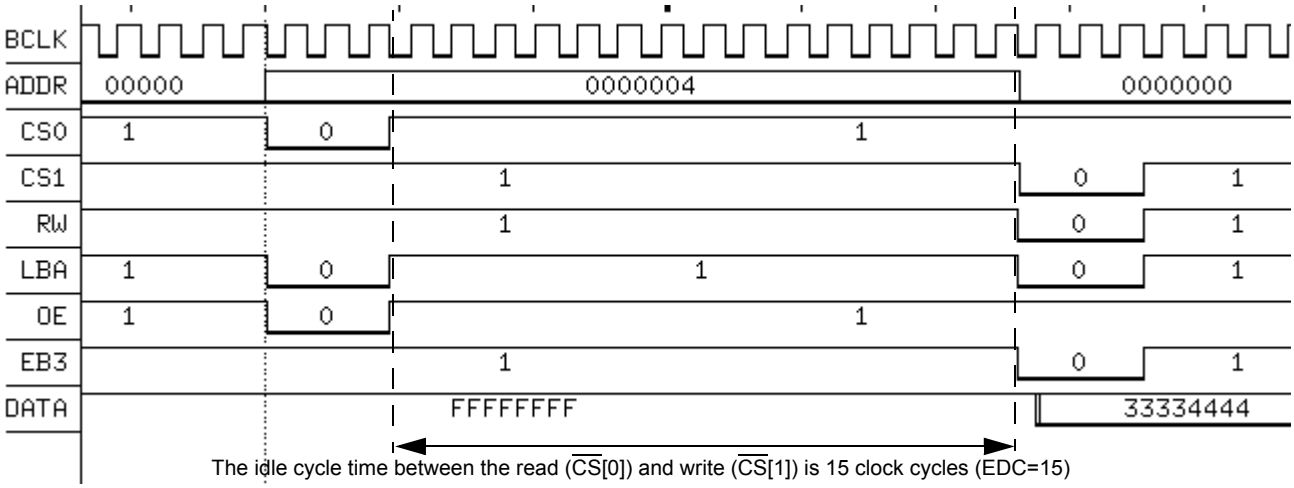

Figure 25 gives an example of varying the Extra Dead Cycle (EDC), depicts a read access on CS[0] followed by a write access from CS[1]. The setting of the EDC bits determine the number of idle cycles inserted after a read cycle for back-to-back transfers. The chip select 0 and chip select 1 control register settings for this example are:

CS0U = 0x0000020F
CS0L = 0x00000E01
CS1U = 0x00000200
CS1L = 0x00000E01

The Wait State Control (WCS) bits for both chip selects are set to 2 and for this example, EDC is set to 15 for CS[0]. That means that 15 idle cycles are inserted after the read cycle performed by CS[0] before the write access takes place on CS[1], where EDC only inserts idle cycles for transfers taking between two different chip selects.

Figure 25. CS[0]: WSC=2, EDC=15, EBC=1 (Read). CS[1]: WSC=2, EBC=1 (Write)

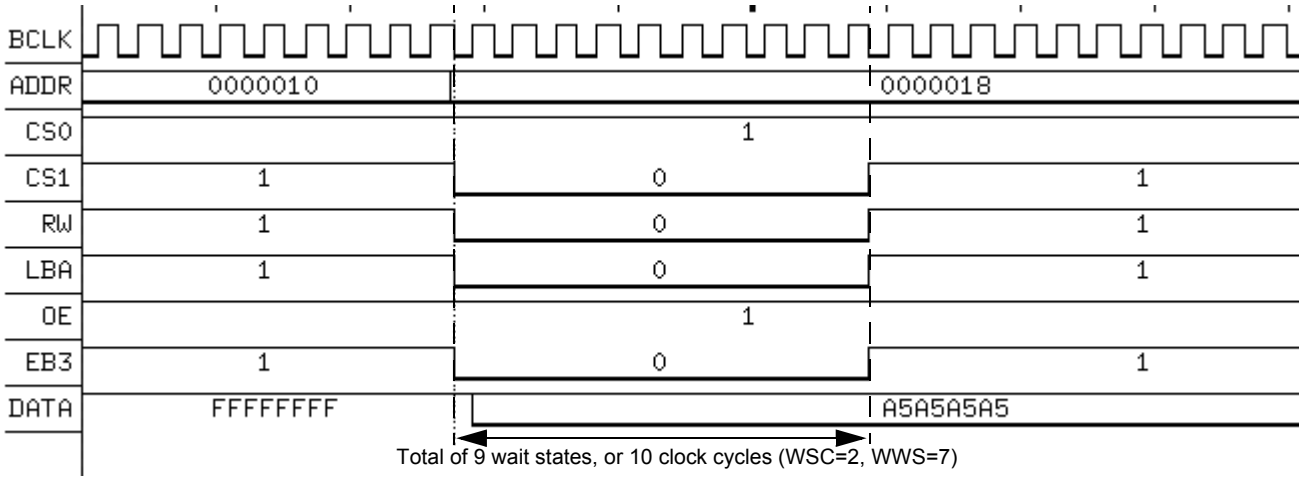

Figure 26 depicts a write access on $\overline{CS}$[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000270
CS1L = 0x00000E01
The Wait State Control (WCS) bits are set to 2 and for this example, WWS (Write Wait States) is set to 7. The WWS setting adds 7 more wait states, totaling 9 wait states for write accesses or 10 clock cycles.

Figure 26. WSC=2, WWS=7, EBC=1 (Write)

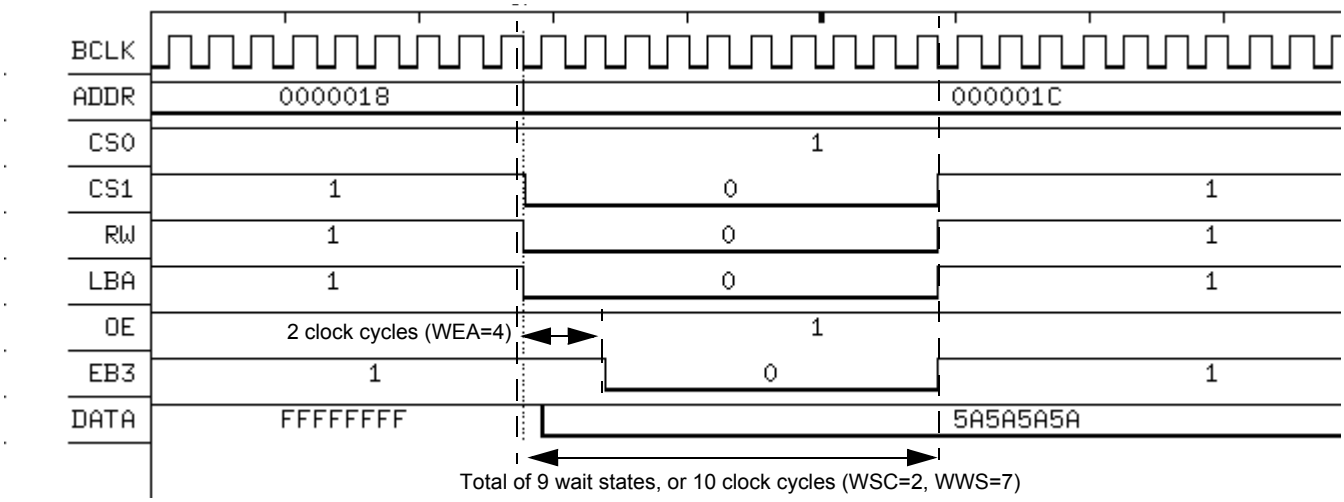

Figure 27 depicts a write access on $\overline{CS}$[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000270
CS1L = 0x00400E01
The Wait State Control (WCS) bits are set to 2 and for this example, WWS (Write Wait States) is set to 7. The WWS setting adds 7 more wait states, totaling 9 wait states for write accesses or 10 clock cycles. Also, in this example, WEA is set to 4 indicating a 2 clock cycle delay from when the address is placed on the bus to the assertion of the $\overline{EB}$ signal, and WEN is set to 0.

Figure 27. WSC=2, WWS=7, WEA=4, WEN=0, EBC=1 (Write)

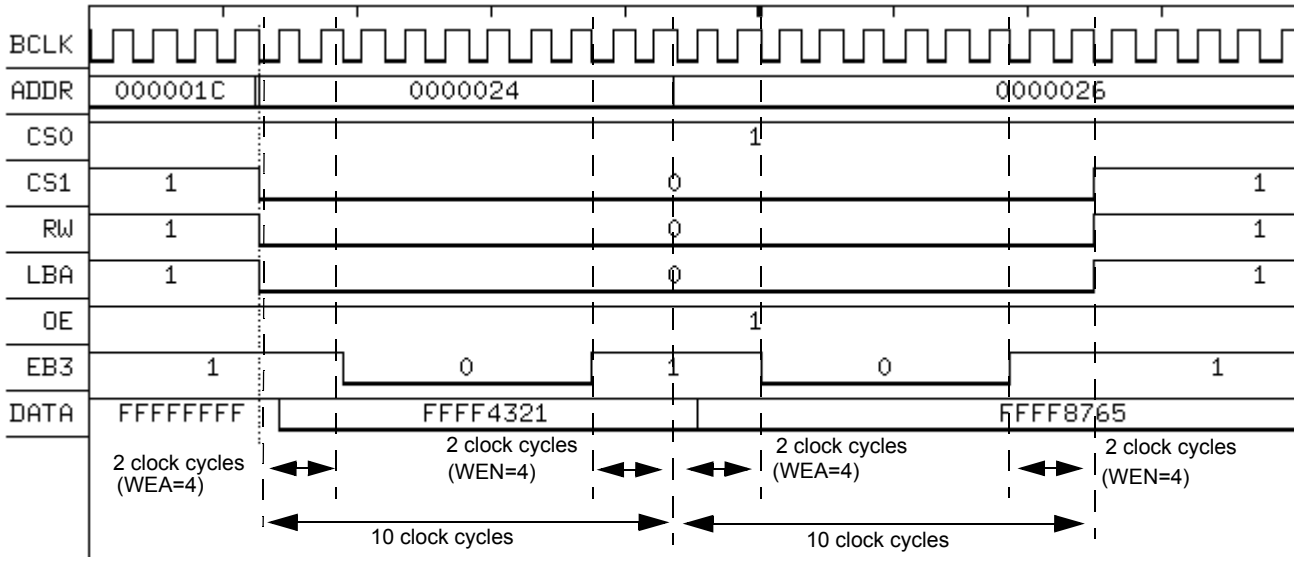

Figure 28 depicts a 32-bit write access on $\overline{CS}$[1] with the EIM set up for a 16-bit data port, in this case causing two external back-to-back 16-bit accesses. The chip select control register settings for this example are:
CS1U = 0x00000270
CS1L = 0x00440D01
The Wait State Control (WCS) bits are set to 2 and for this example, WWS (Write Wait States) is set to 7. The WWS setting adds 7 more wait states, totaling 9 wait states for write accesses or 10 clock cycles. Also, in this example, WEA is set to 4 indicating a 2 clock cycle delay from when the address is placed on the bus to the assertion of the $\overline{EB}$ signal, and WEN is set to 4 indicating that the $\overline{EB}$ signal de-asserts a 2 clock cycles before the de-assertion of the chip select (or in the case of back-to-back write accesses, it will de-assert 2 clock cycles before the associated write address is removed from the bus).

Figure 28. WSC=2, WWS=7, WEA=4, WEN=4, EBC=1, DSIZ= 101 (Write)

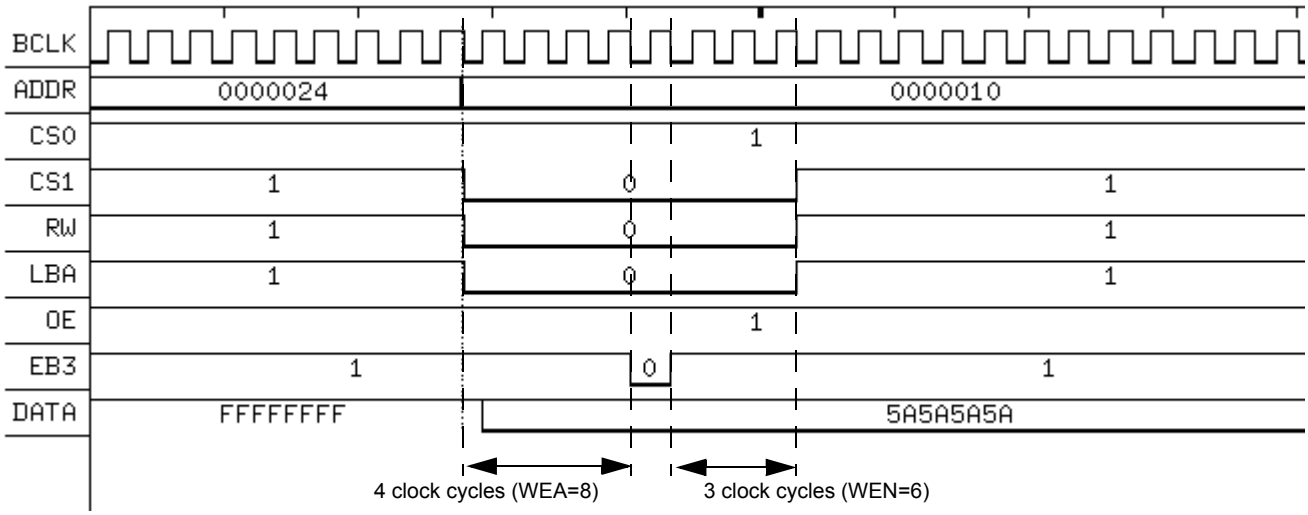

Figure 29 depicts a write access on $\overline{CS}$[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000700
CS1L = 0x00860E01
The Wait State Control (WCS) bits are set to 7 and for this example WEA is set to 8 indicating a 4 clock cycle delay from when the address is placed on the bus to the assertion of the $\overline{EB}$ signal, and WEN is set to 6 indicating that the $\overline{EB}$ signal de-asserts 3 clock cycles before the de-assertion of the chip select (or in the case of back-to-back write accesses, it will de-assert 3 clock cycles before the associated write address is removed from the bus).

Figure 29. WSC=7, WEA=8, WEN=6, EBC=1 (Write)

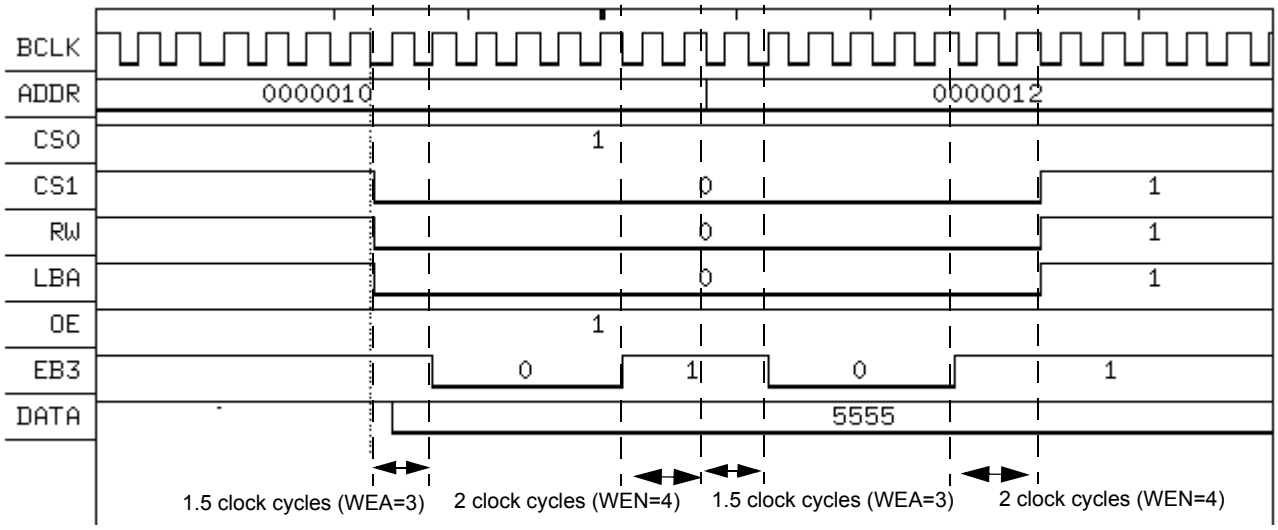

Figure 30 depicts a 32-bit write access on $\overline{CS}$[1] with the EIM set up for a 16-bit data port forcing two back-to-back 16-bit accesses. The chip select control register settings for this example are:
CS1U = 0x00000700
CS1L = 0x00340D01
The Wait State Control (WCS) bits are set to 7 and for this example WEA is set to 3 indicating a 1.5 clock cycle delay from when the address is placed on the bus to the assertion of the $\overline{EB}$ signal, and WEN is set to 4 indicating that the $\overline{EB}$ signal de-asserts 2 clock cycles before the de-assertion of the chip select (or in the case of back-to-back write accesses, it will de-assert 2 clock cycles before the associated write address is removed from the bus).

Figure 30. WSC=7, WEA=3, WEN=4, EBC=1, DSIZ= 101 (Write)

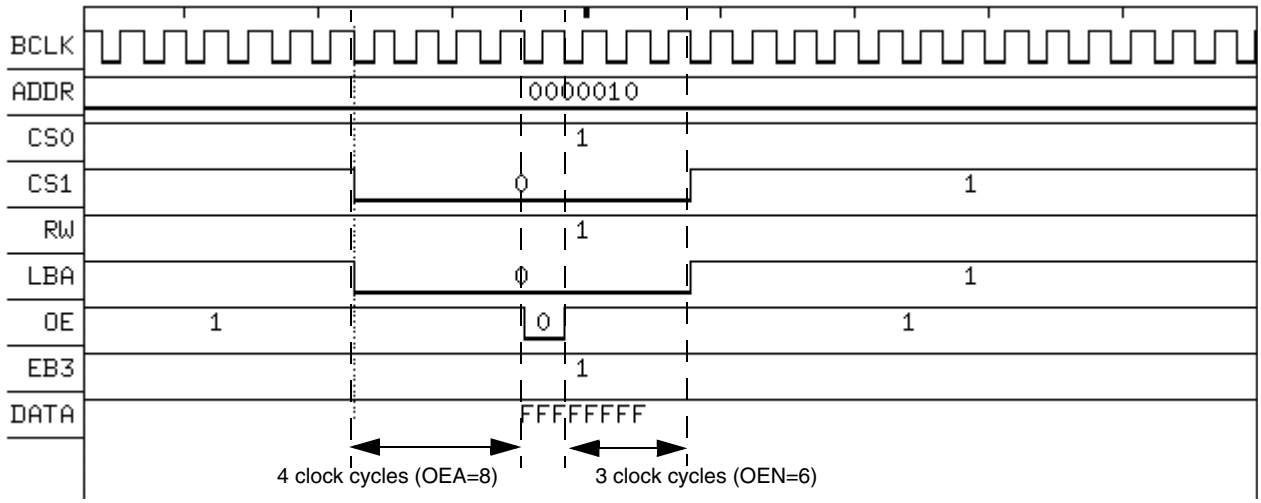

Figure 31 depicts a read access on $\overline{CS}$[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000700
CS1L = 0x86000E01
The Wait State Control (WCS) bits are set to 7 and for this example OEA is set to 8 indicating a 4 clock cycle delay from when the address is placed on the bus to the assertion of the $\overline{OE}$ signal, and OEN is set to 6 indicating that the $\overline{OE}$ signal de-asserts 3 clock cycles before the de-assertion of the chip select (or in the case of back-to-back write accesses, it will de-assert 3 clock cycles before the associated write address is removed from the bus).

Figure 31. WSC=7, OEA=8, OEN=6, EBC=1 (Read)

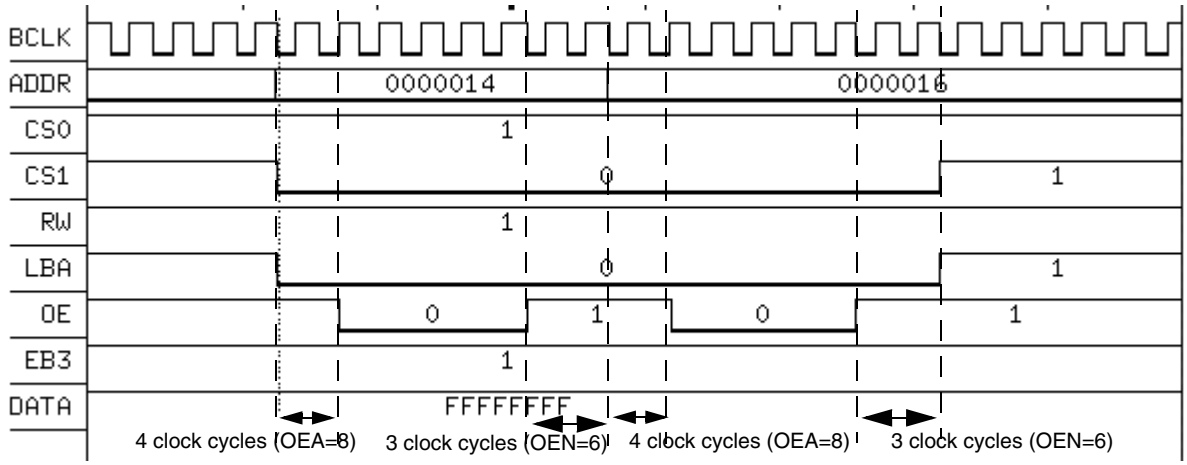

Figure 32 depicts a 32-bit read access on $\overline{CS}$[1] with the EIM set up for a 16-bit data port, forcing two external back-to-back 16-bit accesses. The chip select control register settings for this example are:
CS1U = 0x00000700
CS1L = 0x86000D01
The Wait State Control (WCS) bits are set to 7 and for this example OEA is set to 8 indicating a 4 clock cycle delay from when the address is placed on the bus to the assertion of the $\overline{OE}$ signal, and OEN is set to 6 indicating that the $\overline{OE}$ signal de-asserts 3 clock cycles before the de-assertion of the chip select (or in the case of back-to-back write accesses, it will de-assert 3 clock cycles before the associated write address is removed from the bus, as seen in the figure above).

Figure 32. WSC=7, OEA=8, OEN=6, EBC=1, DSIZ= 101 (Read)

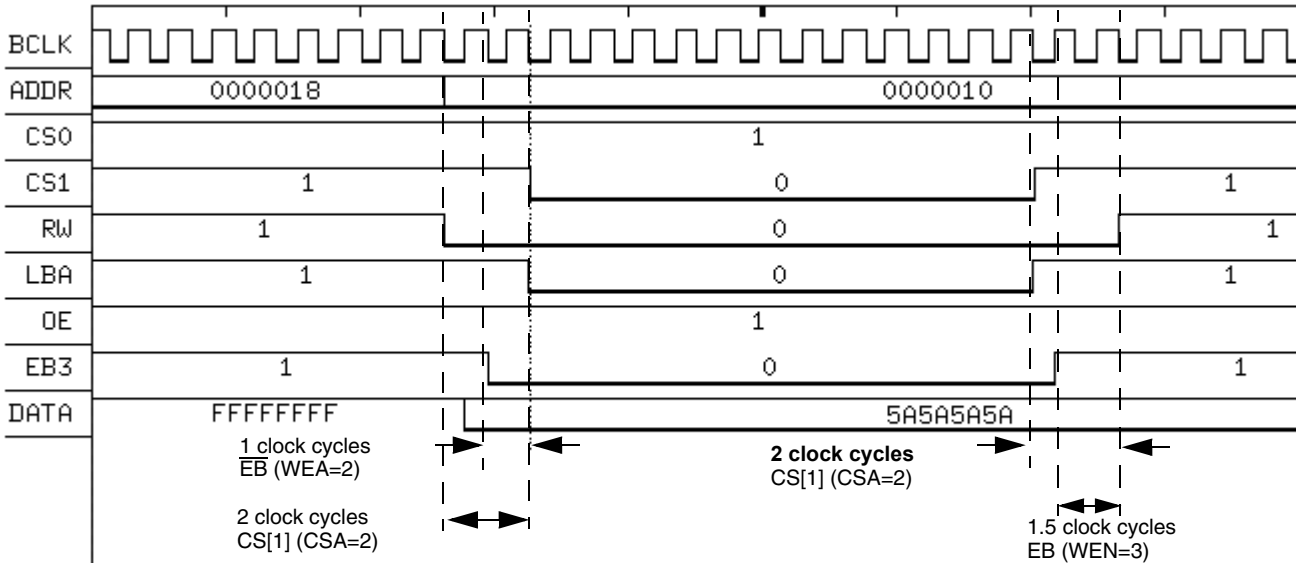

Figure 33 depicts a write access on $\overline{CS}$[1] with the EIM set up for a 32-bit data port. The chip select control register settings for this example are:
CS1U = 0x00000F00
CS1L = 0x00232E01
The Wait State Control (WCS) bits are set to 15 and for this example, a write cycle with a combination of settings for WEA, WEN, and CSA. WEA is set to 2 indicating a 1 clock cycle delay from when the address is placed on the bus to the assertion of the $\overline{EB}$ signal, and WEN is set to 3, indicating that the $\overline{EB}$ signal will de-assert 1.5 clock cycles from the de-assertion of the R/W signal. Normally, we would reference the $\overline{EB}$ signal de-assertion to the de-assertion of the $\overline{CS}$[1], but you will notice that by setting the CSA bits, the $\overline{CS}$[1] timing also changes, such that in this case, the $\overline{CS}$[1] asserts 2 clock cycles after the address is placed on the bus and de-asserts 2 clock cycles before the de-assertion of the R/$\overline{W}$ signal. In fact, for write cycles, the timing changes in $\overline{CS}$[1] and $\overline{EB}$ may be referenced from the assertion/de-assertion of the R/$\overline{W}$ signal as it's timing is not affected by any of the EIM chip select control register bits (except for the total access time which is programmed via the WSC bits).

Figure 33. WSC=15, WEA=2, WEN=3, CSA=2, EBC=1 (Write)

4 References

The following documents can be used for additional information:

1. *MC9328MX1 i.MX Integrated Portable System Processor Reference Manual* (order number: MC9328MX1RM)
2. *MC9328MXL i.MX Integrated Portable System Processor Data Sheet* (order number: MC9328MXLRM)
3. *MC9328MXS i.MX Integrated Portable System Processor Data Sheet* (order number: MC9328MXSRM)

For these and other technical documents about the i.MX products, go to www.freescale.com/imx.

5 Revision History

This revision is for the purpose of applying the Freescale template and does not include technical content changes.

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