Freescale Semiconductor
Application Note

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Common Footprint for the MPC7441, MPC7445, MPC7447, MPC7447A, and MPC7448

This document describes how to design a platform with a common footprint for the MPC7441, MPC7445, MPC7447, and MPC7447A. It is intended to help you design a single board that is compatible with all of these devices. This document is not a complete migration guide.

In general, the MPC7447A is backwards-compatible with a system designed for the MPC7441, MPC7445, or MPC7447 if the proper core voltage can be supplied. Similarly, a system designed for the MPC7447A can accommodate these earlier processors if the core voltage is compatible with or can be changed to accommodate the earlier device. See the appropriate hardware specifications and part number specifications (if applicable) for detailed information.

Forward compatibility with the MPC7448 requires separate consideration. Therefore, this application note presents recommendations for various signals to ensure forward compatibility with future generations of devices following the MPC7447A, including the MPC7448.

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1 Footprint Compatibility for MPC7447A and Earlier Devices

This section discusses signal differences among the MPC7447A and the MPC7441, MPC7445, and MPC7447. Only signals requiring a change during migration are discussed. Signals not mentioned, such as the 60x/MPX system bus signals, are identical in all generations of the device family and require no special consideration for backward or forward compatibility. Detailed information and the full pin listing for each device is available in the corresponding hardware specifications listed in Table 1.

Table 1. Hardware Specifications for MPC744x Devices

Device	Hardware Specifications Document Title	Freescale Order Number
MPC7441	*MPC7441 RISC Microprocessor Hardware Specifications*	MPC7441EC
MPC7445	*MPC7455 RISC Microprocessor Hardware Specifications*	MPC7455EC
MPC7447	*MPC7457 RISC Microprocessor Hardware Specifications*	MPC7457EC
MPC7447A	*MPC7447A RISC Microprocessor Hardware Specifications*	MPC7447AEC

1.1 Pin Differences Summary

The pinout for each device is presented in the corresponding hardware specifications listed in Table 1. Table 2 summarizes the pin differences among the MPC7441, MPC7445, MPC7447, and MPC7447A. The table also includes recommendations for forward compatibility with the MPC7448; for details on forward compatibility with the MPC7448, see Section 2, “Forward Compatibility with the MPC7448.”

Table 2. Pin Differences Summary

Pin	MPC7441 MPC7445 MPC7447	MPC7447A	Comment
A13	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
A16	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
A17	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
A18	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
A19	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
B13	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
B16	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
B17	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
B18	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
B19	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
C13	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
E12	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
E13	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
E16	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility

Table 2. Pin Differences Summary (continued)

Pin	MPC7441 MPC7445 MPC7447	MPC7447A	Comment
E18	OV_{DD}	OVDD_SENSE	Connect to OV_{DD} if unused
E19	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
F12	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
F13	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
F16	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
F17	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
F18	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
F19	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
G11	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
G12	No Connect	GND_SENSE	Recommend connect to GND if unused, may be unconnected
G13	No Connect	VDD_SENSE	Recommend connect to V_{DD} if unused, may be unconnected
G16	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
G18	OV_{DD}	OVDD_SENSE	Connect to OV_{DD} if unused
G19	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
H14	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
H17	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
H18	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
H19	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
J14	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
L14	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
M14	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
M15	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
M16	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
M17	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
M18	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
M19	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
N12	No Connect	VDD_SENSE	Recommend connect to V_{DD} if unused, may be unconnected
N13	No Connect	GND_SENSE	Recommend connect to GND if unused, may be unconnected
N14	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
N15	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
N16	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
N17	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
N18	No Connect	TEMP_ANODE	Anode of temperature sense diode

Table 2. Pin Differences Summary (continued)

Pin	MPC7441 MPC7445 MPC7447	MPC7447A	Comment
N19	No Connect	TEMP_CATHODE	Cathode of temperature sense diode
P15	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility
P16	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
P18	No Connect	V_{DD}	May be unconnected, recommend connect to V_{DD} for forward compatibility
P19	No Connect	GND	May be unconnected, recommend connect to GND for forward compatibility

1.2 New Signals on the MPC7447A and Backward Compatibility with the MPC7441, MPC7445, and MPC7447

This section discusses new signals on the MPC7447A compared to the MPC7441, MPC7445, and MPC7447, and it presents recommendations for incorporating them into a footprint that can accommodate all of these processors.

1.2.1 Power and Ground Signals

In general, most changes use no-connect pins for additional power and ground pins. For backwards compatibility, these pins can be left unconnected with no detrimental effects. Similarly, the MPC7441, MPC7445, or MPC7447 can be populated in a socket where these signals are connected to the power and ground planes; see Section 1.2.6, “Boundary Scan Testing Considerations,” for cautions on boundary scan testing.

1.2.2 GND_SENSE

The GND_SENSE signals are no-connect pins for the MPC7441, MPC7445, and MPC7447. For the MPC7447A, they are connected to the GND plane inside the device package. They allow an external device to detect the voltage level on the ground plane inside the package. If these signals are not used, they can be connected directly to the GND plane on the board (in which case they essentially become additional ground pins), or they may be left unconnected. See Section 1.2.6, “Boundary Scan Testing Considerations,” for cautions on boundary scan testing.

1.2.3 VDD_SENSE

The VDD_SENSE signals are no-connect pins for the MPC7441, MPC7445, and MPC7447. For the MPC7447A, they are connected to the V_{DD} plane inside the device package and allow an external device to detect the actual voltage level present on this plane. For example, a power supply with compensation capabilities can use this signal to detect a low-voltage condition at the device and raise the voltage level accordingly to compensate. If these signals are not used, they can be connected directly to the V_{DD} plane on the board (in which case they essentially become additional power pins), or they can be left unconnected. See Section 1.2.6, “Boundary Scan Testing Considerations,” for cautions on boundary scan testing.

1.2.4 OVDD_SENSE

The OVDD_SENSE signals are OV_{DD} pins for the MPC7441, MPC7445, and MPC7447. For the MPC7447A, they are connected to the OV_{DD} plane inside the device package and allow an external device to detect the actual voltage level on this plane. For example, a power supply with compensation capabilities can use this signal to detect a low-voltage condition at the device and raise the voltage level accordingly to compensate. If these signals are not used, they can be connected directly to the OV_{DD} plane on the board (in which case they essentially become additional power pins), or they can be left unconnected. Because these signals are OV_{DD} pins for the MPC7441, MPC7445, and MPC7447, it is recommended that they be connected to OV_{DD} if they are not used as voltage sense pins.

1.2.5 TEMP_ANODE and TEMP_CATHODE

The TEMP_ANODE and TEMP_CATHODE signals are no-connect pins for the MPC7441, MPC7445, and MPC7447. On the MPC7447A, these signals provide connections to the on-chip temperature diode, thus allowing an external device to determine the die temperature of the MPC7447A. The signals should be left unconnected if unused. For details on the temperature diode, see the *MPC7447A RISC Microprocessor Hardware Specifications*. See also Section 1.2.6, “Boundary Scan Testing Considerations,” for cautions on boundary scan testing.

1.2.6 Boundary Scan Testing Considerations

For signals that are defined as no-connect pins on the MPC7441, MPC7445, and MPC7447, caution must be exercised if boundary scan testing is performed when one of these earlier devices is populated in a system designed for the MPC7447A. Boundary scan operations can cause the MPC7441, MPC7445, and MPC7447 to actively drive these no-connect signals, creating contention and excess current draw through these signals. Therefore, boundary scan testing must not cause these signals to be driven.

1.3 Configuration Signals

The configuration signals for the MPC7447A are identical to those on the MPC7441, MPC7445, and MPC7447. The sections that follow contain supplemental information and recommendations for configuring these signals.

1.3.1 BVSEL

BVSEL selects the I/O voltage mode for the 60x/MPX bus interface. The possible configurations of this signal are the same for all of the devices described in this document and are shown in Table 3.

Table 3. I/O Voltage Selection for the MPC7441, MPC7445, MPC7447 and MPC7447A

BVSEL	I/O voltage mode	Comment
0	1.8 V	Use 250-Ω or stronger pull-down resistor

Table 3. I/O Voltage Selection for the MPC7441, MPC7445, MPC7447 and MPC7447A (continued)

BVSEL	I/O voltage mode	Comment
¬$\overline{\text{HRESET}}$	Not available	¬$\overline{\text{HRESET}}$ is the inverse of active-low $\overline{\text{HRESET}}$ signal
HRESET	2.5 V	Connect to $\overline{\text{HRESET}}$ via jumper to allow reconfiguration
1	2.5 V	Use weak (10-KΩ or stronger) pull-up resistor
Unconnected	2.5 V	Internal pull-up resistor on die; not recommended

We recommend that you use a flexible configuration scheme so that this pin can be reconfigured later. For the same reason, leaving this pin unconnected to select 2.5-V I/O voltage mode is not recommended even though this is functionally permissible. For information on this pin and forward compatibility, see Section 2.3, "Forward Compatibility and BVSEL." Note that because connecting BVSEL to $\overline{\text{HRESET}}$ selects the same I/O voltage mode as terminating it to OV_{DD}, new designs need only implement options to pull this pin high or low; and an option to connect it to $\overline{\text{HRESET}}$ is not necessary.

1.3.2 PLL_CFG[0:4]

The PLL_CFG[0:4] signals determine the processor core frequency by selecting the multiplier to be multiplied by the SYSCLK frequency to achieve the core frequency. Due to speed enhancements between generations and often within a single generation, you may have to select different bus-to-core ratios to accommodate a variety of device speed grades. It is also useful during system debug to be able to reduce the core frequency if a thermal, power supply, or noise issue is suspected as the cause of problems in a system. Therefore, both pull-up and pull-down resistor options should always be provided for all PLL_CFG signals to allow the flexibility to reconfigure them later.

2 Forward Compatibility with the MPC7448

This section presents recommendations for designing a footprint to ensure forward compatibility with the MPC7448 processor.

2.1 Forward Compatibility for Power and Ground

For new designs, the added power and ground pins should be connected to the appropriate power or ground plane to allow for forward compatibility, because future products, including the MPC7448, may require these additional power and ground signals to achieve higher core frequencies.

2.2 Forward Compatibility and TEST[0:4]

TEST[0:4] are designated as factory test pins on the MPC7441, MPC7445, MPC7447, and MPC7447A. However, on the MPC7448, these pins are redefined as additional reset configuration pins to support additional features. Therefore, it is strongly recommended that new designs implement a flexible configuration scheme that allows these signals to be connected to either OV_{DD} or GND to ensure the ability to take full advantage of any future enhancements. For information on the functions of these signals, consult the *MPC7448 RISC Microprocessor Hardware Specifications* and *MPC7450 RISC Microprocessor Family User's Manual*. Table 4 shows the terminations required for the MPC7441,

MPC7445, MPC7447, and MPC7447A, as well as the recommendations to ensure forward compatibility with the MPC7448.

Table 4. TEST[0:4] Terminations for the MPC7447A and MPC7448

Pin	MPC7447A (and earlier devices)		MPC7448	
	Signal Name	Required Termination	Signal Name	Recommended Termination
A12	TEST[0]	OV_{DD}	DFS2	Can be pulled up if unused, or it can be connected to external logic to allow control of DFS mode via hardware. Note that pulling down both $\overline{DFS2}$ and $\overline{DFS4}$ completely disables dynamic frequency switching (including software control), which may be desirable in some systems.
B6	TEST[1]	OV_{DD}	DFS4	
B10	TEST[2]	OV_{DD}	LVRAM	OV_{DD}; provide option to connect to GND.
E10	TEST[3]	OV_{DD}	BVSEL[1]	Provide options to connect to OV_{DD} or GND.
D10	TEST[4]	GND	PLL_CFG[5]	Provide options to connect to OV_{DD} or GND.

Additional information on some of these signals is provided in the sections that follow.

2.3 Forward Compatibility and BVSEL

The MPC7448 uses a bus voltage configuration method similar to the MPC7447A and earlier products. However, it implements a second bus voltage select signal, BVSEL1, to configure the I/O voltage. Both this signal and BVSEL0 (named BVSEL on the MPC7447A) are actively monitored input signals. This replaces the previous configuration scheme of the MPC7447A where the BVSEL signal was sampled twice, once before and once after $\overline{HRESET}$ negation. As a result of this change, new designs need only implement options to pull this pin high or low, and an option to connect it to $\overline{HRESET}$ is not necessary

Table 5 compares the I/O voltages mode configurations for the MPC7447A and MPC7448. If the I/O voltage is 2.5 V, then no change is necessary if BVSEL1 (called TEST3 on the MPC7447A and earlier devices) is pulled high per the requirements for the earlier devices. This includes cases where BVSEL0 is connected to $\overline{HRESET}$ because, as shown in the table, the MPC7448 is always in 2.5 V mode when BVSEL1 is pulled high, regardless of the state of BVSEL0. The configuration must be modified if the I/O voltage is 1.8 V because the termination of BVSEL1 must be changed from pulled up to pulled down.

Table 5. Input Threshold Voltage Setting for the MPC7447A and MPC7448

I/O Voltage Mode	MPC7447A (and earlier devices)		MPC7448	
	BVSEL (pin B7)	TEST3 [1] (pin E10)	BVSEL0 (pin B7)	BVSEL1 (pin E10)
1.8 V	0	1	0	0
2.5 V	$\overline{HRESET}$	1	0	1
1.5 V	— [2]	—	1	0

Table 5. Input Threshold Voltage Setting for the MPC7447A and MPC7448 (continued)

I/O Voltage Mode	MPC7447A (and earlier devices)		MPC7448	
	BVSEL (pin B7)	TEST3 [1] (pin E10)	BVSEL0 (pin B7)	BVSEL1 (pin E10)
2.5 V	1	1	1	1

1. TEST3 must be pulled up on the MPC7447A, MPC7447, MPC7445, and MPC7441.
2. The MPC7447A, MPC7447, MPC7445, and MPC7441 do not support 1.5V I/O.

Future devices may offer a different range of supported I/O voltages. Therefore, regardless of the I/O voltage mode is selected, enough flexibility must be incorporated into the design to allow for future reconfiguration of these signals. A programmable logic device meets this criterion. If these signals are instead to be configured by termination to OV_{DD} or GND, make provisions to allow for selection of other configurations by providing resistor pads or jumper options for other terminations.

2.4 Forward Compatibility and PLL_CFG Signals

The PLL configurations for the MPC7447A and MPC7448 are identical if one excludes the addition of PLL_CFG[5]. This additional PLL_CFG signal allows for future flexibility but is currently defined as a factory-only test pin and should be pulled down to ensure proper device operation. Therefore, no change is necessary to PLL_CFG[0:4] when migrating from the MPC7447A unless you want to change the core frequency. Note that some earlier devices (the MPC7441 and early revisions of the MPC7445) used different PLL_CFG settings. See the *MPC7448 RISC Microprocessor Hardware Specifications* for information on the configuration of the PLL on the MPC7448.

Because speed enhancements are made with each device generation, the multipliers supported by each device may change from time to time to allow for the inclusion of multipliers more appropriate for the core frequency targets of the device. Furthermore, speed enhancements often occur within a single generation, and it may be desirable to reconfigure the PLL to select a higher multiplier to take advantage of faster device offerings if they become available. Therefore, both pull-up and pull-down resistor options should always be provided for all PLL_CFG signals to allow the flexibility to reconfigure them later.

2.5 Other MPC7448 Signals

Other MPC7448 signals of note are as follows:

- GND_SENSE. These signals are identical to the GND_SENSE signals on the MPC7447A.
- VDD_SENSE. These signals are identical to the VDD_SENSE signals on the MPC7447A.
- OVDD_SENSE. These signals are identical to the OVDD_SENSE signals on the MPC7447A.
- TEMP_ANODE and TEMP_CATHODE. These signals are identical to the TEMP_ANODE and TEMP_CATHODE signals on the MPC7447A.

3 Revision History

Table 6 provides a revision history for this application note.

Table 6. Document Revision History

Rev. No.	Date	Substantive Change(s)
4	01/2007	Non-substantive formatting.
3	01/25/05	Section 2.3: Corrected Table 5. Pin values in parentheses were incorrect
2	01/13/05	Section 2.3: Corrected Table 5 and accompanying text. BVSEL[0:1] settings were incorrect.
1	01/05/05	Section 1.2.4, “OVDD_SENSE”: Corrected recommendation for unused OVDD_SENSE pin to be terminated to OVDD (not VDD as was previously stated). Updated document as appropriate and changed title to reflect MPC7448 information.
0.1	06/04/04	Corrected terminations for TEST[0:3] AND TEST[4] in Table 4. The correct terminations are given in the MPC7447A hardware specifications.
0	03/24/04	Initial release

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