Freescale Semiconductor
Application Note

Document Number: AN2537
Rev. 3, 11/2006

Power Network Design

MC9328MX1, MC9328MXL, and MC9328MXS

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1 Abstract

As power network design becomes more complex, a number of criteria must be considered. Because the i.MX applications processors are designed to support several independent voltage banks and voltage ranges, specific knowledge of power connections, power-up sequences, and some design techniques is required.

This application note captures recent measurements of different operating currents, leakage measurements, and provides recommended power network design techniques. This information is useful in power network systems that use i.MX application processors with the ARM920T core.

This document applies to the following i.MX devices, collectively called i.MX throughout:

- MC9328MX1
- MC9328MXL
- MC9328MXS

Contents

2 Modes of Operation

There are three different power modes supported by i.MX processors:

1. Run mode
2. Doze mode
3. Stop mode

These modes, when combined with the easily configured on-chip clocking system, provide developers with high flexibility to manage power consumption of their target system to achieve the best power efficiency. Figure 1 shows the i.MX system clocking scheme.

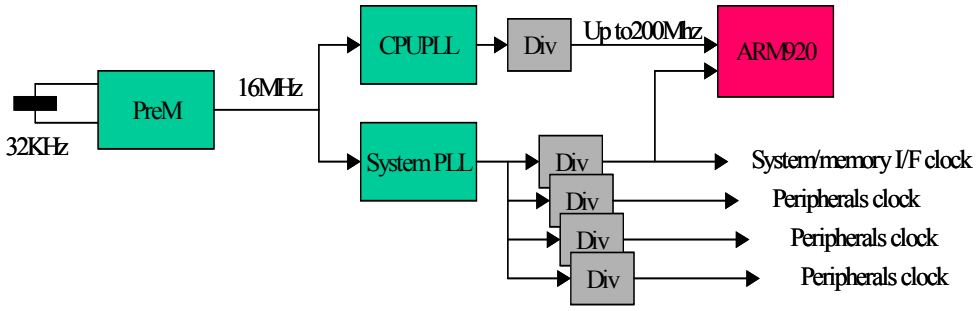

Figure 1. System Clocking Scheme

Typical i.MX power consumption data is provided in this section. Unless specified otherwise, the following data was obtained on the MC9328MX1 ADS board with NVDD, BTRFVDD, and AVDD set to 3.0V and QVDD set to 1.8V. For simplicity, NVDD, BTRFVDD, and AVDD are grouped together as "3V NVDD" in the measurement and QVDD is grouped as "1.8V VDD".

2.1 Run Mode Operation

In Run mode, the core is fully running, the CPU-PLL and System-PLL are turned on, their operation clock frequency can boost to 192 MHz and 96 MHz respectively, and the clock gating control from GCCR can be turned on. In a typical OS, Run mode is entered only from Doze or Stop mode, or immediately after Power-up. However, when all tasks are finished, the system is expected to leave Run mode and enter either Doze mode or Stop mode, with the exception of when RTC timer tasks are active.

Table 1 provides the measurement conditions and results for Run mode using embedded SRAM (eSRAM) and Table 2 provides the measurement conditions and results for Run mode using SDRAM.

Table 1. Run Mode with CPU in Fastbus Mode Using eSRAM

Measurement Conditions			
• CPU core in fastbus mode—that is, System clock = MCU clock = BCLK • MCU PLL disabled • System PLL = 96 MHz • PERCLK1 = PERCLK2 = 6 MHz • PERCLK3 = 750 kHz • All modules disabled except RTC and LCD controller • Sharp 320x240 16-bit TFT panel with picture data stored in on-chip • embedded SRAM (incomplete picture due to the size limit of eSRAM) (refresh rate = 60 Hz) • A Memory read/write program running on eSRAM			
System Clock (MHz)	**3V NVDD[1] (mA)**	**1.8V QVDD (mA)**	**Power (mW)**
16	2.1	13.7	31.0
32	2.1	23.4	48.4
48	2.1	33.5	66.6
96	2.1	62.7	119.2

1 NVDD, BTRFVDD, and AVDD are included under 3V NVDD.

Table 2. Run Mode with CPU in Fastbus Mode Using SDRAM

Measurement Conditions			
• CPU core in fastbus mode—that is, System clock = MCU clock = BCLK) • MCU PLL disabled • System PLL = 96 MHz • PERCLK1 = PERCLK2 = 6 MHz • PERCLK3 = 750 kHz • All modules disabled except RTC, LCD controller and SDRAM controller • Sharp 320x240 16-bit TFT panel with picture data stored in eSRAM (refresh rate = 60 Hz) • A Memory read/write program running on SDRAM			
System Clock (MHz)	**3V NVDD[1] (mA)**	**1.8V QVDD (mA)**	**Power (mW)**
16	11	14	57
32	14	29	95
48	17	37	119
96	30	66	209

1 NVDD, BTRFVDD, and AVDD are included under 3V NVDD.

2.2 Doze Mode Operation

Similarly, in Doze mode, the CPU core of the i.MX processor stops execution and enters a low-power state by executing a “wait for interrupt” instruction. It stays in the low-power state until an eligible interrupt wakes it up. The CPU-PLL can be shut down during Doze mode to provide further power savings. Example 1 shows a typical sequence to enter Doze mode.

The System-PLL continues to generate a clock in Doze mode to keep the required peripheral modules, such as the LCD controller, in operation. Additional power savings can be obtained during Doze mode through lowering the system clock speed by setting the system clock divider (BCLKDIV) to a higher

value. Adjusting the system clock does not affect the other peripherals, such as UART or USB, because they are driven by different clock paths.

For example, a system might have its CPU running at 200 MHz and its system clock at 96 MHz while in Run mode. When switched into Doze mode, the CPU stops execution and the system clock is lowered to 32 MHz to minimize power consumption, while maintaining the necessary functions (such as keeping the LCD on) in Doze mode. The system clock is required to maintain the data throughput for refreshing the LCD display during Doze mode. For an LCD of smaller size or color depth, a lower system clock may suffice for maintaining the display.

When the system enters Doze mode, the SDRAM controller, by default, continues to operate as if it is in Run mode. However, by programming the Clock Suspend Time-out (CLKST) bits of the SDRAM Control Register, the SDRAM can be put into clock suspend or power-down mode to provide further power savings. Refer to the SDRAM Memory Controller chapter of the MC9328MX1 or MC9328MXL reference manual for the detailed descriptions of the CLKST bits. (See Section 4, “References.”)

Again, in a typical OS, the system enters Doze mode if there are no more pending active tasks with the exception of the RTC timer. Normally the system is expected to switch to either Stop mode—after a fixed idle time, or Run mode—if an active task is executed, for example an interrupt from the touch panel.

Example 1 provides the programming sequence for Doze mode and Table 3 provides the measurement conditions and results for Doze mode using embedded SRAM (eSRAM) and Table 4 provides the measurement conditions and results for Doze mode using SDRAM.

Example 1. Doze Mode Programming Sequence

```
;disable MCUPLL by clearing the MPEN bit
        mov r1, #0x0021B000
        mov r2, #0xFFFFFFFE
        ldr r3,[r1,#0x0]
        and r2,r2,r3
        str r2,[r1,#0x0]

;put CPU to "wait for interrupt" state
        mcr p15,0,r1,c7,c0,4
```

Table 3. Doze Mode with LCD Displaying Data from Embedded SRAM

Measurement Conditions			
• Sharp 320x240 16-bit TFT panel with picture data stored in on-chip • Embedded SRAM (incomplete picture due to the size limit of eSRAM) (refresh rate = 60 Hz) • All modules disabled except RTC and LCD controller • MCU PLL disabled • System PLL = 96 MHz • PERCLK1 = 6 MHz • PERCLK2 = 16 MHz • PERCLK3 = 750 kHz			
System Clock (MHz)	**3V NVDD[1] (mA)**	**1.8V QVDD (mA)**	**Power (mW)**
16	1.9	10.9	25.3
32	1.9	17.4	37.0
48	1.9	23.5	48.0
96	1.9	42.3	81.8

1 NVDD, BTRFVDD, and AVDD are included under 3V NVDD.

Table 4. Doze Mode with LCD Displaying Data from SDRAM

Measurement Conditions			
• Sharp 320x240 16-bit TFT panel with picture data stored in SDRAM (refresh rate = 60 Hz) • All modules disabled except RTC, LCD controller & SDRAM controller • MCU PLL disabled • System PLL = 96 MHz • PERCLK1 = 6 MHz • PERCLK2 = 16 MHz • PERCLK3 = 750 kHz			
System Clock (MHz)	**3V NVDD[1] (mA)**	**1.8V QVDD (mA)**	**Power (mW)**
16	10.2	12.0	52.2
32	12.8	19.0	72.6
48	15.3	25.9	92.5
96	20.2	46.5	144.3

1 NVDD, BTRFVDD, and AVDD are included under 3V NVDD.

2.3 Stop Mode Operation

The i.MX processor attains the lowest power consumption in Stop mode with both the MCU PLL and the System PLL shut down. Only the 32 kHz clock is running. The CPU core and all the peripheral modules except the Real Time Clock (RTC) module are stopped to maximize the power savings.

The MCU PLL and the System PLL can be shut down by clearing the MPEN and UPEN bits of the Clock Source Control Register (CSCR). Upon clearing these bits, the MCU PLL is shut down immediately. Whereas, there is a delay before the System PLL shuts down. When the UPEN bit is cleared, the clock controller invokes a shut down counter, which is configured through the SD_CNT bits of CSCR. At the same time, it informs the SDRAM controller that the system is going into Stop mode. The SDRAM

controller then starts the self-refresh sequence after any in-progress SDRAM accesses are complete. After the SDRAM has safely entered self-refresh mode, the SDRAM controller acknowledges the system clock controller that it is ready to enter Stop mode. Only after receiving the acknowledgement and after the shut down counter times out, will the clock controller shut down the System PLL. Example 2 shows a typical sequence to enter Stop mode.

Example 2 provides the programming sequence for Stop mode and Table 5 provides the measurement conditions and results for Stop mode without external loading.

Example 2. Stop Mode Example Sequence

```
;disable both MCU and System PLLs by clearing MPEN & UPEN bits
         mov r1, #0x0021B000
         mov r2, #0xFFFFFFFC
         ldr r3,[r1,#0x0]
         and r2,r2,r3
         str r2,[r1,#0x0]

;MCU PLL will be shut down immediately while the System PLL will only
;shut down after the shut-down count times out (duration determined by
;shut-down Control (SD_CNT) setting of the Clock Source Control Register)
;put CPU to "wait for interrupt" state
         mcr p15,0,r1,c7,c0,4
```

Table 5. Stop Mode (with No External Loading)

Measurement Conditions		
• Measurement done on a special evaluation board with no memories and other external components. • MCU PLL and System PLL disabled • All GPIO pins set to input with pull-up or pull-down resistors enabled. • 32kHz clock still running		
3V NVDD[1] (mA)	**1.8V QVDD (mA)**	**Power (mW)**
0.001	0.025	0.0480

1 NVDD, BTRFVDD, and AVDD are included under 3V NVDD.

3 Power Characteristic

This section provides design techniques and processor usage to maximize the high-speed performance and ultra-low power benefits of the i.MX application processors.

3.1 DC Characteristic for i.MX Connections

Table 6 summarizes the voltage requirements for each voltage bank for the i.MX processors.

Table 6. Voltage Bank Requirements

Rating	Symbol	Minimum	Maximum	Unit
I/O supply voltage for Memory Bus and related control signals	$NVDD_1$	1.70	3.30	V
I/O supply voltage, JTAG, I^2C, CSI, PWM, TIMER, LCD, and CSI	$NVDD_2$	1.70	3.30	V

Table 6. Voltage Bank Requirements (continued)

Rating	Symbol	Minimum	Maximum	Unit
I/O supply voltage, SPI, UART1, and SSI	$NVDD_3$	1.70	3.30	V
I/O supply voltage, UART2, USBd, SIM, and MMC/SD/MS	$NVDD_4$	1.70	3.30	V
Internal supply voltage (Core = 150 MHz)	QVDD	1.70	1.90	V
Internal supply voltage (Core = 200 MHz)	QVDD	1.80	2.00	V
Analog supply voltage (System)	$AVDD_1$	1.70	3.30	V
Bluetooth I/O voltage (Bluetooth)	BTRFVDD	1.70	3.10	V
Bluetooth I/O voltage (Non Bluetooth applications)	BTRFVDD	1.70	3.30	V

3.2 Power-Up Sequence

Because the silicon of the i.MX processors support multiple voltage banks, an exact power-up sequence is required to avoid leakage via the inner ESD structure. Use the following sequence in your design.

General Silicon Power-Up Sequence:

The power-up sequence begins with the highest voltage bank first, followed by the next highest, with the lowest voltage bank powering up last.

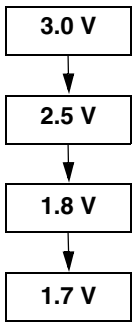

Figure 2. Power-Up Sequence

General Silicon Power-Down Sequence:

The power-down sequence begin with the lowest voltage bank powering down first, followed by the next lowest, with the highest voltage bank powering up last.

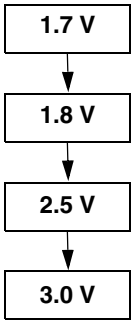

Figure 3. Power-Down Sequence

3.3 Minimizing Leakage

Freescale recommends that users follow standard practice for connection techniques on the PCB during system development.

3.3.1 ESD Leakage During Power-Up and Power-Down

In Freescale Semiconductor's silicon design structure, the ESD network is constructed within each power bank. Incorrect power sequence can lead to a forward bias of the ESD diodes, and can result in a large amount of current drawn via the Power or I/O connections to GND.

Users are required to power the Voltage Banks (NVDD*x*, BTRFVDD, AVDD*x* and QVDD) from the highest level of voltage to the lowest level. For example, from 3.0V to 1.8V.

IMPORTANT:

FROM: **Bank with Highest voltage,** *TO:* **Bank with Lowest voltage.**

3.3.2 i.MX Connection Clamp Diode Leakage

Generally, no voltage is applied to any of the I/Os on the silicon before the silicon is powered because the path is equivalent to a forward bias of internal ESD to GND. In this situation, a single connection can possibly consume 300mA if 2.7V is applied on the connection pin where the NVDD is 0V or at small resistance to GND. In fact, the same phenomenon occurs to all ESD protected components. As previously explained, a single connection can draw 300mA. Improper system power network design can damage the board or components.

IMPORTANT:

Avoid or Minimize the Power-delay between connected components.

3.3.3 i.MX Connection Leakage due to Unstable State During Power-Up

i.MX processors have a leakage issue during power-up. Before the ARM920T core is powered-up, internal logic to control the input connection circuits is not initiated. Therefore, following the recommended power-up sequence can cause an input connection tied directly to GND to draw 75 mA for the period before QVDD achieves 1.8 V. Consequently, six inputs tied to directly to GND can lead to a current drain of 450 mA during power up.

IMPORTANT:

Always terminate unused inputs that require logic 0 with a 1 kΩ pull-down resistor to GND. This limits the undesirable current drain.

For i.MX processors, three inputs that require external termination are as follows:

- BOOT[3:0]
- TRISTATE
- BIG_ENDIAN

3.3.4 Idd Leakage

In STOP mode, a floating input such as a GPIO, BOOT[3:0], TRISTATE, or BIG_ENDIAN can increase standby current from < 30 uA to ~ 1.2 mA. The system designer must ensure that no input is floating. To do this, use the on-chip pull-up resistor for an input GPIO or program the GPIO as an output. Terminate BOOT[3:0], TRISTATE, and BIG_ENDIAN per section 3.3.3.

IMPORTANT:

Do not allow i.MX inputs to float.

3.3.5 Input / Analog Connection/eSRAM Leakage

Input and Analog connections can consume approximately <1uA per connection, and eSRAM can draw approximately 30mA before the internal system reset initialization is complete. This requires the workaround by eSRAM access.

3.3.6 Leakage Over JTAG Port–TDO

Per the JTAG specification, JTAG output enable (TDO enable) is not enabled at all times. The TDO output is driven in the Shift-DR and Shift-IR controller states of the TAP controller state machine. When the JTAG output is not enabled, TDO is OFF and tristated. Therefore, it is recommended to either pull-up or pull-down this pin.

4 References

The following documents are recommended for a complete description of the i.MX applications processors and are necessary to design properly with the device. These documents may be found at the Freescale Semiconductor World Wide Web site at http://www.freescale.com/imx. These documents may be downloaded directly or printed versions may be ordered.

MC9328MX1 Data Sheet (order number MC9328MX1)

MC9328MX1 Reference Manual (order number MC9328MX1RM)

MC9328MXL Data Sheet (order number MC9328MXL)

MC9328MXL Reference Manual (order number MC9328MXLRM)

MC9328MXS Data Sheet (order number MC9328MXS)

MC9328MXS Reference Manual (order number MC9328MXSRM)

Power Performance of MC9328MX1 (order number AN2501)

5 Document Revision History

Table 7 summarizes revisions to this document since Rev. 2.

Table 7. Revision History

Location	Revision
Table 1 through Table 5	Changed unit of measure for Power from mA to mW.
Section 3.2, “Power-Up Sequence,” on page 7	Replaced Power Up and Power Down numbered list sequences with sentences and figures 2 and 3.
Section 3.3.6, “Leakage Over JTAG Port–TDO,” on page 9	Added this section to document.
Table 6	Removed Analog supply voltage from table.

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Rev. 3
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