Application Note

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Using PLL to Indicate Oscillator Start-Up Performance during Power On Reset

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Introduction

Customers have reported problems that have been traced to slow oscillator start-up performance.

If the oscillator is not stable when Reset is released, the MCU will exit Power on Reset in Limp Home Mode. It is possible for the device to prematurely indicate that the oscillator has stabilised, thereby releasing the part from Limp Home Mode to the oscillator clock with an unstable oscillator. Where this occurs, the duty cycle of the oscillator clock may not be 50% giving insufficient time for data or address values to be latched correctly. Under these conditions code runaway or inadvertent erasure of memory is possible.

One way to avoid this is for customers to measure the time taken for their oscillator to stabilise and ensure that the Reset pin is held low for a sufficiently long time to allow stabilisation to occur and avoid the MCU starting in Limp Home Mode.

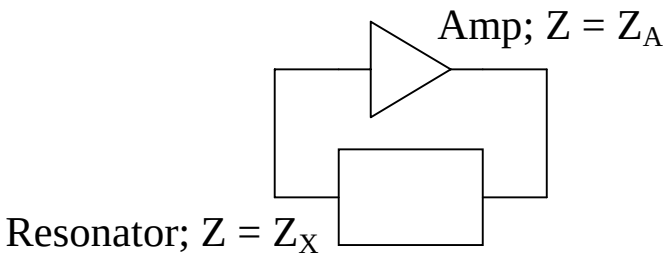
The oscillator circuitry on the HC12 D family is sensitive to excess capacitance, making it difficult for customers to investigate the start-up behaviour of their oscillators during power on reset without disturbing the characteristics of the very parameter they seek to observe. This document offers an alternative approach to monitor the start-up performance of the oscillator within an application.

Explanation

The HC12 D family oscillator specification requires lower power consumption than the traditionally used Pierce oscillator. This resulted in the use of a low power Colpitts oscillator design.

The stability of the Colpitts oscillator is more susceptible to the effects of stray capacitance and as such care must be taken to reduce this during PCB layout design and component selection. This susceptibility also extends to the stray capacitance induced when a scope probe is attached to EXTAL in order to monitor oscillator start-up.

Oscillator circuits can be viewed as a loop with a feed forward portion (amplifier) and a feedback portion (the crystal).



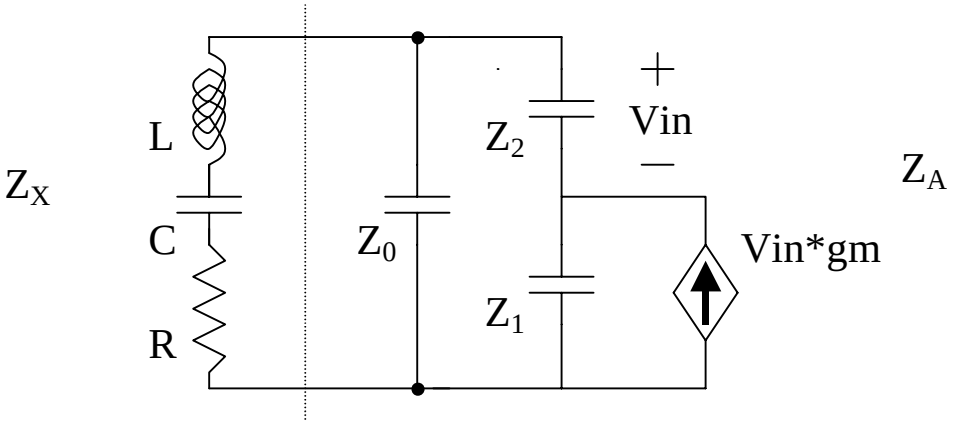
For sustained oscillation, oscillator circuits must meet the following criterion:

- The loop phase must be 360 degrees (or integer multiple thereof)
- The loop gain must be unity (>1 for start-up)

The resonator or crystal network will provide about 180 degrees of phase shift at resonance. The amplifier and its components must provide the other 180 degrees. These criteria can be expressed mathematically as:

$$Z_A + Z_X = 0 \quad \text{or} \quad -Z_A = Z_X$$

The basic oscillator implementation's small signal circuit is shown below. To a first order, the parasitic resistances (device output resistance, bias resistance, and pin leakage) are ignored. The impedance of the circuit (Z_A) can be expressed as a function of transconductance and the three major impedances - Z_0, Z_1, and Z_2. First order analysis assumes these impedance's are lossless (caps).

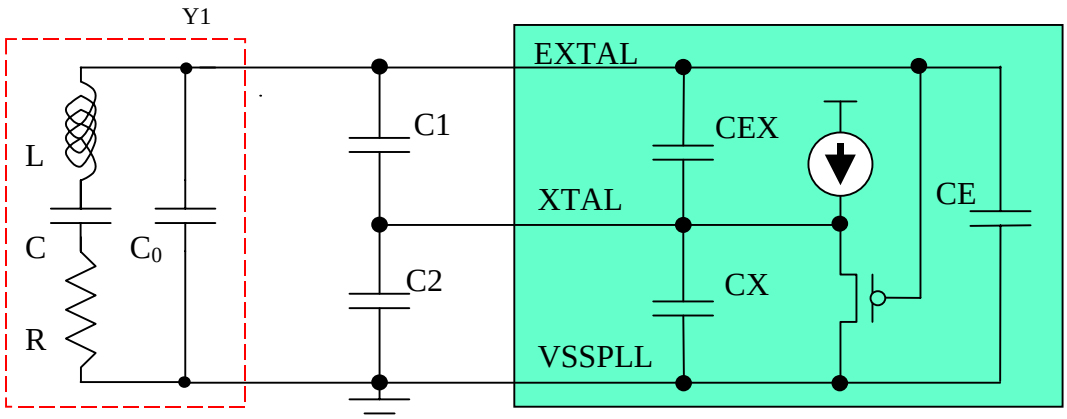


If the real parts of the impedance's are considered; one gets:

$$-R(Z_A) = R(Z_X)$$

If $-R(Z_A) > R(Z_X)$ then oscillation grows. If $-R(Z_A) < R(Z_X)$ then oscillation decays.

If we now introduce the parasitic capacitance between the EXTAL, XTAL and VSSPLL pins, the HC12 oscillator circuit can be approximated by the following diagram:



In this instance Z_0, = C_' = C_ + CE, Z_1 = C_' = C_ + CEX, and Z_2 = C_' = C_ + CX.

The capacitance component of Z_0 has increased which will in effect decrease the impedance of $R(Z_A)$ thus reducing the growth of oscillations.

It is now apparent that putting an oscilloscope probe across EXTAL and VSSPLL to monitor the crystal start-up will add to the capacitance of C_0 and therefore further reduce $R(Z_A)$ causing an even greater adverse effect on oscillation growth.

Thus to monitor oscillator start-up performance either special high impedance / low capacitance probes will be required (expensive and not readily available) or an alternative non-intrusive means must be found.

Solution

When a Power On Reset occurs, a 4096 cycle oscillator start-up delay is imposed before the Reset recovery sequence commences. During this 4096 cycle delay, Reset is held low internally by the MCU.

The reset recovery sequence will not commence if the 4096 cycle delay has not been completed or the Reset pin is held low externally.

Assuming that VDDPLL is tied to VDD, then the 13-stage counter which controls the 4096 cycle delay is initially clocked by the VCO at its limp home frequency, until the oscillator is detected (Limp Home Mode).

When the clock monitor detects the presence of an external clock on the EXTAL pin, then Limp Home Mode is de-asserted and the 13-stage counter is clocked by EXTAL. This can occur during the 4096 cycle count or at any later stage. If Limp Home Mode is de-asserted during the 4096 cycle delay, then it is probable but not guaranteed that the MCU will come out of Reset with a stable clock.

(The clock monitor can be misled by EXTAL into reporting a good signal before it has fully stabilised. The clock monitor only detects oscillations at the input to EXTAL; it does not measure quality.)

If Limp Home Mode is still asserted when the MCU exits Reset then the oscillator start-up is too long and there is no stable clock available thus risking code runaway.

The PLL will only achieve lock when the MCU is not in reset and a stable clock is present, i.e. when the MCU is not in Limp Home Mode It is therefore possible to use the PLL as an indication of the quality of the oscillator at Reset.

To do this it is necessary to calculate the estimated PLL lock time for the XFC components used in the application, and measure the time from the release of Reset till PLL Lock is achieved. If this measurement is significantly greater than the PLL lock time, then it may be assumed that the oscillator was not stable at the time reset was released and that the customer runs a risk of code runaway.

Root cause fix

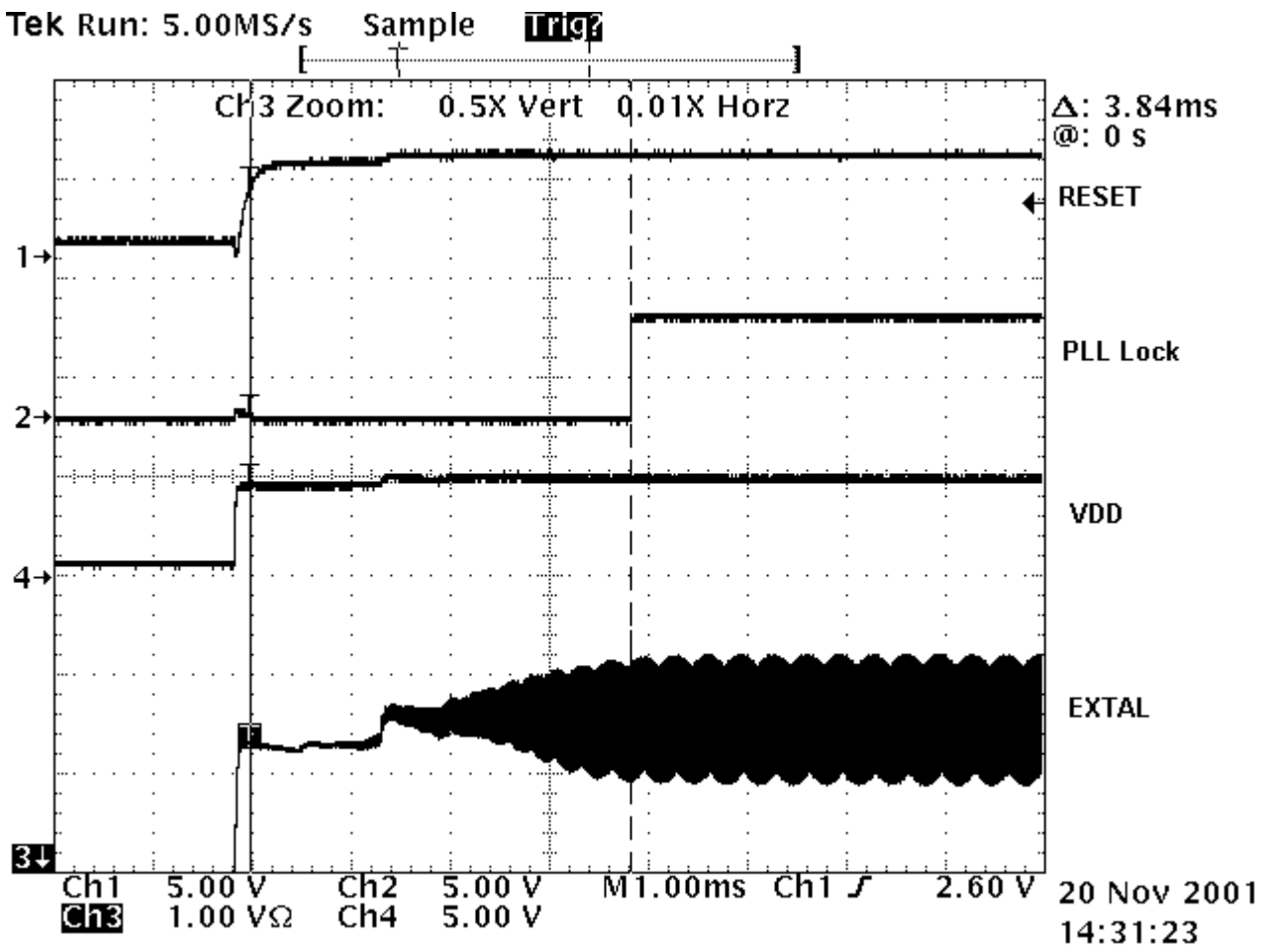
The quickest and easiest way to allow the PLL to lock in a controlled manner is to allow it to use it's default settings after reset to synthesize the oscillator frequency i.e. SYNR = REFDV = $00, PLLCR = $60 (AUTO = 1, PLLON = 1).

The status of the LOCK bit in PLLFLG can be monitored via any available port pin. The LHOME bit can be monitored in a similar manner if so desired. The following code gives an example of how to achieve PLL Lock and monitor the LOCK and LHOME bits.

```
main()
{
            Regs.porta.byte = 0x00;       // Initialise PORT a to 0
            Regs.porte.byte = 0x00;       // Initialise PORT e to 0
            Regs.ddra.byte = 0x01;        // PA0 = output
            Regs.ddre.byte = 0x80;        // PE7 = output
            Regs.rtictl.byte = 0x20;      //Disable the RTI watchdog
            while(1)
            {
                        Regs.porte.bit.pe7 = Pll.pllflg.bit.lhome;
                        Regs.porta.bit.pa0 = Pll.pllflg.bit.lock;
            }
}
```

This code should be downloaded into the application and the appropriate port pins plus Reset monitored.

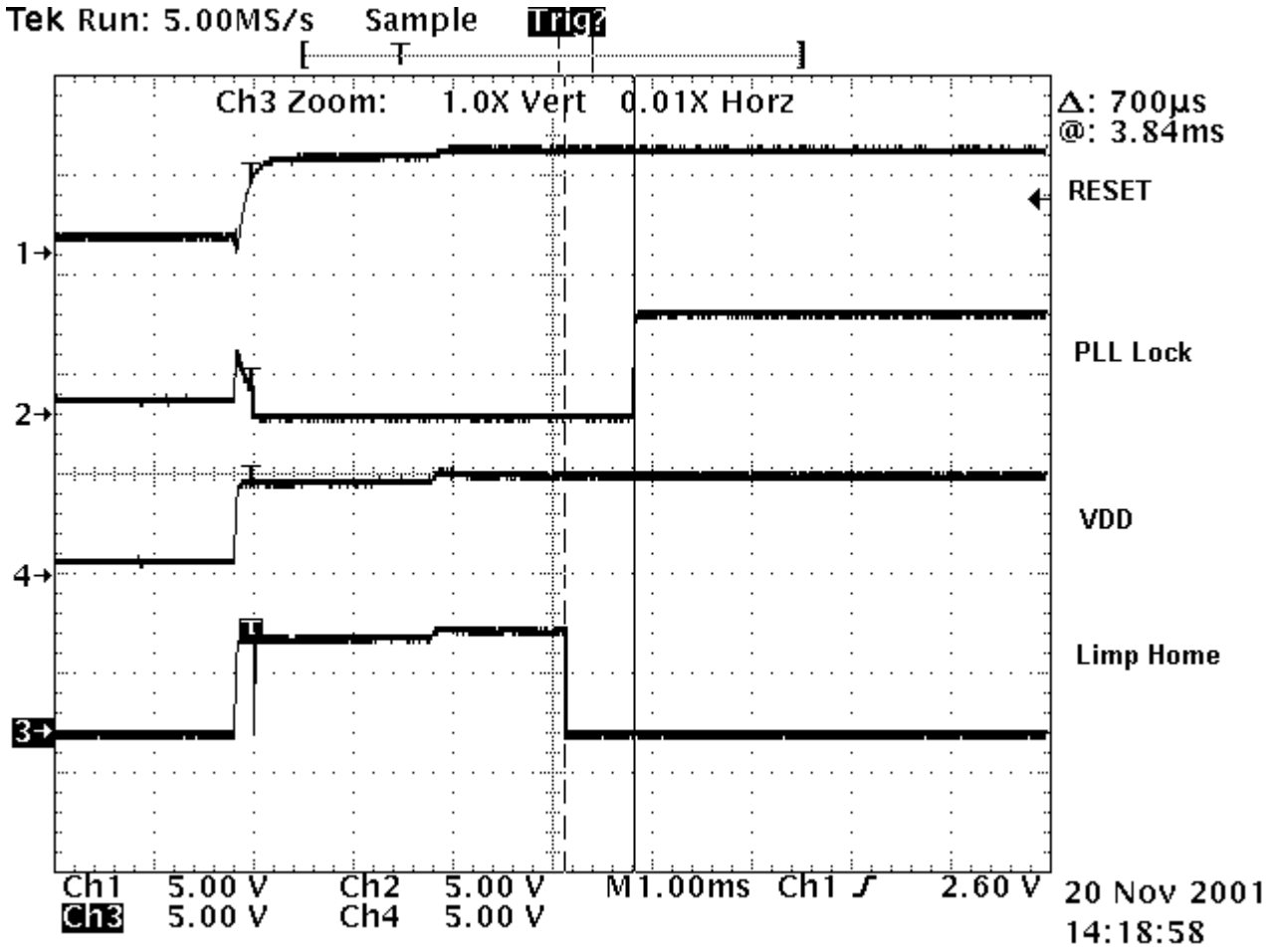
The following scope trace shows an example of a poor oscillator start-up, caused by the premature release of Reset after VDD has been applied. In the example, a 4MHz crystal was used in conjunction with a DG128. The components on the XFC pin were a 3K3 resistor and a 10nF and 1nF capacitors. For these components the estimated PLL Lock time is approximately 0.74mS.



In this scope trace, Reset is released almost immediately after VDD. The scope trace clearly shows that the oscillator has not started when Reset is released, thus the MCU is in Limp Home Mode.

As the MCU is running in Limp Home Mode the PLL will have to wait until Limp Home Mode has been de-asserted (LHOME bit =0) before it can attempt to lock. Thus we would expect the time from the release of Reset to PLL Lock to be greater than the calculated lock value of 0.74mS, which it is, indicating that the oscillator start-up in this case shows a poor performance.

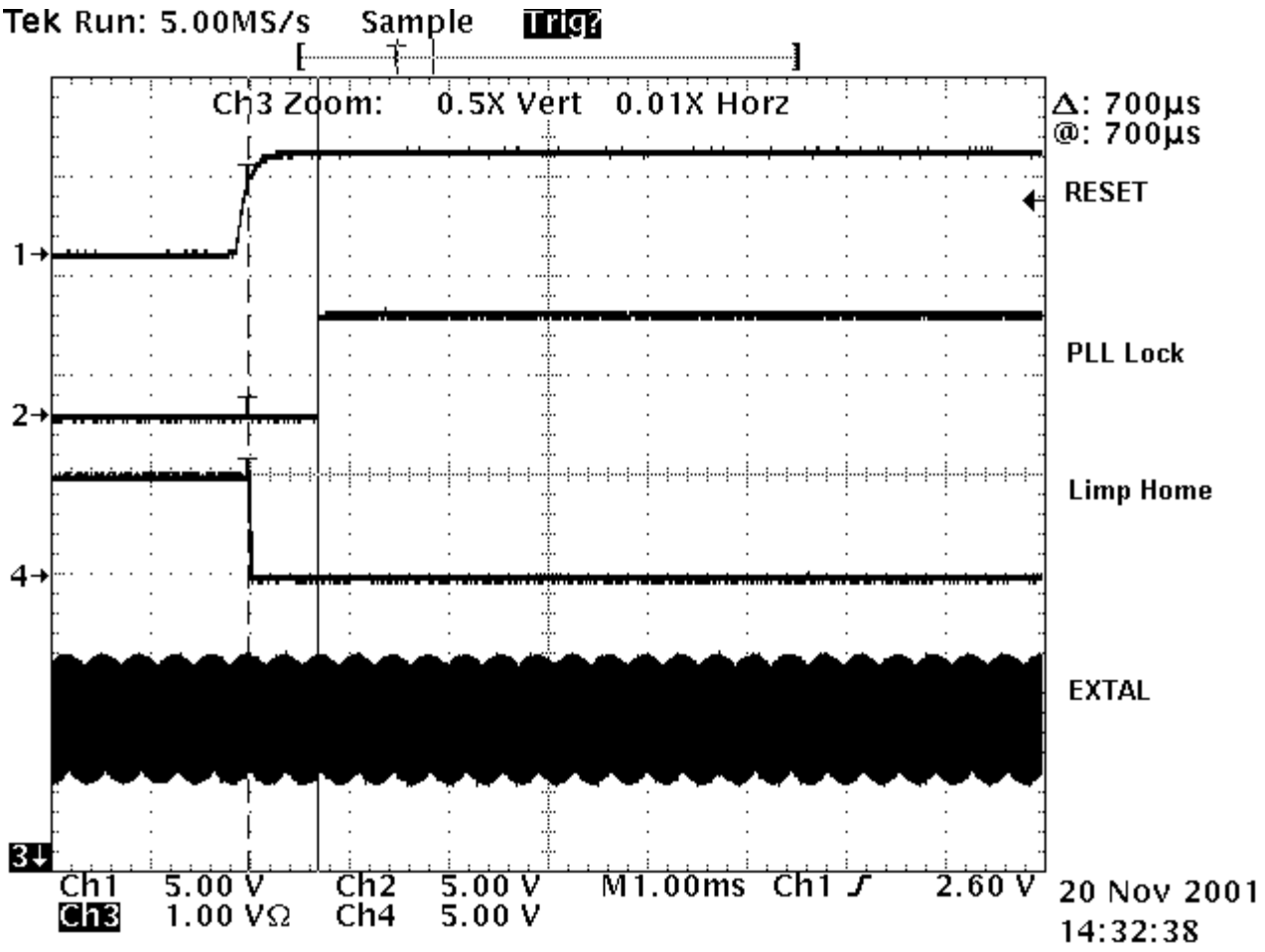
The next scope trace shows the same conditions again, but this time the status of the LHOME bit is monitored instead of EXTAL.



This trace shows where Limp Home Mode is de-asserted. We cannot tell from the scope trace whether Limp Home Mode was de-asserted either during or after the 4096 cycle delay. We can see from this trace that the PLL achieves lock 0.7mS after the MCU exits Limp Home Mode. This suggests that the oscillator signal at EXTAL was stable when Limp Home Mode was de-asserted, as the PLL Lock time was estimated at 0.74mS.

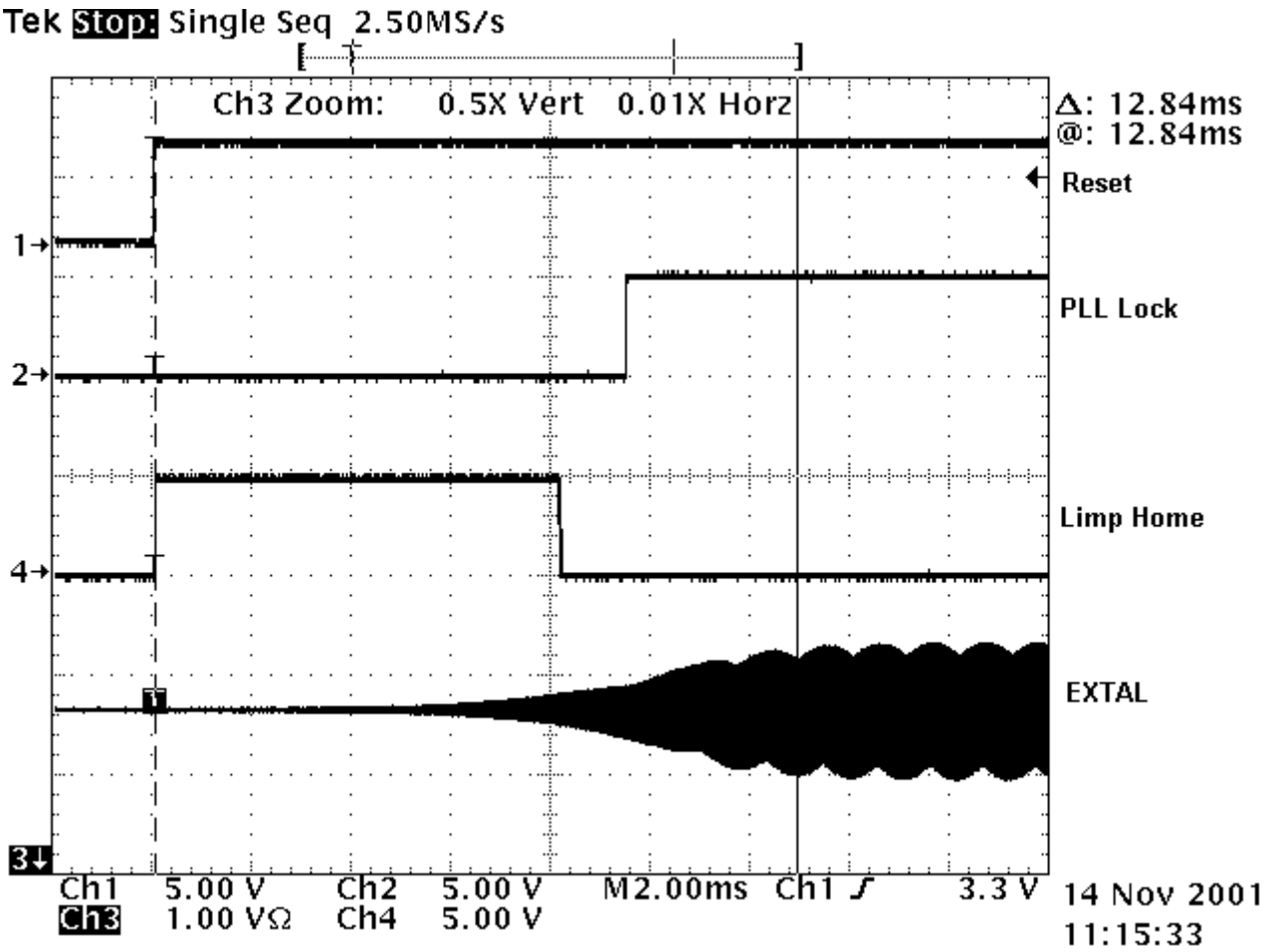
(The module used in this evaluation was an oscillator test board, designed to optimise oscillator start-up. Thus in the two previous scope traces, the oscillator was stable before the 4096 cycle delay completed, and the de-assertion of Limp Home Mode coincides with the internal MCU release of reset at the end of the 4096 cycle delay. The PLL would therefore start to track it's target frequency from this point, and attain lock in approximately 0.74mS)

Using the same hardware set-up as before, Reset is held low externally, until the oscillator is stable. This is an example of a good oscillator start-up.



In this trace Reset has been held low externally for a sufficiently long time to allow the oscillator to become stable, and the internal 4096 cycle delay to be completed. Here the PLL achieves lock very quickly, in almost the exact time predicted by the PLL lock time calculation. This indicates that the oscillator start-up exhibits a good performance.

The final scope trace is from an actual customer application, which was proven to exhibit poor oscillator start-up. In this customer's application, the PLL lock time was estimated at 2.3mS, the POR delay was 13mS and the oscillator had been was shown to stabilise approximately 7.6mS after the release of Reset.



The trace shows that the time from the release of the Reset pin till PLL lock is about 9.5mS, far greater than the calculated 2.3mS. Even without the advantage of being able to observe the EXTAL signal, the Reset – PLL Lock measurement clearly indicates that the application has oscillator start-up issues which merit further investigation.

Remarks

This technique is not intended to be a substitute for a full and proper investigation using high impedance / low capacitance scope probes. It does however provide a quick indication of oscillator start-up performance, which can be measured using standard probes without interfering with the oscillator start-up.

An estimate of the approximate PLL Lock time for the HC12 D family can be calculated using the following equation:

Tlock[mS] = 0.057 x C x exp((Fbus-1.675)/10.795) + 0.128/Fextal

Where –

C is the main filter series capacitor in nF
Fbus is the internal bus frequency in MHz
Fextal is the oscillator frequency in MHz
This equation is valid for REFDV = $00, and VDD = 5V.

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