Application Note

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Differences Between the HC908AZ60A and the HC908AZ60

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Introduction

The purpose of this document is to help customers to transfer from the 0.65µ HC908AZ60 to the HC908AZ60**A** (0.5µ device). It highlights the differences between the devices, gives two methods for detecting which device is present as well as providing a checklist to help with code development.

The main difference between the devices is that the HC908AZ60A is constructed from a newer non-volatile memory (NVM) technology. However, it is important that the user should consider all differences when developing code that is to be used on both the HC908AZ60A and the HC908AZ60.

Differences between the HC908AZ60A and the HC908AZ60

This section describes the differences between the HC908AZ60A and the HC908AZ60. Each affected module is listed along with a summary of the changes.

FLASH

This section discusses the main differences between the Flash module on the HC908AZ60A versus the HC908AZ60. For a detailed explanation of the Flash on the HC908AZ60A the user is advised to consult Application Note AN2156/D entitled ‘Programming and Erasing FLASH and EEPROM Memories on the MC68HC908AS60A/AZ60A’. AN2156/D explains in detail how to program and erase the HC908AZ60A Flash module. Additionally, the user should refer to the Flash section of the latest MC68HC908AZ60A Specification for programming and erasing algorithm details.

Flash Architecture

On the HC908AZ60A and HC908AZ60 devices, code is stored in non-volatile electrically erasable and programmable memory, Flash.

The HC908AZ60A Flash is constructed from a newer NVM technology and is arranged in pages of 128 bytes with 2 rows per page. Programming is carried out on a row (64 bytes) at a time. The minimum erase operation applies to a page (128 bytes) of memory.

The HC908AZ60 is arranged in rows of 64 bytes with 8 pages per row. This programming is carried out on a page (8 bytes) at a time. The minimum erase operation applies to a row (64 bytes) of memory.

Note that the definition of page and row sizes is different between HC908AZ60A and HC908AZ50.

Flash Control Registers

Flash-1 control register (FLCR1 or FL1CR) is located at address $FE0B on the HC908AZ60 but is located at address $FF88 on the HC908AZ60A. Flash-2 control register (FLCR2 or FL2CR) is located at address $FE11 on the HC908AZ60 but is located at address $FE08 on the HC908AZ60A. Bits [4:7] of these registers are no longer used on the HC908AZ60A. This is because clock control for the flash charge pump is achieved automatically on this device and erasing of variable block sizes is replaced by the MASS bit. Bit 2 of these registers has a different function on the HC908AZ60A – it controls a mass (bulk) or a page erase operation. On the HC908AZ60 it activates ‘margin read’ operation.

HC908AZ60A Registers

FL1CR	Bit 7	6	5	4	3	2	1	0
$FF88	**0**	**0**	**0**	**0**	HVEN	**MASS**	ERASE	PGM
Reset:	0	0	0	0	0	0	0	0

FL2CR	Bit 7	6	5	4	3	2	1	0
$FE08	**0**	**0**	**0**	**0**	HVEN	**MASS**	ERASE	PGM
Reset:	0	0	0	0	0	0	0	0

HC908AZ60 Registers

FLCR1	Bit 7	6	5	4	3	2	1	0
$FE0B	**FDIV1**	**FDIV0**	**BLK1**	**BLK0**	HVEN	**MARGIN**	ERASE	PGM
Reset:	0	0	0	0	0	0	0	0

FLCR1	Bit 7	6	5	4	3	2	1	0
$FE11	**FDIV1**	**FDIV0**	**BLK1**	**BLK0**	HVEN	**MARGIN**	ERASE	PGM
Reset:	0	0	0	0	0	0	0	0

FDIV[1:0] — Frequency Divide Control Bits select the factor by which the charge pump clock is divided from the system clock.

BLK[1:0] — Block Erase Control Bits allow erasing of blocks of varying size.

Flash Programming Procedure

Programming the Flash module on the HC908AZ60A is similar to programming the HC908AZ60 Flash module. However, an extra dummy write operation to any address in the page is required prior to programming data into one of the two rows in the page. Margin reading of programmed data is no longer required.

Flash Programming Time

The byte programming time on the HC908AZ60A is 30 to 40µs which is significantly less than the byte programming time on the HC908AZ60.

Flash Block Protection

The range of protection on the HC908AZ60A has increased. The Flash block protection registers on the HC908AZ60A are 8-bit registers and array protection ranges can be incremented 1 page (128 bytes) at a time with the smallest block being 256 bytes. The HC908AZ60 uses 4 bits of the Flash block protection registers and array protection ranges can be incremented 8k bytes at a time. The user is advised to read the Flash Block Protection section of the latest MC68HC908AZ60A specification for more details of Flash block protection.

HC908AZ60A Registers

FL1BPR	Bit 7	6	5	4	3	2	1	0
$FF80	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
Reset:	0	0	0	0	0	0	0	0

FL2BPR	Bit 7	6	5	4	3	2	1	0
$FF81	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
Reset:	0	0	0	0	0	0	0	0

HC908AZ60 Registers

FLBPR1	Bit 7	6	5	4	3	2	1	0
$FF80	0	0	0	0	BPR3	BPR2	BPR1	BPR0
Reset:	0	0	0	0	0	0	0	0

FLBPR2	Bit 7	6	5	4	3	2	1	0
$FF81	0	0	0	0	BPR3	BPR2	BPR1	BPR0
Reset:	0	0	0	0	0	0	0	0

Also, on the HC908AZ60A the high voltage (V_{HI}) is no longer needed on the $\overline{IRQ}$ pin to program or erase the Flash block protect registers.

Flash Endurance

The FLASH endurance for the HC908AZ60A has increased to 10,000 write/erase cycles whereas the HC908AZ60 is specified at 100 write/erase cycles.

EEPROM

This section will concentrate on the operation of the HC908AZ60A EEPROM module, which is made from a newer NVM technology as the Flash but with a physical control layer to enable byte equations. HC908AZ60A EEPROM read operations remain the same as for the HC908AZ60, however, program and erase operations are a super-set of the current HC908AZ60 algorithm. Also, Application Note AN2156/D entitled 'Programming and Erasing FLASH and EEPROM Memories on the MC68HC908AS60A/AZ60A' discusses the EEPROM on the HC908AZ60A in detail.

Each of the HC908AZ60A EEPROM modules contains 2 new registers that must be set up correctly before any attempt is made to program or erase the EEPROM. The new registers are required to provide the EEPROM with a constant timebase of 35µs from the user's oscillator frequency. It should be noted that EEPROM-2 configuration register (EE2CR) is located at address $FF7D on the HC908AZ60A but on the HC908AZ60 this register is located at address $FE19. Also, EEPROM-2 array configuration register (EE2ACR) is located at address $FF7F on the HC908AZ60A as opposed to address $FE1B on the HC908AZ60 and EEPROM-2 non-volatile register (EE2NVR) is located at address $FF7C on the HC908AZ60A but address $FE18 on the HC908AZ60.

It is important to spend time gaining familiarity with the new HC908AZ60A EEPROM as it is essential that the EEPROM module is set up correctly before any program or erase operations are called. Failure to do so could cause premature wear out of the EEPROM or could result in improper programming/erasing of the EEPROM.

The basic programming and erase operations for the EEPROM on the HC908AZ60 and the EEPROM on the HC908AZ60A are the same. Also, bit polarity is the same with the programmed state being a logic 0 and the erased state a logic 1. The user is advised to consult the latest MC68HC908AZ60 and MC68HC908AZ60A specifications for details of program and erase algorithms.

The HC908AZ60A EEPROM requires a constant timebase source for program and erase operations. The clock source that is required to drive the EEDIV clock divider input must first be selected using bit-7 in the CONFIG-2 register at address $FE09. Secondly, the divide ratio from this source has to be set up for each 512 byte EEPROM module by programming an 11-bit time base pre-scalar into the divider registers, EExDIVH and EExDIVL (where x is 0 or 1 depending on which EEPROM module is selected). These registers must be programmed with a proper value before starting any EEPROM erase or programming steps. The function of the divider is to provide a constant clock source with a period of 35µs (within ± 2µs) to the internal timer and related EEPROM circuits for proper program or erase operations. The recommended frequency range of the reference clock is 250KHz to 16MHz.

The EEDIV value is calculated by the following formula:

$$EExDIV = INT[Reference\ Frequency(Hz) \times 35 \times 10^{-6} + 0.5]$$

The result is rounded down to the nearest integer value.

For example, if the Reference Frequency is 4.9152MHz, the EEDIV value in the above formula will be 172. To examine the time base output of the divider, the Reference Frequency is divided by the calculated EEDIV value (172), which equals to 28.577KHz in frequency or 34.99µs in period.

The user must exercise caution when setting up the divide ratio – EExDIVH and EExDIVL are volatile registers. They have duplicate non-volatile registers, EExDIVHNVR and EExDIVLNVR whose contents are loaded into EExDIVH and EExDIVL upon reset. One of the following 2 options could be used to set up EExDIV:

Option 1:

1. If the device is a HC908AZ60A – EExDIVHNVR and EExDIVLNVR are write once non-volatile registers unaffected by reset, therefore the user can write the divider value that they would like downloaded into EExDIVH and EExDIVL every time the device is reset into EExDIVHNVR and EExDIVLNVR with their s-record. Once, these registers are set up the user no longer needs to consider EExDIV in their programming routine.

Option 2:

1. Software detects which device is present and if the device type is HC908AZ60A, complete steps 2 and 3 otherwise continue as normal. **Figure 1** and **Figure 2** on page 10 show methods for performing the device detection.
2. In the user's initialisation routine that is called every time the device is reset and before any EEPROM program or erase operations are attempted, write the required divider value into EExDIVH and EExDIVL.
3. Ignore the non-volatile EExDIVHNVR and EExDIVLNVR registers. After a reset, the initialisation routine will be executed and the required divider value will be written into EExDIVH and EExDIVL. This will overwrite the default value of $FF that was downloaded upon reset from EExDIVHNVR and EExDIVLNVR.

NOTE: *The EExDIVH and EExDIVL registers are shown below and it should also be noted that Bit-7, EEDIVSECD, of EExDIVH (and EExDIVHNVR) controls EEPROM security. If this bit is programmed to 0 after system reset the security feature is permanently enabled and the divider value in the EEDIV registers cannot be changed.*

EE1DIVH	Bit 7	6	5	4	3	2	1	0
$FE1A	**EEDIVSECD**					EE1DIV10	EE1DIV9	EE1DIV8
Reset:	EE1DIVHNVR	X	X	X	X	EE1DIVHNVR	EE1DIVHNVR	EE1DIVHNVR

EE1DIVL	Bit 7	6	5	4	3	2	1	0
$FE1B	EE1DIV7	EE1DIV6	EE1DIV5	EE1DIV4	EE1DIV3	EE1DIV2	EE1DIV1	EE1DIV0
Reset:	EE1DIVLNVR	EE1DIVLNVR	EE1DIVLNVR	EE1DIVLNVR	EE1DIVLNVR	EE1DIVLNVR	EE1DIVLNVR	EE1DIVLNVR

EE2DIVH	Bit 7	6	5	4	3	2	1	0
$FF7A	**EEDIVSECD**					EE2DIV10	EE2DIV9	EE2DIV8
Reset:	EE2DIVHNVR	X	X	X	X	EE2DIVHNVR	EE2DIVHNVR	EE2DIVHNVR

EE2DIVL	Bit 7	6	5	4	3	2	1	0
$FF7B	EE2DIV7	EE2DIV6	EE2DIV5	EE2DIV4	EE2DIV3	EE2DIV2	EE2DIV1	EE2DIV0
Reset:	EE2DIVLNVR	EE2DIVLNVR	EE2DIVLNVR	EE2DIVLNVR	EE2DIVLNVR	EE2DIVLNVR	EE2DIVLNVR	EE2DIVLNVR

The HC908AZ60A EEPROM also contains a new feature selected via an AUTO bit in the EEPROM control registers (EE1CR at address $FE1D for EEPROM module 1 and EE2CR at address $FF7D for EEPROM module 2). Setting bit-1 of these registers (which is an unused bit in the HC908AZ60 EECR1 and EECR2) enables the AUTO function. The AUTO function enables significantly faster programming/erasing of the EEPROM by allowing the logic of the MCU to automatically use the optimum programming or erasing time for the EEPROM. Using the AUTO function means that the user does not need to wait for the normal minimum specified programming or erasing time. After setting the EEPGM bit as normal the user just has to poll that bit again, waiting for the MCU to clear it indicating that programming or erasing is complete. This feature is not available on the HC908AZ60. Therefore, if code is to be compatible with both devices, the user should first detect which device is present (**Figure 1** and **Figure 2** show methods for performing this task) and then only use the AUTO feature if the device type is HC908AZ60A.

Selective Bit Programming

The EEPROM can be programmed such that one or multiple bits are programmed (written to a logic 0) at a time. However, the user may never program the same bit location more than once before erasing the entire byte. In other words, the user is not allowed to program a logic 0 to a bit that is already programmed (bit state is already logic 0).

For some applications it might be advantageous to track more than 10K events with a single byte of EEPROM by programming one bit at a time. For that purpose, a special selective bit programming technique is available. An example of this technique is illustrated in **Table 1**.

Table 1. Example Selective Bit Programming Description

Description	Program Data in Binary	Result in Binary
Original state of byte (erased)	n/a	1111:1111
First event is recorded by programming bit position 0	1111:1110	1111:1110
Second event is recorded by programming bit position 1	1111:1101	1111:1100
Third event is recorded by programming bit position 2	1111:1011	1111:1000
Fourth event is recorded by programming bit position 3	1111:0111	1111:0000
Events five through eight are recorded in a similar fashion		

Note that none of the bit locations are actually programmed more than once although the byte was programmed eight times.

When this technique is utilized, a program/erase cycle is defined as multiple program sequences (up to eight) to a unique location followed by a single erase operation.

Configuration Registers

The HC908AZ60 and the HC908AZ60A use two configuration registers (Config-1 and Config-2) which need to be written by the user to select the required options. The configuration registers are write-once registers. Out of reset the configuration registers will read their default values. Once these registers have been written to, further writes will have no effect until a reset occurs.

Config-2 Register

The HC908AZ60A has two new active bits in its Config-2 register (located at address $FE09 for both devices). Bit-7 is particularly important when writing to the EEPROM.

HC908AZ60 Register

Config-2	Bit 7	6	5	4	3	2	1	0
$FE09	**0**	0	0	MSCAND	**0**	0	0	AZxx
Reset:	0	0	0	1	0	0	0	0

Bit-0 (AZxx) is used to configure the device as a ‘AZ’ device and should be set to a ‘1’ by the user.

Bit-4 (MSCAND) is used to disable the MSCAN module. When set to a ‘1’ the MSCAN module is disabled.

HC908AZ60A Register

Config-2	Bit 7	6	5	4	3	2	1	0
$FE09	**EEDIVCLK**	R	R	MSCAND	**AT60A (read only)**	R	R	AZxx
Reset:	0	0	0	1	1	0	0	0

R = Reserved

Bit 0 and bit 4 are the same as for the HC908AZ60. The following bi descriptions refer to the new active bits on the HC908AZ60A:

Bit 3 (AT60A) is new to the HC908AZ60A and is a device indicator read-only bit that identifies the device as new A-suffix silicon. If this bit is a ‘1’ then it is HC908AZ60A silicon.

Bit 7 (EEDIVCLK) is new to the HC908AZ60A and is the EEPROM Timebase Divider Clock Select bit that selects the reference clock source for the EEPROM timebase divider. Selected as a ‘1’ means that the CPU bus clock (possibly the PLL) drives the EEPROM time base divider. A ‘0’ selects CGMXCLK instead.

Illegal Address Reset

An opcode fetch (but **not** a data fetch) from an illegal address on the HC908AZ60A will generate an illegal address reset.

Monitor Mode Entry and COP Disable Voltage

The monitor mode entry and COP disable voltage specifications (V_{HI}) have been increased for the HC908AZ60A. Please consult the Specifications chapter of the latest HC908AZ60A specification for details.

Low Voltage Inhibit (LVI)

The user should be aware that the low voltage inhibit (LVI) specifications for trip and recovery voltage (V_{LVI}) for the HC908AZ60A are different to the HC908AZ60. Please consult the Specifications chapter of the latest HC908AZ60A specification for details.

Differences Guide

The flowcharts shown in figures 1 and 2 illustrate possible methods for determining whether a device is a HC908AZ60A or a HC908AZ60. Figure 3 is a checklist of the main HC908AZ60A differences.

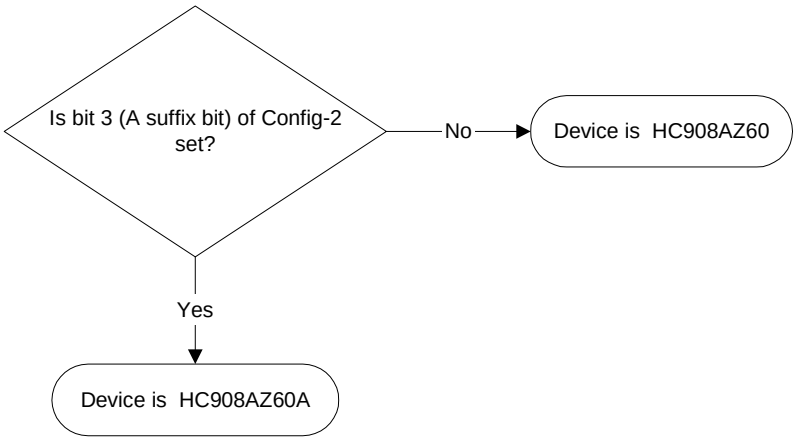

Figure 1. Method to detect a HC908AZ60A

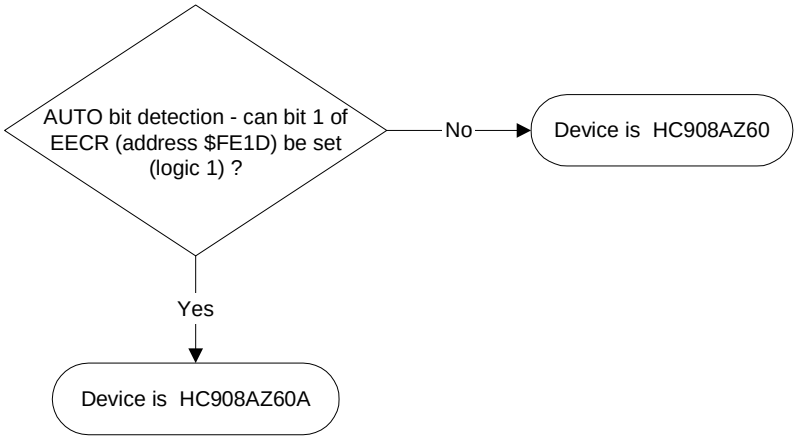

Figure 2. Alternative Method to detect a HC908AZ60A

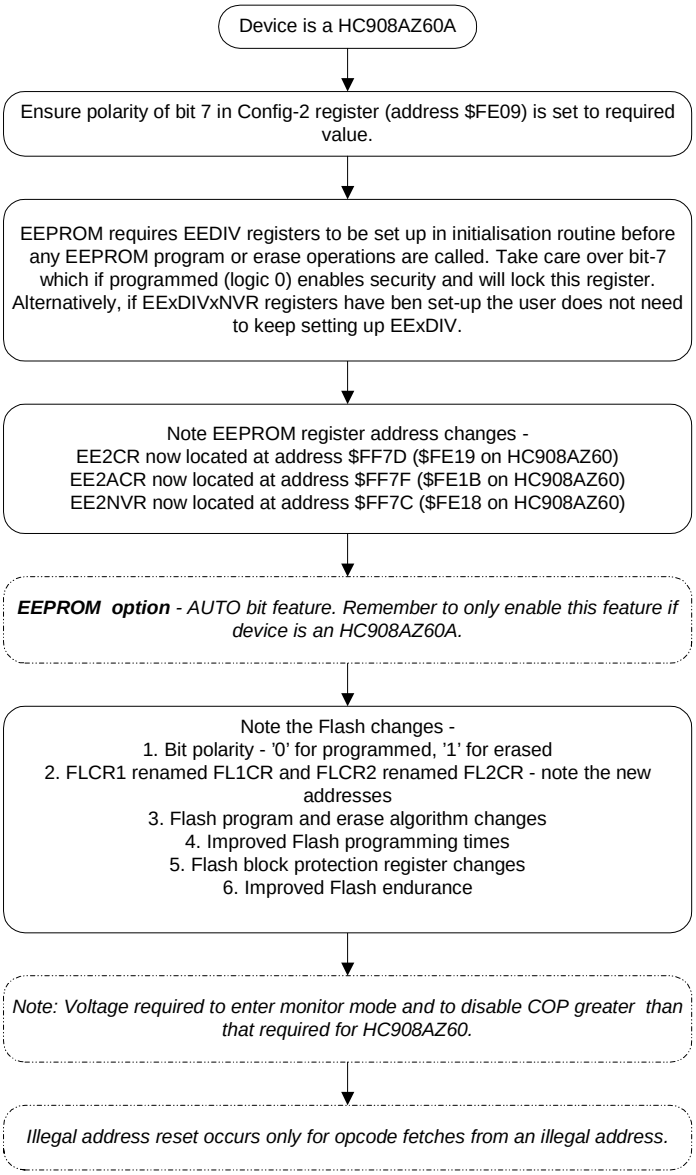

Figure 3. Main differences to consider when designing in the HC908AZ60A

Conclusion

All of the differences discussed above should be taken into account when transferring HC908AZ60 code for the HC908AZ60A. These differences should also be considered if code is being developed for use on both the HC908AZ60A and the HC908AZ60. The methods shown in **Figure 1** and **Figure 2** enable detection of HC908AZ60 versus HC908AZ60A and will prove useful if this is required.

Finally, the user is advised to read the relevant chapters of the latest MC68HC908AZ60 and MC68HC908AZ60A specifications to ensure all differences have been fully captured.

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