Order this document
by AN2158/D

Semiconductor Products Sector
Application Note

AN2158

Designing with the MC68HC908JL/JK Microcontroller Family

By Yan-Tai Ng
Applications Engineering
Microcontroller Division
Hong Kong

This application note describes design techniques for the Motorola MC68HC908JL/JK family of MCU devices, hereafter referred to as the JL/JK family, or JL/JK for a single device.

For full device specifications, please refer to the data sheets, Motorola order numbers: MC68HC908JL3/H and MC68HC08JL3/H.

Introduction

The JL/JK family are popular, low-cost, general purpose MCUs in the Motorola HC08 Family. The JL/JK devices have 4096 or 1536 bytes memory for user code, 128 bytes RAM, crystal or RC oscillator, analog-to-digital converter, 16-bit timer, and is available in various packages. The new generation FLASH memory on the FLASH parts has a program-erase cycle of 10,000 times.

The versatility of the JL/JK makes the device suitable for many applications, and sometimes finding itself in some very noisy environments. These noise and interference problems are made worse by poor circuit design and PCB layout, resulting in intermittent MCU failures and even complete breakdown.

To avoid these undesirable effects, there are some basic techniques that can be applied during circuit design and PCB layout. This application note outlines some recommendations.

The JL/JK family comprises an array of devices with common modules, different size FLASH, ROM, and oscillator options. Table 1 below lists the devices in the JL/JK family:

Table 1. MC68HC908JL/JK Family

Device	FLASH (Bytes)	ROM (Bytes)	Oscillator	Pin Count	Comments
MC68HC908JL3	4096	—	XTAL	28 pins	
MC68HRC908JL3	4096	—	RC	28 pins	
MC68HLC908JL3	4096	—	XTAL	28-pins	Operating voltage: 2V to 2.4V
MC68HC908JK3	4096	—	XTAL	20 pins	
MC68HRC908JK3	4096	—	RC	20 pins	
MC68HLC908JK3	4096	—	XTAL	20 pins	Operating voltage: 2V to 2.4V
MC68HC908JK1	1536	—	XTAL	20 pins	
MC68HRC908JK1	1536	—	RC	20 pins	
MC68HLC908JK1	1536	—	XTAL	20 pins	Operating voltage: 2V to 2.4V
MC68HC08JL3	—	4096	XTAL	28 pins	
MC68HRC08JL3	—	4096	RC	28 pins	
MC68HC08JK3	—	4096	XTAL	20 pins	
MC68HRC08JK3	—	4096	RC	20 pins	
MC68HC08JK1	—	1536	XTAL	20 pins	
MC68HRC08JK1	—	1536	RC	20 pins	

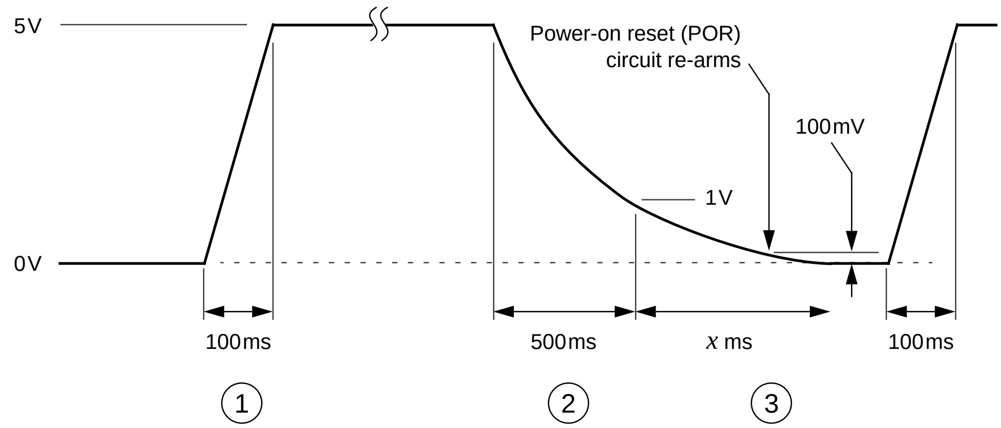
NOTE:
These devices are available in various packages; please refer to the device data sheets for full ordering part numbers.

Power-Up and Power-Down Requirements

The precautions described below must be followed for MCU power-up and power-down, otherwise unpredictable MCU behavior may occur.

Power supply rise-time

Power supply fall-time



Note: Related parameters are specified in the datasheet.

Figure 1. Power Supply Power-Up/Down Requirements

Meeting power-on reset requirements

1. At power-up, supply voltage rise-time should be as short as possible; less than 143ms for 5V operation; best to aim for less than 100ms.
2. At power-down, supply voltage should fall below 1V in less than 500ms.
3. Before power-up again, supply voltage must fall below 100mV for the JL/JK power-on reset circuit to rearm.
4. In addition, keep the external reset pin ($\overline{RST}$) pulled low at least until supply voltage has reached its operating level.

Improper power-up or power-down conditions cause problems for all MCUs, not just the JL/JK. Since the MCU contains a microprocessor and running a program, an improper power-up may cause the MCU to behave erratically and execute runaway codes. In severe cases, devices with electrically erasable memory (e.g. FLASH memory) could experience memory erasure if these power-up and power-down parameters are not taken seriously.

MCU Clock Generation and Distribution

A reliable, stable and clean reference clock input is very important in MCU application designs, since the clock is the heart of the MCU.

Two oscillator options are available for the JL/JK family: crystal oscillator and RC oscillator. The oscillator option is defined by a mask layer in the silicon and is distinguished by the device part numbering. The crystal oscillator option also supports ceramic resonators and direct clock input.

Clock distribution

Figure 2 shows how the reference clock is divided and distributed to the main modules inside the JL/JK.

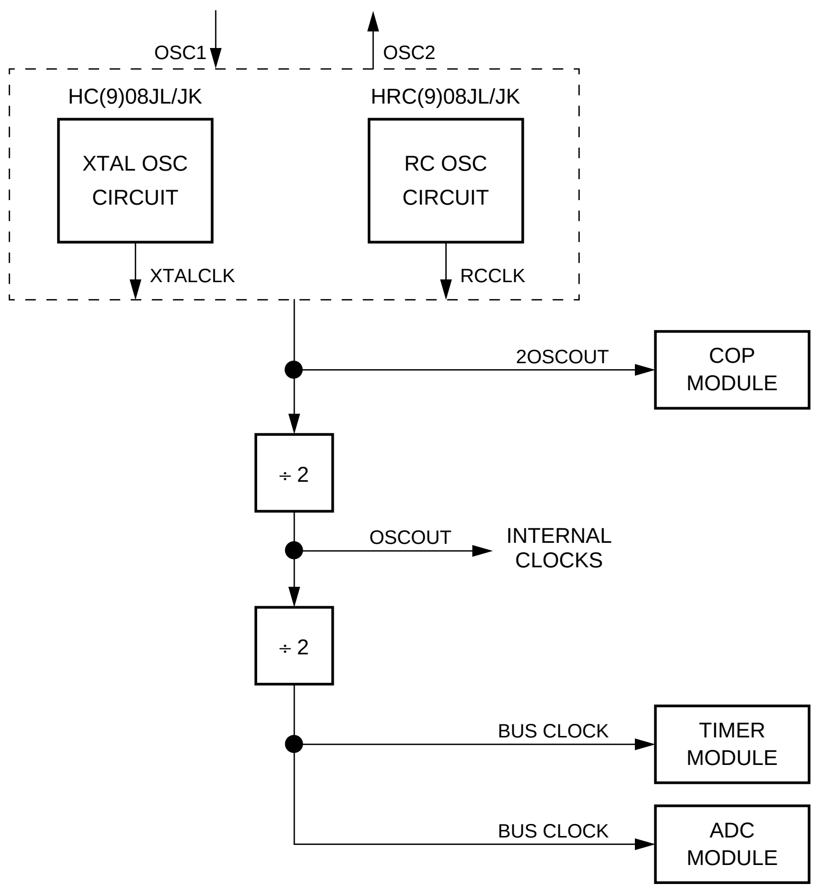


Figure 2. JL/JK Clock Distribution

Crystal connection between OSC1 and OSC2 pins

With the crystal oscillator option, the external component values vary slightly for high frequency and low frequency crystals.

High-frequency crystal

Use the following components when using a high frequency crystal (1 MHz to 24 MHz).

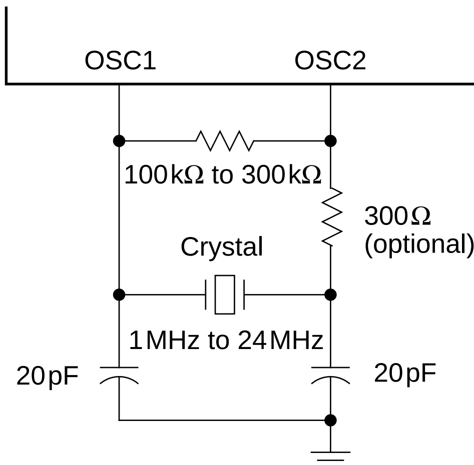


Figure 3. Components for 1 MHz to 24 MHz Crystal Oscillator

Low-frequency crystal

Use the following components when using a 32.768 kHz crystal.

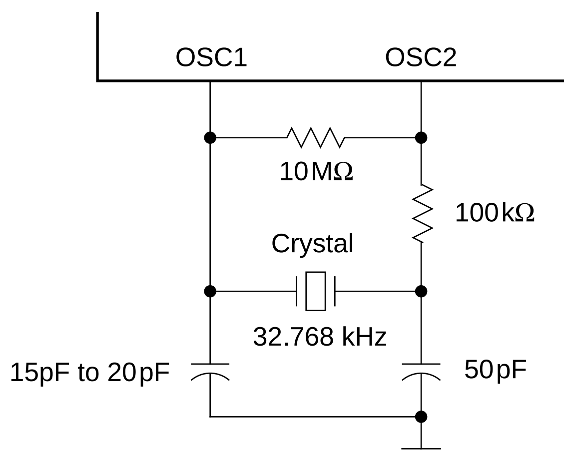


Figure 4. Components for 32 kHz Crystal Oscillator

Crystal oscillator start-up time

Figure 5 shows the typical crystal start-up waveform for the 5V and 3V JL/JK devices. Notice that the crystal oscillation only becomes stable when the supply voltage rises above the LVI circuit trip point.

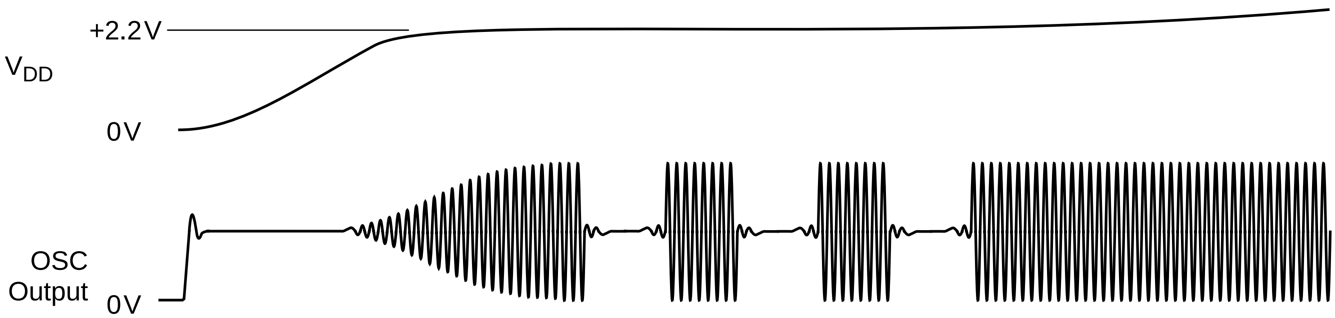


Figure 5. Crystal Oscillator Start-Up

External clock drive into OSC1

The alternative input for the crystal oscillator option is to use a square wave from an external oscillator, driven directly into the OSC1 pin, and leaving OSC2 pin unconnected. The square wave should have a 50% duty cycle. Using this method, the maximum clock input is 32 MHz, providing a bus frequency of 8 MHz. Figure 6 shows the external clock drive.

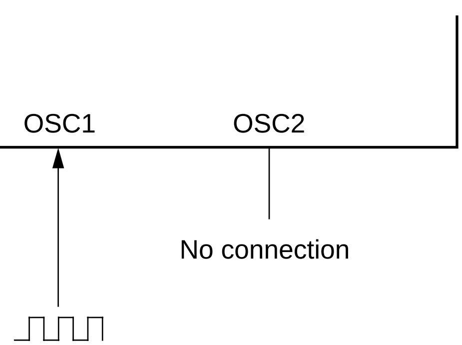


Figure 6. External Oscillator Drive to OSC1

Resistor-Capacitor connection to OSC1

Figure 7 shows the basic connections for the RC option. Refer to the data sheet for values of R and C versus the desired frequency.

Basic RC connection

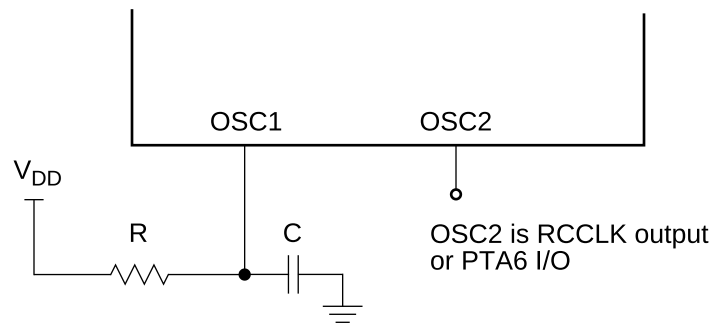


Figure 7. RC Oscillator Connection

To improve noise immunity and reduce switching transients, the component configuration shown in Figure 8 is recommended.

Better RC connection

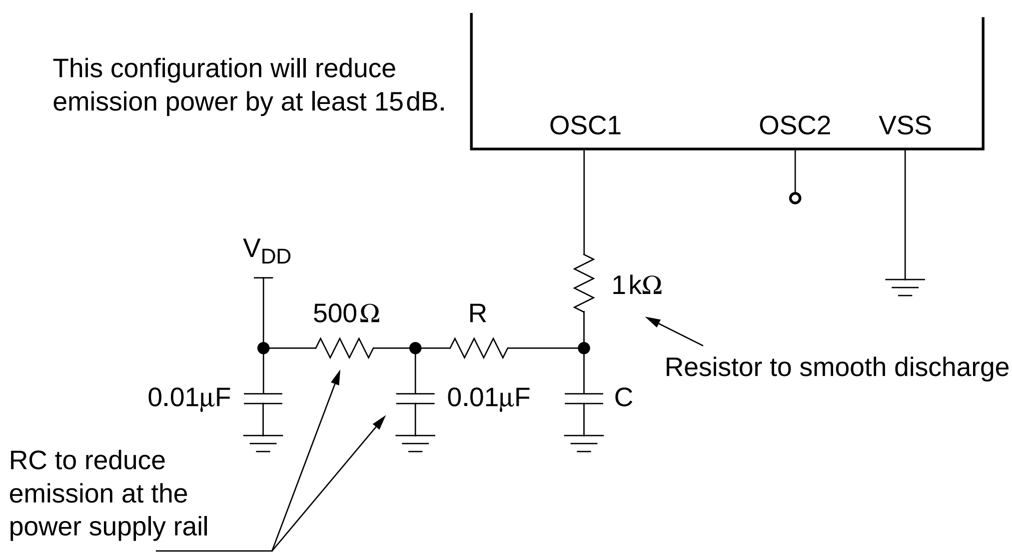
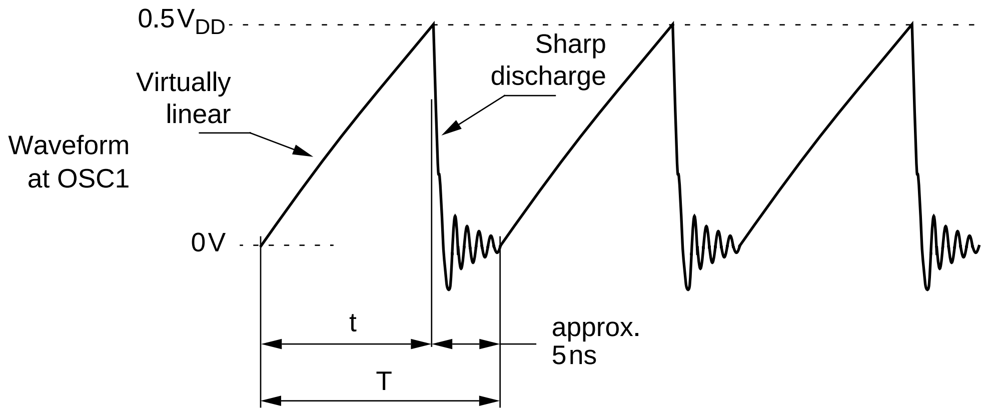


Figure 8. Improved RC Oscillator Connection

Calculating the RC frequency

Although values of the RC frequency can be obtained from the graph in the data sheet, it is possible to calculate this frequency. Figure 9 shows the typical capacitor charge/discharge curve. The calculation includes overshoot time and any parasitic capacitance.



Capacitor charge up time:

$$t = \frac{2}{RC}$$

RC period including overshoots:

$$T = \frac{2}{RC} + 5ns$$

RC frequency:

$$f_{RC} = \frac{1}{\left[\frac{2}{RC} + 5ns\right]}$$

RC frequency, including parasitic capacitance:

$$f_{RC} = \frac{1}{\left[\frac{2}{R(C + C_P)} + 5ns\right]}$$

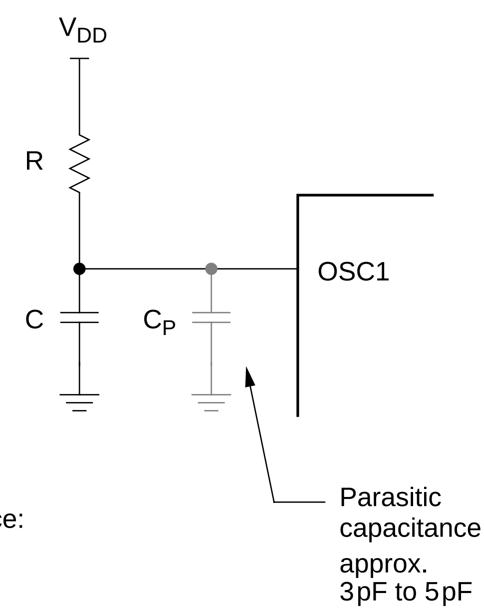


Figure 9. RC Frequency Calculation

FLASH Memory Block Protection

The FLASH block protect register ($FE09)

On the JL/JK FLASH devices, the FLASH memory is block protected after a MCU reset. FLASH program or erase operation is only possible when the FLASH memory is unprotected by writing to the FLASH block protect register at $FE09 (write $FF into $FE09 to unprotect the entire array).

Replacing FLASH devices with ROM devices

The following sub-sections outline the precautions when switching from FLASH with ROM devices.

The USER code

The user code for the FLASH device can be used directly for the ROM device as long as the code does not access any FLASH related registers (i.e. $FE08 and $FE09). These registers are reserved locations on the ROM device.

FLASH related registers

The FLASH related registers ($FE08 and $FE09) are reserved locations on the ROM device.

Monitor ROM

The monitor ROM program on the ROM device is used for MCU testing only. No FLASH programming operations are available.

Using RC clock option

The RC vs. frequency characteristics are not identical for FLASH and ROM devices. Please refer to the respective data sheets for the RC vs. frequency curves.

The Low-Voltage MC68HLC908JL/JK

The JL/JK family includes three low-voltage devices, with an operating voltage of 2V to 2.4V:

- MC68HLC908JL3
- MC68HLC908JK3
- MC68HLC908JK1

The differences to the 5V and 3V devices are:

- FLASH memory can only be read. Program and erase is achieved at an operating voltage of 5V or 3V.

- There is no low-voltage inhibit circuit. Therefore, no low-voltage reset. The associated register bits are reserved bits.
- Only crystal oscillator or direct clock input is supported.

PCB Layout for Critical Signals

PCB layout is often overlooked in a majority of cost-sensitive circuit designs. It is surprising that how a signal is routed can affect the overall performance of the circuit on the PCB. The following sub-sections outline some techniques.

Crystal oscillator connections

Connect these critical components as close as possible to the MCU and with the shortest return path to the MCU ground pin. Each V_{DD} pin should be decoupled to ground with its own capacitor.

Figure 10 shows examples of PCB layout for the crystal oscillator components.

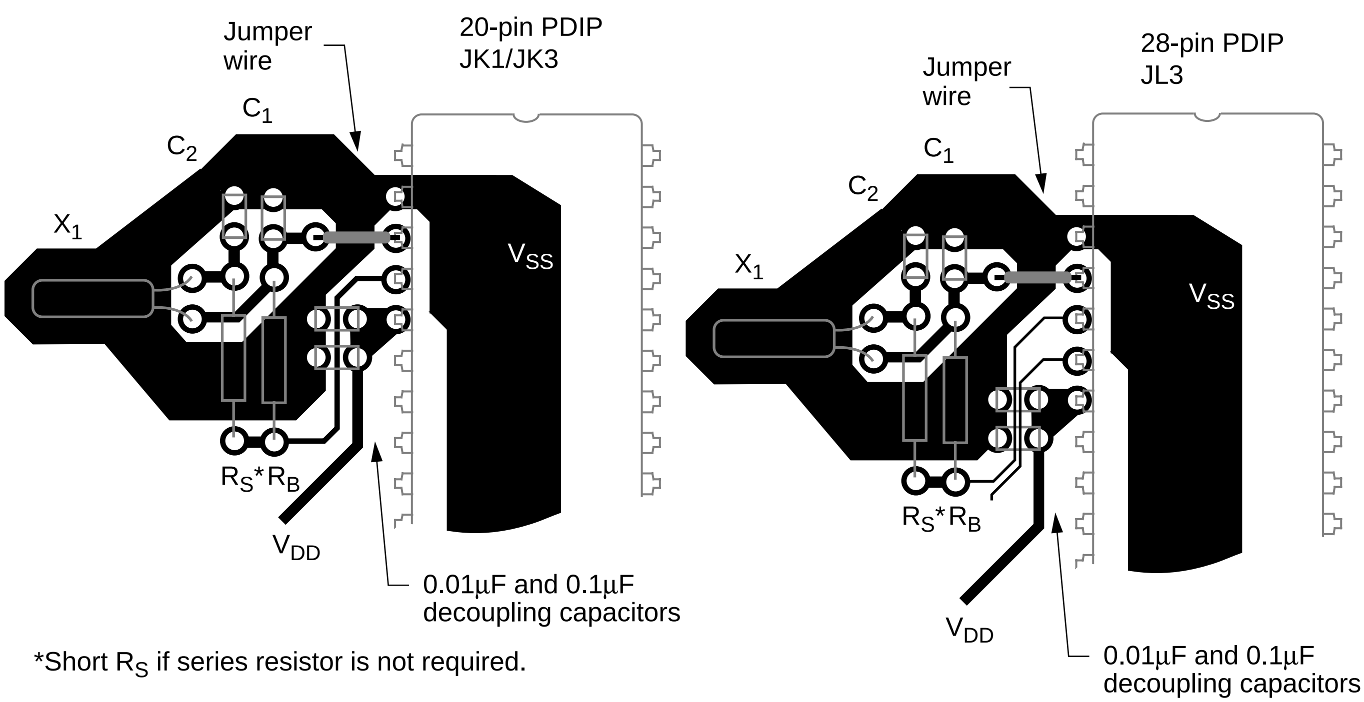


Figure 10. Crystal Oscillator PCB Layout

Ground return for high-current devices

Keep high current return ground paths separate from low current return ground paths, and join them at a single point near the regulator or the power supply input.

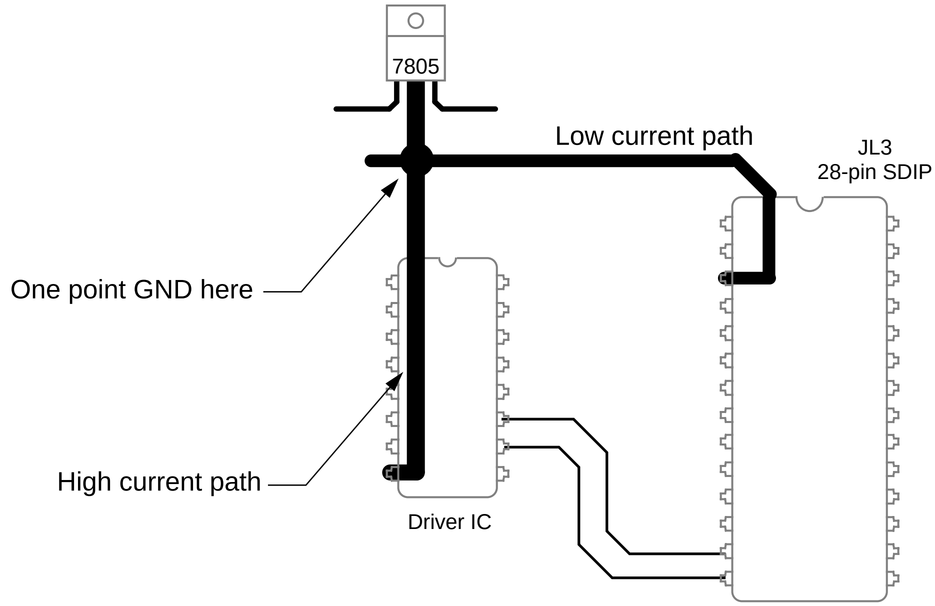


Figure 11. Ground Return for High Current Devices

Long signal paths to ADC pins

Terminate a long PCB trace carrying analog signal with a decoupling capacitor — at the MCU ADC input pin (see Figure 12 and Figure 13).

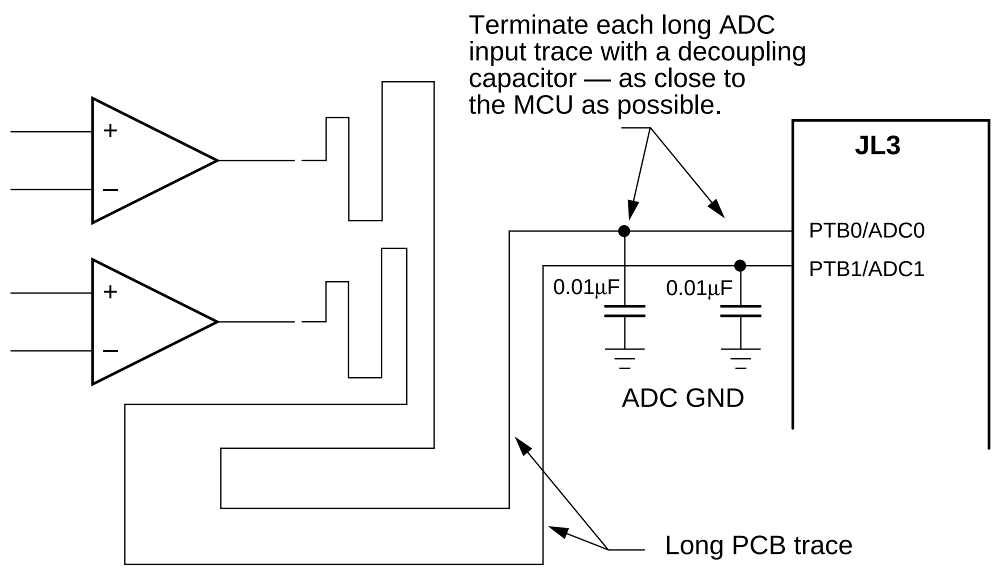


Figure 12. Long Analog Signal Paths

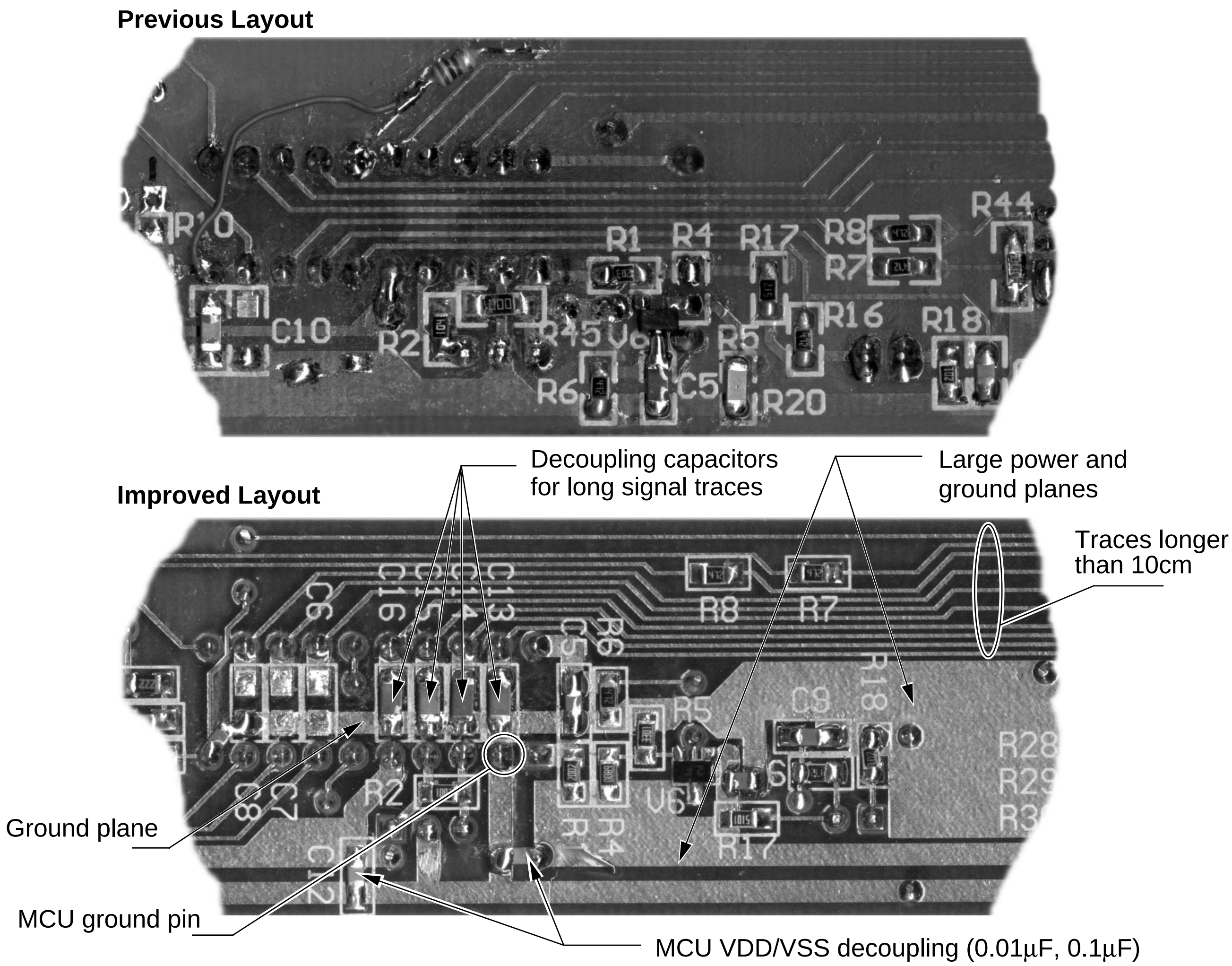


Figure 13. Example PCB Layout