AN12576

MC33771x/MC33772x hot plug performance and prevention measures

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Document information

Information	Content
Keywords	MC33771x, MC33772x, monitoring cell voltage, temperature and current, hot plug, battery management systems
Abstract	AN12576 defines and analyzes hot plug, hot plug risk and ways to mitigate the risk of hot plug, primarily in MC33771x devices.

1 Introduction

MC33771x/MC33772x devices are designed for monitoring cell voltage, temperature, and current in automotive and industrial applications such as BEV, PHEV, ESS, etc. The MC33771x/MC33772x product data sheets provide general peripheral setup and configuration information. Automotive applications may present additional challenges. This application note documents hot plug performance and case by case hot plug prevention measures. The case by case prevention measures can be used in the hardware design phase to mitigate hot plug risks.

MC33771x/MC33772x devices can be used with 14 V, 24 V, 48 V, and HV battery management systems (BMS). The hot plug risk is low when supply voltage is low. MC33772x devices have low hot plug risk. Therefore, the main discussion and analysis in this application note focuses on the MC33771x.

2 What is hot plug?

Hot plug is a common concept in the computer industry. The hot plug concept allows components to be added or replaced without stopping or shutting down the system. Specifically, hot plug describes inserting and/or removing components without interruption to the system. With appropriate software installed on a computer, a user can plug and unplug components without rebooting or shutting down the computer. A well-known example of hot plug functionality is the Universal Serial Bus (USB). USB allows users to add or remove peripheral components such as a mouse, keyboard, printer, or portable hard drive. Depending upon the supplier, such devices are characterized as hot-pluggable.

For battery management systems, MC33771x/MC33772x devices connect directly by sense wire to the battery/cell. The battery/cell is always powered on and has high discharging capability. If discharging current is high enough, internal connection or circuitry cannot tolerate an inrush current surge and the internal block maybe damaged permanently. MC33771x devices require some external components to mitigate hot plug risks. These components can be optimized slightly for different application scenarios.

3 MC33771x cell terminals protection

3.1 Internal ESD structure

MC33771x incorporates various ESD safeguards to ensure robust performance. An equivalent circuit showing the specific protection structures is shown in Figure 1.

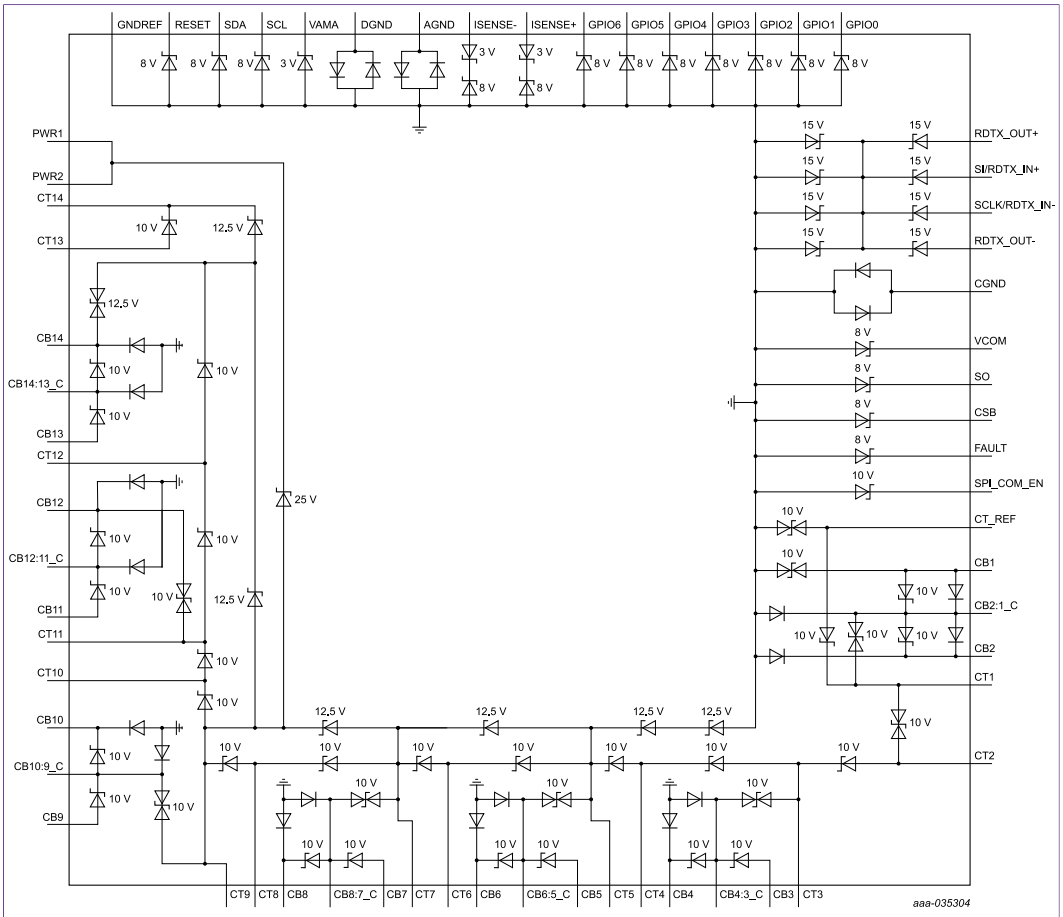

Figure 1. Internal ESD structure

3.2 External components required

Hot plug prevention measures are shown in the MC33771x product data sheets. Refer to the "Hot plug protection" section. See Figure 2.

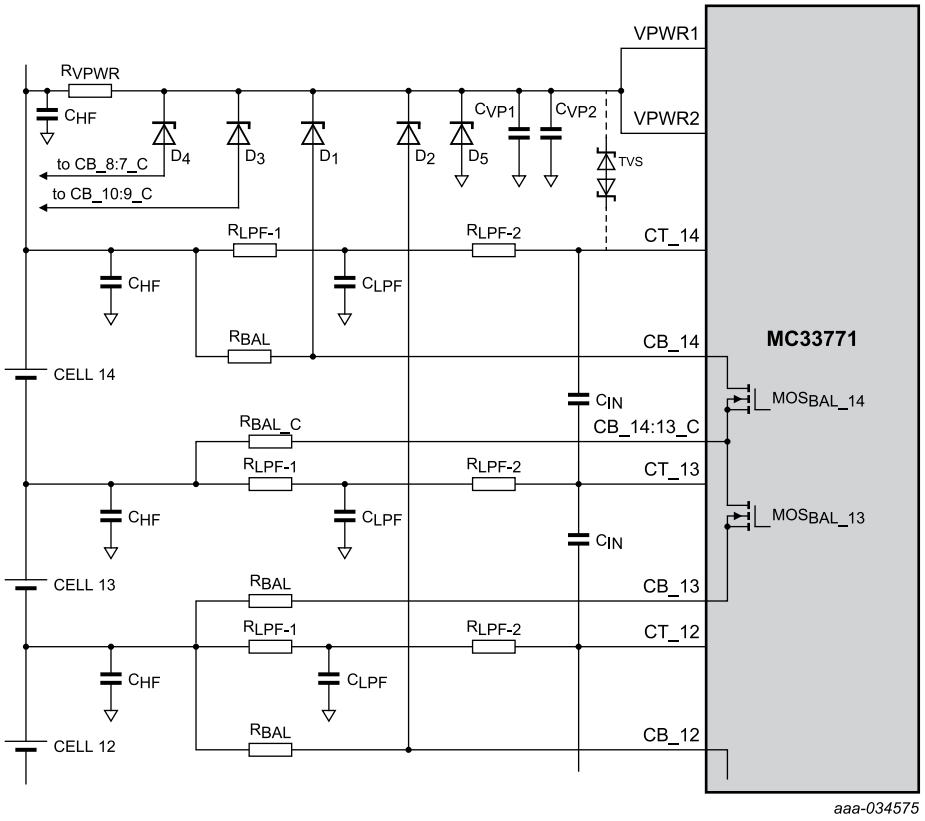

Figure 2. Hot plug protection scheme

Zener diodes D1 to D4 are required to protect internal ESD structures between V_{PWR} and CBx pins. There are two main paths for hot plug risk.

- When V_{PWR} and GND are connected before CTx, charging energy to the CHF via CBx pins exceeds the capability of the internal ESD at max operating voltage
- When CTx and GND are connected before connecting the V_{PWR} pin, charging energy to C_{PWR} exceeds the capability of the internal ESD

Zener diodes D1 to D4 are placed on CB_14, CB_12, CB_10:9_C, and CB_8:7_C pins according to the internal ESD topology. As a result of internal cell balancing transistors, highly robust during hot plug, other CBx pins (i.e., CB_14:13_C, CB_13, CB_12:11_C, CB_11, CB_10, CB_9, CB_8, CB_7) are also protected with these four Zener diodes. All other CBx pins do not need external Zener diodes, since internal ESD clamping voltage is higher than V_{PWR} max operating value. Clamping voltages of Zener diodes D1 to D4 are defined to be higher than the max rating between V_{PWR} and CBx, and lower than the clamping voltage of the internal ESD between these pins.

CBx channels are the main hot plug risk. For CT pins, the risk is lower because the R_{LPF-2} resistor (2 kΩ) reduces the current.

Table 1. Components to avoid hot plug issues

ID	Value	Units	Comments
D_5	75	V	To protect the IC against transient overvoltage, use the specified Zener voltage. For example, use MMSZ5267BT1G (75V) or BZX384-B75
D_4	43	V	D4 is rated 43 V because max operating voltage between VPWR and CB_8:7_C is 35 V and typical internal ESD clamping voltage between VPWR and CB_8:7_C is 60 V. For example, use MMSZ5260BT1G (43v) or BZX384-B43.
D_3	27	V	D3 is rated in the range 26.5 V to 29.5 V, because max operating voltage between VPWR and CB_10:9_C is 25 V and typical internal ESD clamping voltage between VPWR and CB_10:9 is 50 V. The diode voltage rating is limited because the typical internal ESD clamping voltage between VPWR and CT9 is 33v. For example, use MMSZ5255BT1G (28v) or BZX384-B27.
D_2	20	V	D2 is rated 20 V, because max operating voltage between VPWR and CB_12 is 10 V and typical internal ESD clamping voltage between VPWR and CB_12 is 50 V. For example, use MMSZ5250BT1G (20v) or BZX384-B20.
D_1	2 x 8.2	V	D1 is rated 16.4 V, because max operating voltage between VPWR and CB_14 is 10 V and typical internal ESD clamping voltage between VPWR and CB_14 is 50 V. Implementation may be done by using two diodes in series, each of which having half Zener voltage. For example, use two MMSZ5237BT1G (8.2v) or two BZX384-B8V2.
R_{VPWR}	10	Ω	Reducing resistance value may jeopardize hot plug capability. Power rating is 0.1 W.
C_{VP1}	220	nF	To withstand hot plug, this value must not be changed
C_{VP2}	1	nF	Ceramic capacitor
TVS (optional)[1]	8	V	If V_{PWR} > 55 V during hot plug then a TVS (PESD5V0V1BB or equivalent) should be added between CT14 and VPWR. The indicated voltage is the nominal breakdown voltage.

[1] The external components' parameter is based on the datasheet.

3.3 Cell terminal protection during hot plug

3.3.1 Hot plug analysis when V_{PWR} and GND pin are connected

This section presents a situation where V_{PWR} and GND pins are connected *prior* to other pins. The empty capacitors (CHF, CLPF) at entry of CTx and CBx induce the charging path. If V_{PWR} is greater than the trigger point of the internal ESD structure, all generated charging current travels through the internal ESD structure, leading to its failure.

The charging path is different when external Zener diodes are introduced. If V_{PWR} is higher than the breakdown point of Zener, the charging current would go through an external Zener prior to internal ESD. For this reason, an external Zener can mitigate hot plug risk. See Figure 3 and Figure 4

Analysis with/without Zener (D3) when VPWR – GND > 35 V (25 V + 10 V)

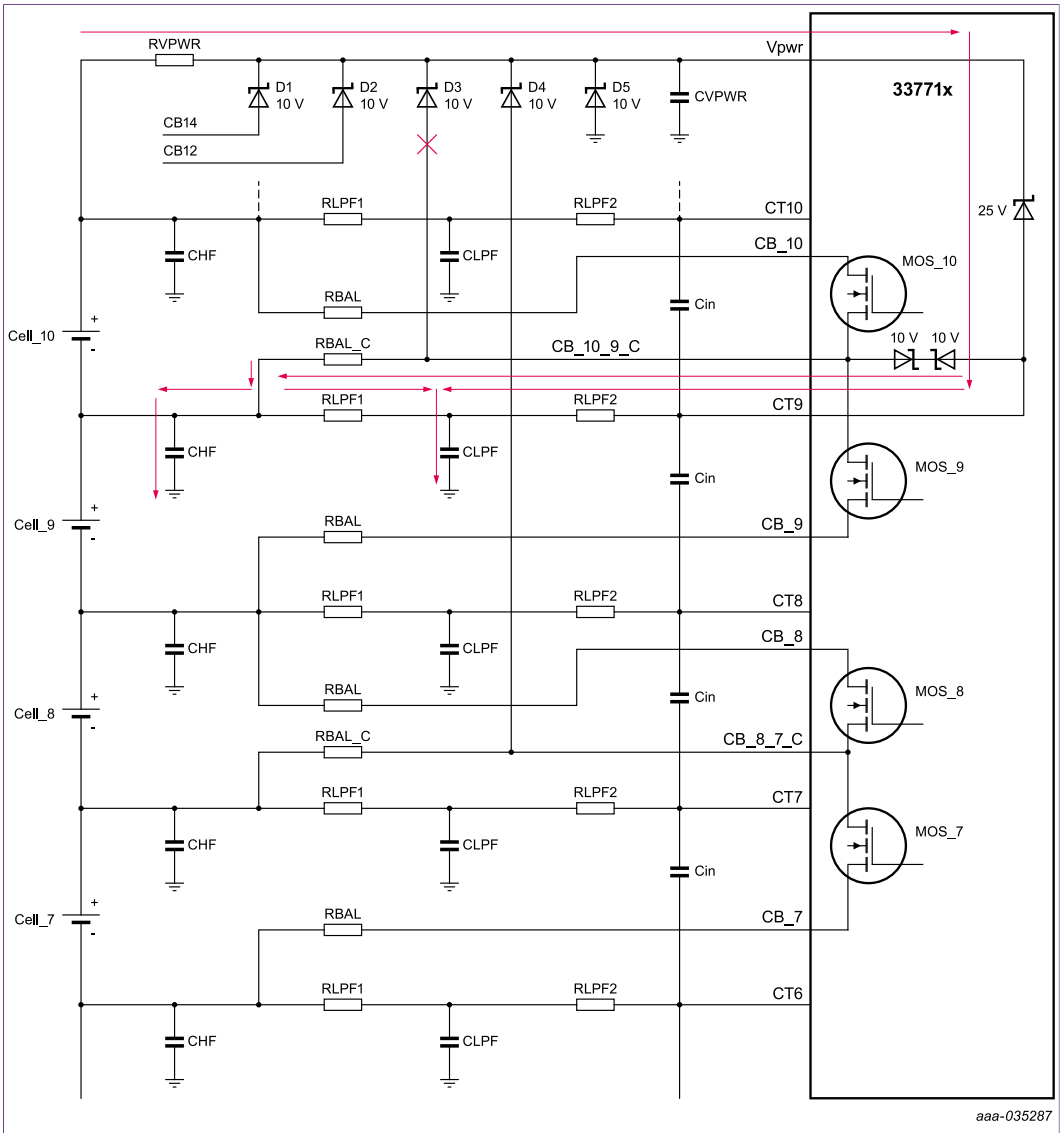

Figure 3. Current path without D3

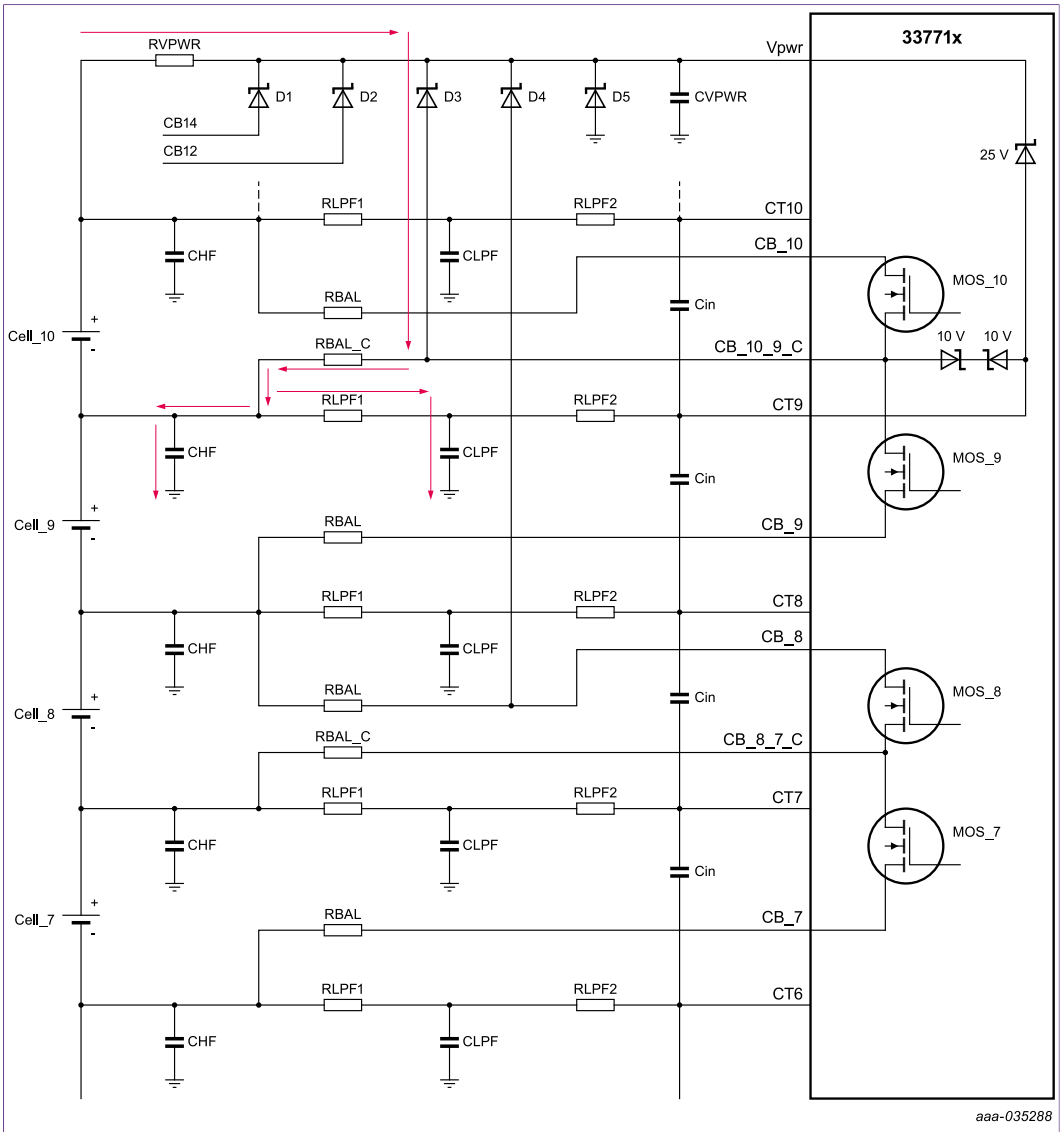

Figure 4. current path with D3

D3 is triggered when VPWR – GND = 27 V, before internal 35 V structures

3.3.2 Hot plug analysis when CELLx and GND pin are connected

The current paths shown in Section 3.3.1 occur when V_{PWR} and GND are connected prior to others. In addition to these paths, there are many other connection combinations during hot plug that include: CELL14 and GND connected first; CELL13 and GND connected first; and so on. In these conditions, the external Zener forwards the bias and the C_{PWR} is charged through the Zener instead of the internal ESD. In this section, hot plug analysis is based on CELL14 and GND connected, and the same analysis can be used for the remaining combinations.

Analysis with/without Zener (D3) when CELL14 – GND > 25 V (12.5 V + 12.5 V)

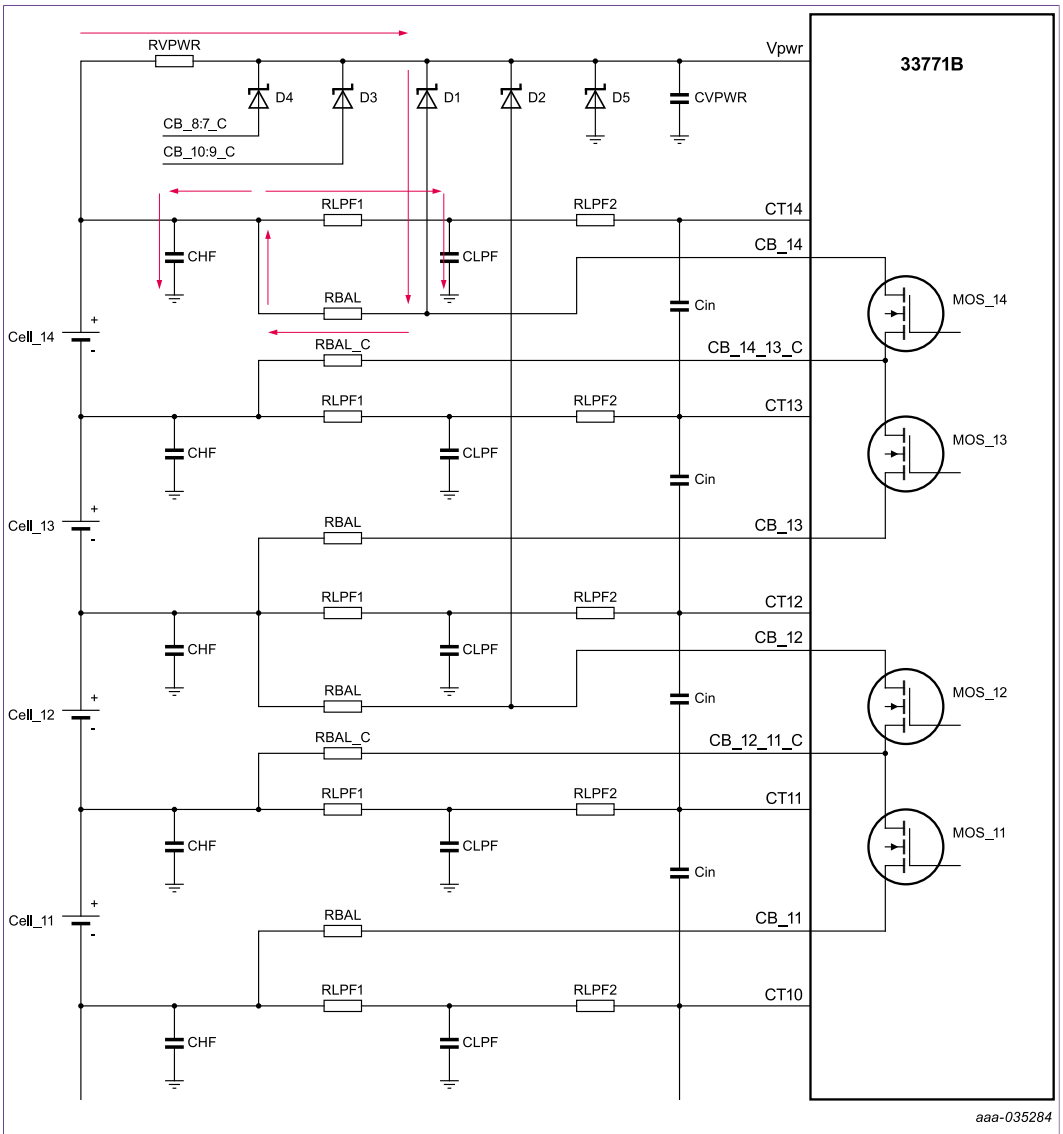

Figure 5. Current path without D1

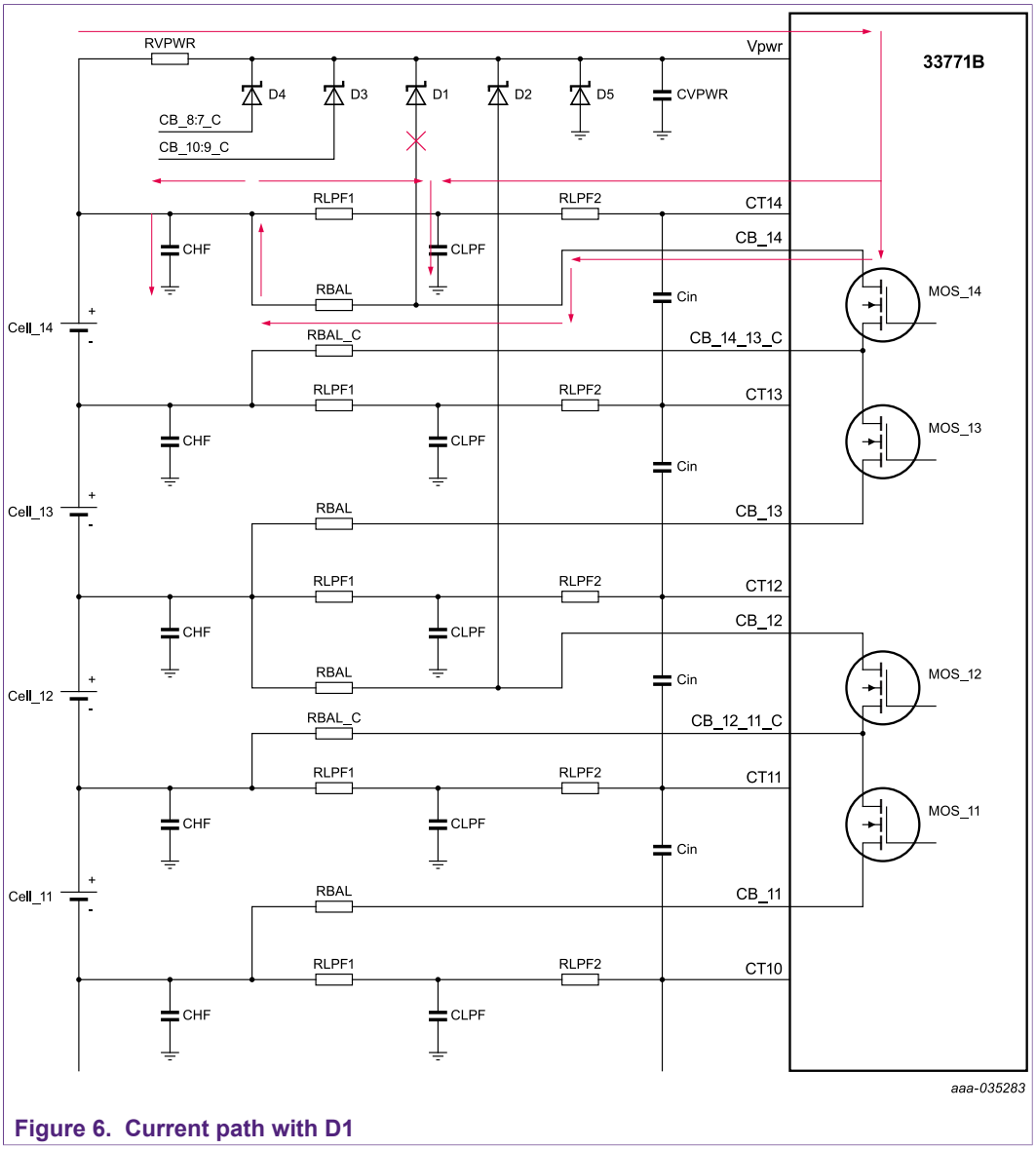

Figure 6. Current path with D1

3.3.3 Hot plug protection when the supply voltage exceeds 55 V

When V_{PWR} of MC33771x exceeds 55 V, a TVS is required between V_{PWR} and CT14 pins as shown in Figure 7. The type is PESD5V0V1BL.

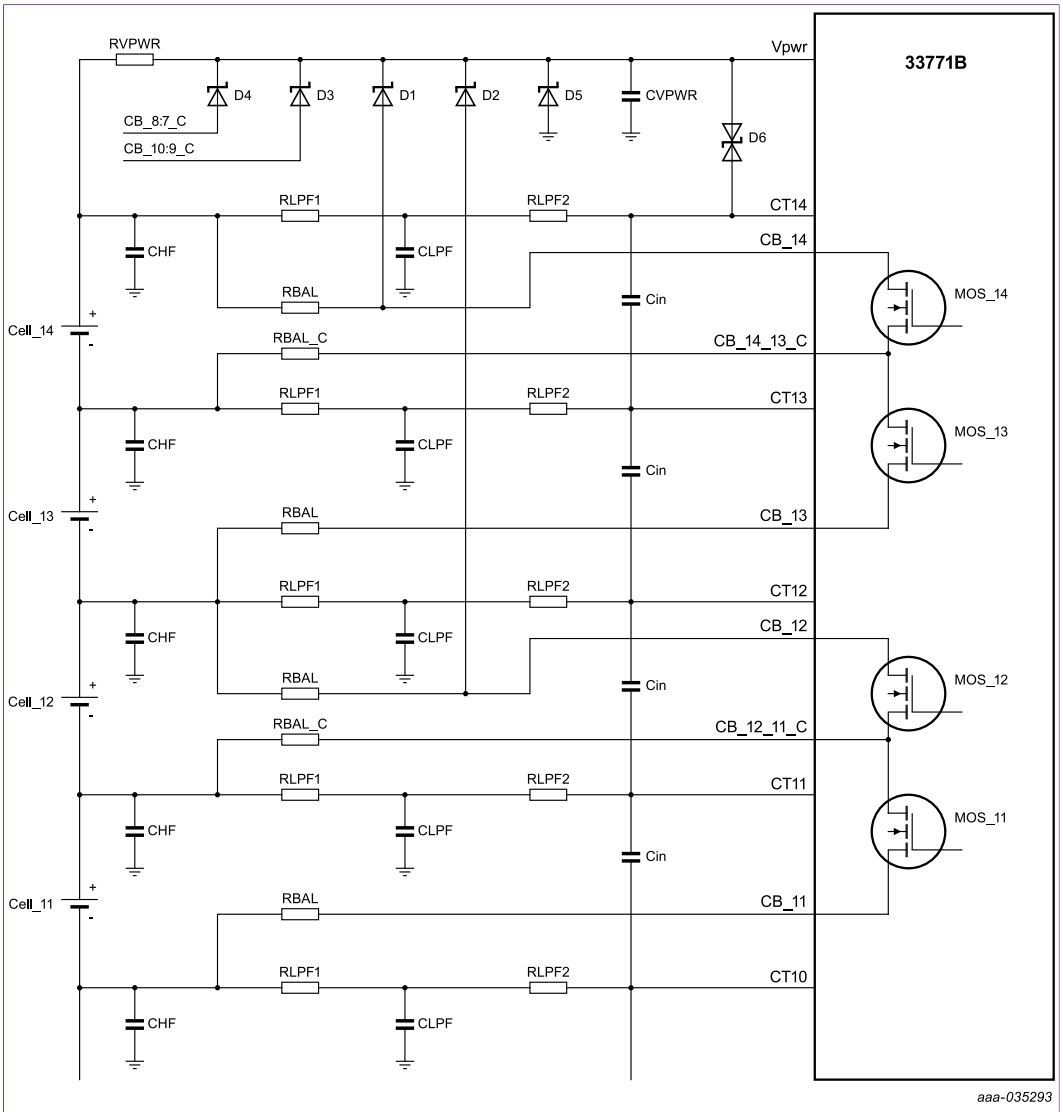

Figure 7. A TVS between VPWR and CT14

Table 2. Hot plug protection parameter above 55 V

ID	Value	Units	Comments
D6	5	V	To protect the IC against transient overvoltage, use the specified TVS operation voltage. For example, use PESD5V0V1BL.

3.3.3.1 TVS selection

As the TVS selection is based on validation, TVS parameters are as follows:

- Breakdown voltage is lower than 8 V
- Diode capacitance is less than 11 pF
- Peak current should be larger than 4.8 A

3.3.3.2 Hot plug analysis at V_{PWR} exceeds 55 V

An internal 25 V clamp structure diode is located between VPWR and CT9. Normally, the hot plug risk on CT pins is not considered because the presence of a 2 kΩ resistor mitigates the charging current of the CLPF capacitor.

However, internal ESD between V_{PWR} and CT9 has a chance to cause damage by charging current for CLPF when V_{PWR} is over 55 V. The charging current may exceed the capability of ESD between VPWR and CT9. Therefore, the external TVS (D6) can mitigate a current surge to internal ESD. See Figure 8 and Figure 9.

Charging current path without TVS at V_{PWR} exceeds 55 V

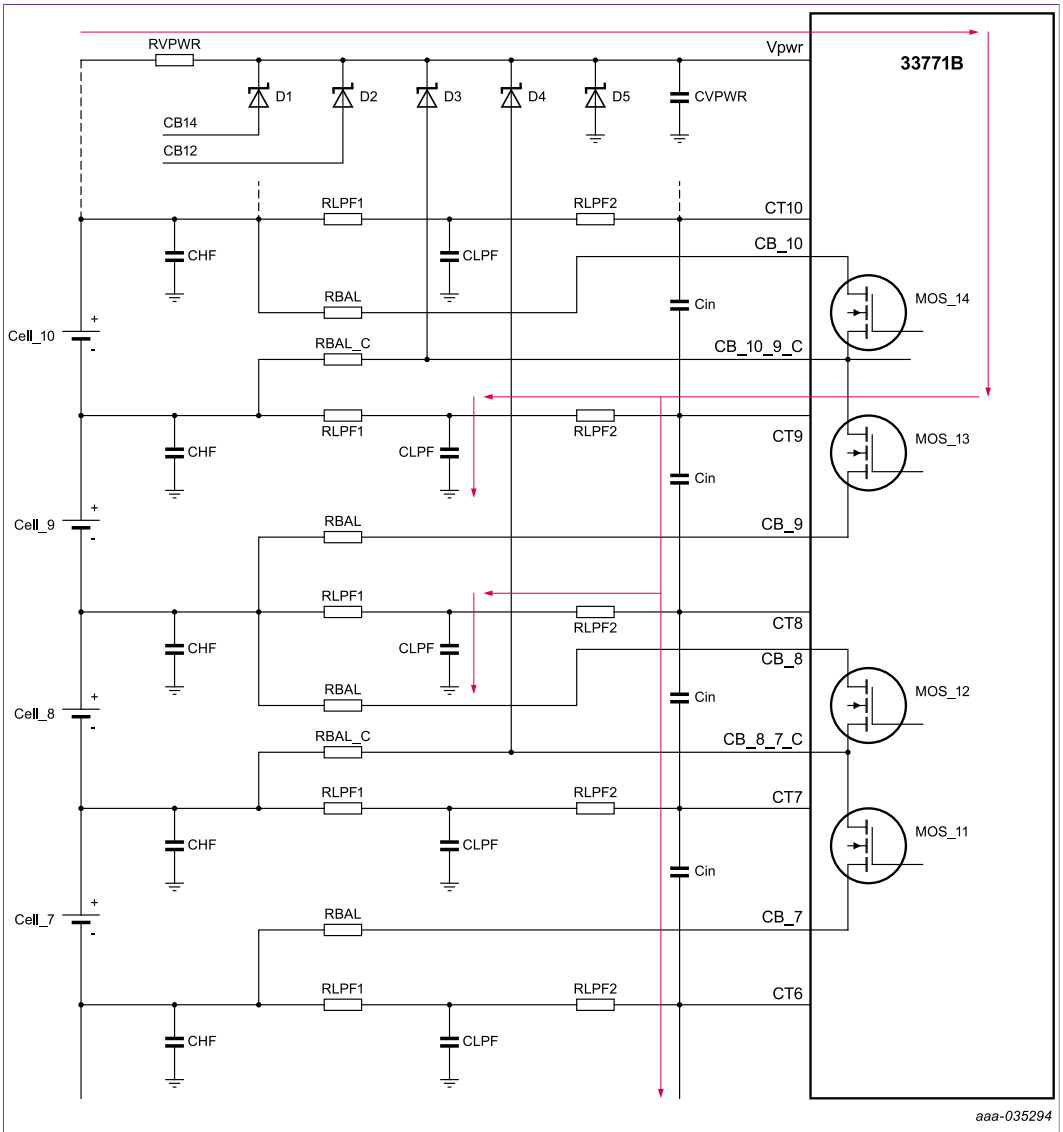

Figure 8. Charging current path without TVS when VPWR exceeds 55 V

Charging current path with TVS when V_{PWR} exceeds 55 V

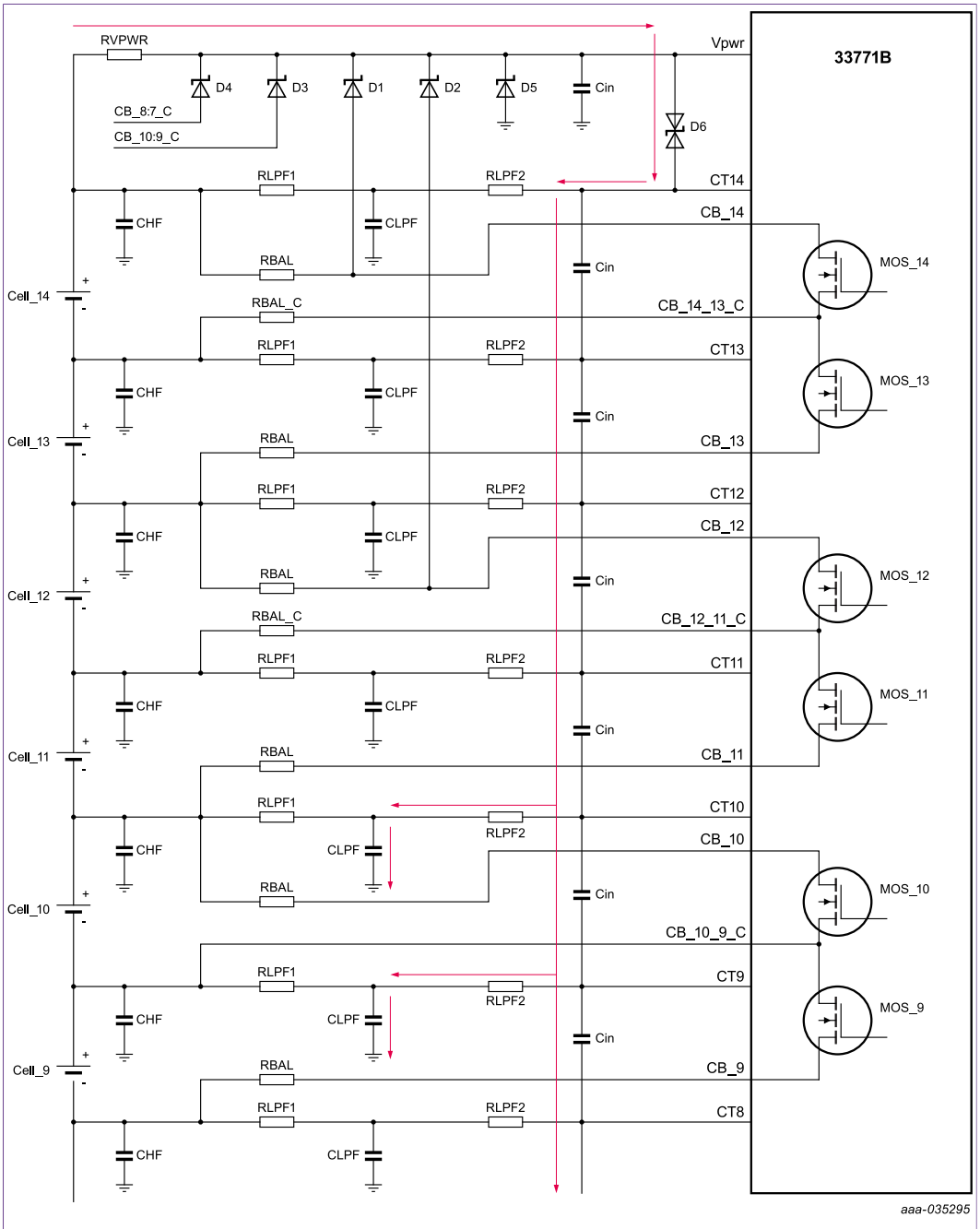

Figure 9. Charging current path with TVS when VPWR exceeds 55 V

3.4 R_{VPWR} functional description

R_{VPWR}, with a recommended value of 10 Ω, can reduce the peak charging current to hot plug. The higher R_{VPWR} is, the better for hot plug. However, the drawback of higher R_{VPWR} is a higher voltage drop between V_{PWR} and CT14 due to the IC current consumption. As the stack voltage is measured across $V_{PWR1, 2}$ pins and ground, the voltage drop affects the stack measurement. Furthermore, accuracy degrades when the

voltage drops between V_{PWR} and CT14, higher than the V_{PWR_CT}. Refer to the V_{PWR_CT} requirement in MC33771x product data sheets.

3.5 D1 functional description

In an actual application, using two diodes in series instead of one diode on D1 is recommended. Transient current can reach approximately 50 mA to 60 mA when the MC33771x is in normal mode and starting communication in the Transformer Physical Layer (TPL) mode. If R_{PWR} is 10 Ω, the voltage drop on R_{PWR} may be approximately 0.5 V to 0.6 V. This means the voltage of CELL14 may be higher than V_{PWR} by approximately 0.5 V to 0.6 V, resulting in a D1 forward bias with the possibility of current going through it. See Figure 10. If this occurs, SM04 may fail when SM04 is running. Refer to the SM04 description in the MC33771x safety manuals.

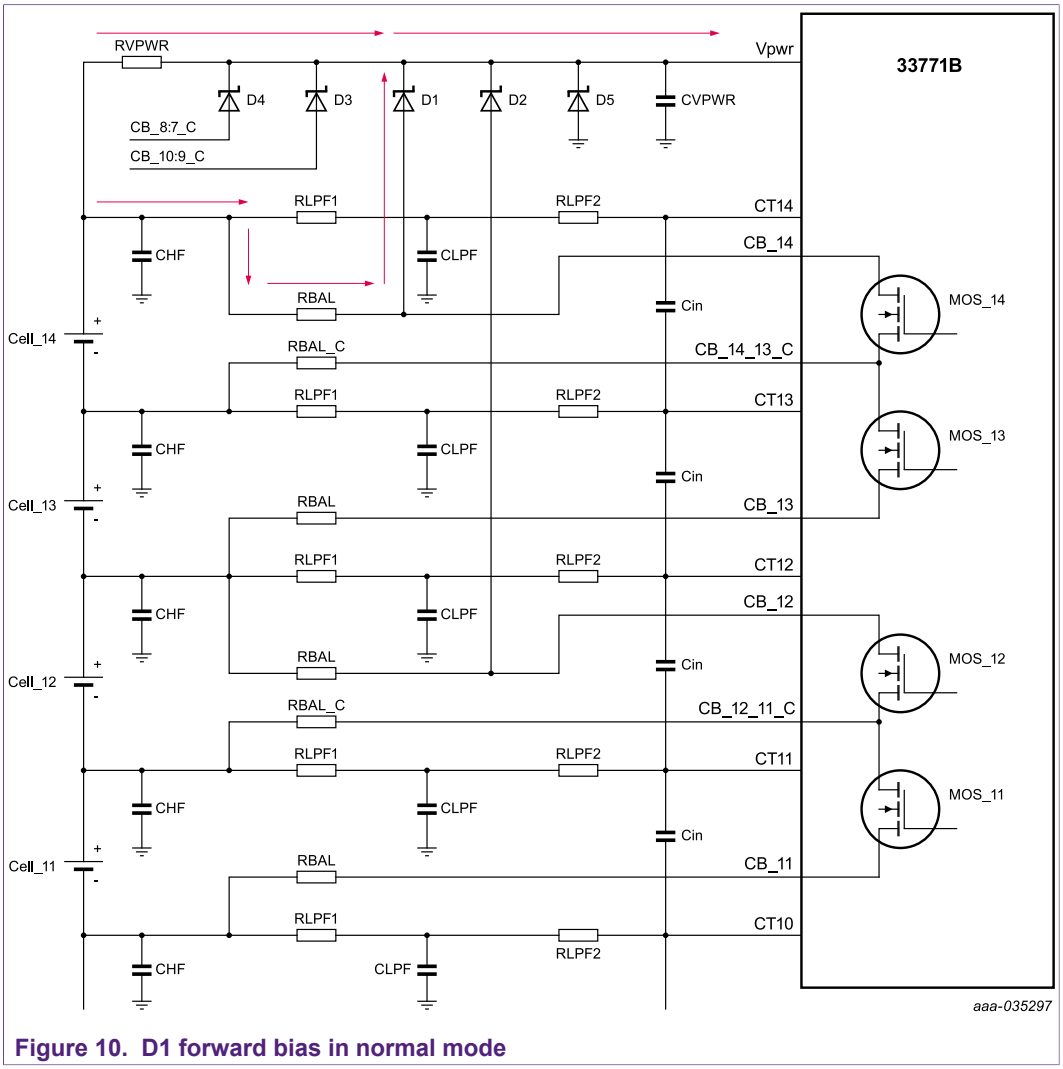

Figure 10. D1 forward bias in normal mode

3.6 The Choice of D5

The Zener diode D5 is not intended for hot plug use. The D5 diode is used to prevent the voltage of V_{PWR} from exceeding the maximum rating of the chip (75 V). In an actual application, the work voltage may be much less than 75 V (for example, using just 12

cells, or using a lithium iron phosphate battery). Under these conditions, reduce the value of the Zener diode D5 or use a TVS instead of the Zener diode. The choice depends on the customer's application. Its position should be at the input of the channel. Namely, it should be between the R_{VPWR} and the connector.

3.6.1 D5 (TVS) selection

- Trigger point (depends on application)
  1. 58 V
  2. 60 V
- Power dissipation (depends on application)
  1. 400 W
  2. 600 W
- Response time
  1. ≤ 1 ns
- Recommended part number
  1. SMBJ60A-HR2
  2. SMBJ58A-HR3
  3. SMBJ64A-HR

Where shall TVS be placed?

- Nearby connector before R_{PWR} (10 Ω) and low impedance to GND.

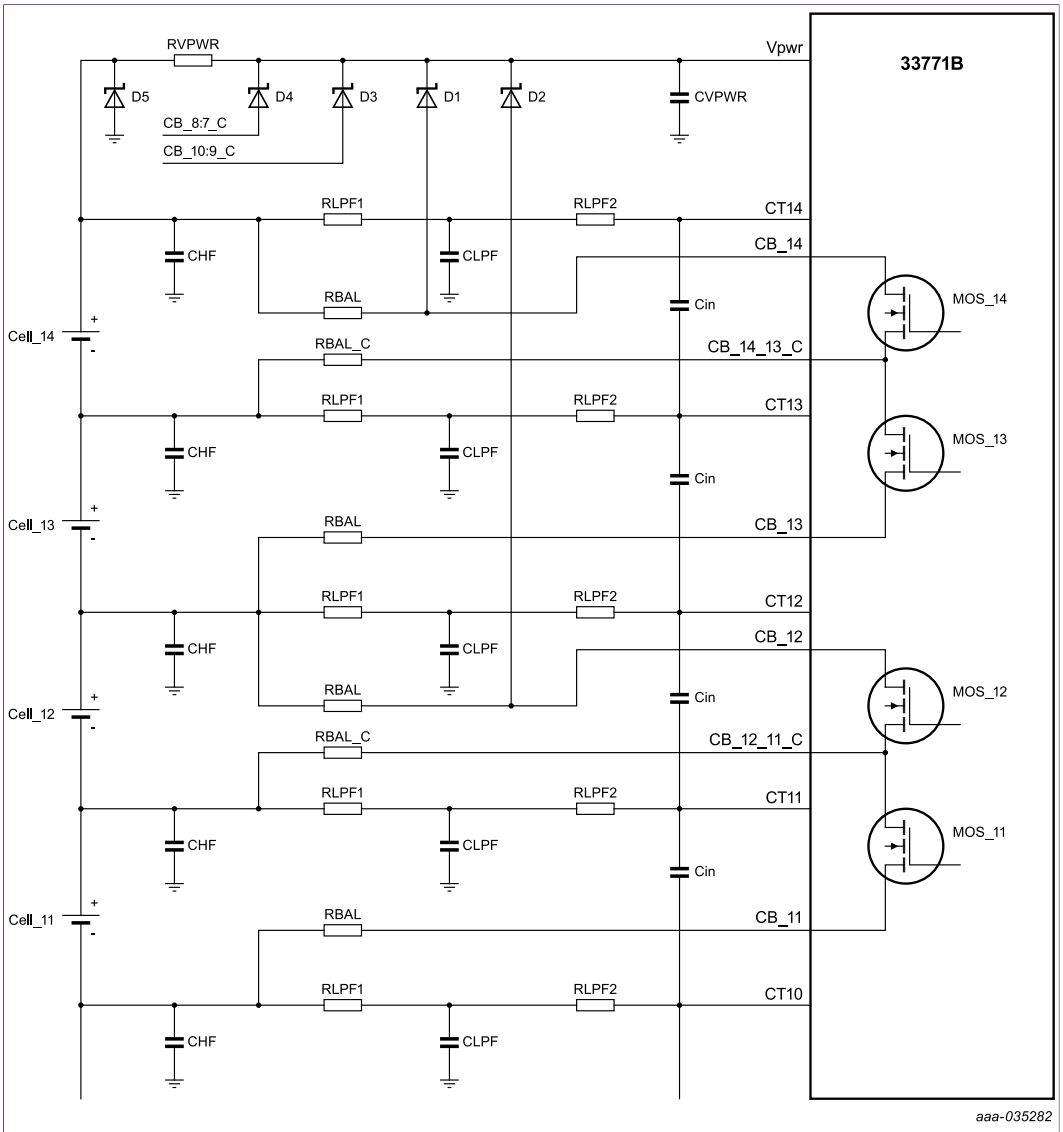

Figure 11. Add TVS at the input of VPWR

3.7 Hot plug on MC33772x

The VPWR line, shown in Figure 12, must be protected by a serial resistor in order to limit the inrush current and a parallel capacitor to filter fast voltage variation. Higher value of R_{VPWR} provides better protection. The drawback of higher R_{VPWR} is higher voltage drop. As the stack voltage is measured across $V_{PWR1, 2}$ pins and ground, stack measurement is affected by such voltage drop. Furthermore, voltage drops higher than V_{VPWR_CT} have a negative impact on cell measurement accuracy.

In order to withstand hot plug, it is mandatory to use components to protect the V_{PWR} line as shown in Figure 12. The maximum voltage of V_{PWR} to sustain hot plug conditions is 24 V (equivalent to 6 cells of 4.0 V).

In general, all components, whose values are given in Table 3, are mandatory to protect the IC when connection is made to the battery pack. Changing the value of any external components listed in Table 3 may result in serious IC damage during the connection to

the battery pack. Capability of the device to sustain random connection to live voltage for pins V_{PWRx}, CT_x, CB_x, CTREF, GND, ISENSE+ and ISENSE− has been extensively evaluated. Nevertheless, the total number of random combinations related to those pins cannot be entirely tested. Therefore, despite all engineering efforts performed by NXP, it is the responsibility of the system provider to ensure safe connection to the battery pack.

It is the responsibility of the system provider to manage the risk of short circuits on any external components connected to the IC, including external low-pass filters. Indeed, a short circuit on the pins connected to the battery can lead to high current flowing through the IC, causing a thermal event on the PCB. The system provider shall employ common practices, such as fuse protection on the V_{PWR} line, series of capacitors on the CT pins, appropriate power rating for external resistors, or any other appropriate measure capable to mitigate hazards.

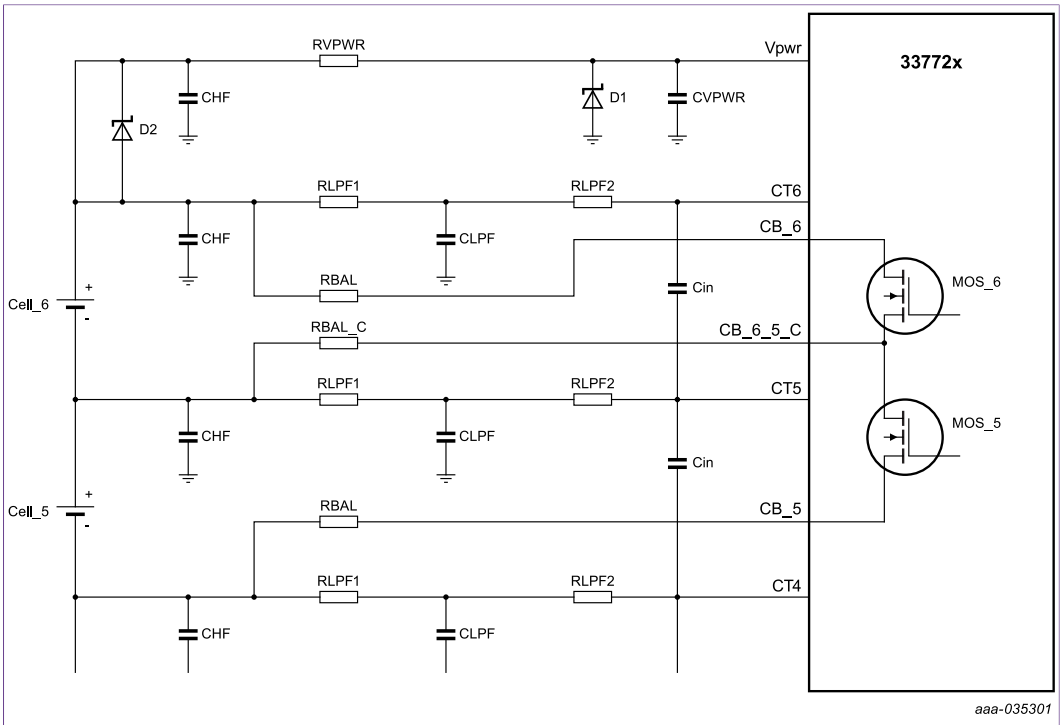

Figure 12. Hot Plug protection for MC33772x

Table 3. Hot plug parameter for MC33772x

ID	Value	Units	Comments
CHF	0.047	µF	To withstand hot plug, use the suggested value
C_{VP1}, C_{VP2}	0.20	µF	To withstand hot plug, this value must not be changed
D1	39	V	To protect the IC against transient overvoltage, use the specified Zener voltage (use BZT52H-B39).
D2	1	A	To withstand hot plug when $V_{PWR1/2}$ and CT_6 are set on different connector lines to connect to the upper cell of the monitored cell stack, use the specified forward current (use PMEG10010ELR) .
RVPWR	6.8	Ω	Reducing the resistance value may jeopardize the hot plug capability. Power rating is 0.1 W

4 Isense protection (MC33771x and MC33772x)

The MC33771x current sense channels (I_{SENSE+} and I_{SENSE-}) can be damaged during the hot plug operation when one of the I_{SENSE+} or I_{SENSE-} pins is connected to shunt and negative battery before MC33771x ground (CGND, AGND, DGND, GNDFLAG, and GNDREF).

To protect the $I_{SENSE+/-}$ pins against hot plugging, one of the following is recommended:

- Ensure the MC33771x ground (CGND, AGND, DGND, GNDFLAG, and GNDREF) is connected to the negative of battery before any $I_{SENSE+/-}$ pins.
- Add a back to back protection Zener diode on I_{SENSE+} and I_{SENSE-} pins, shown in Figure 13.

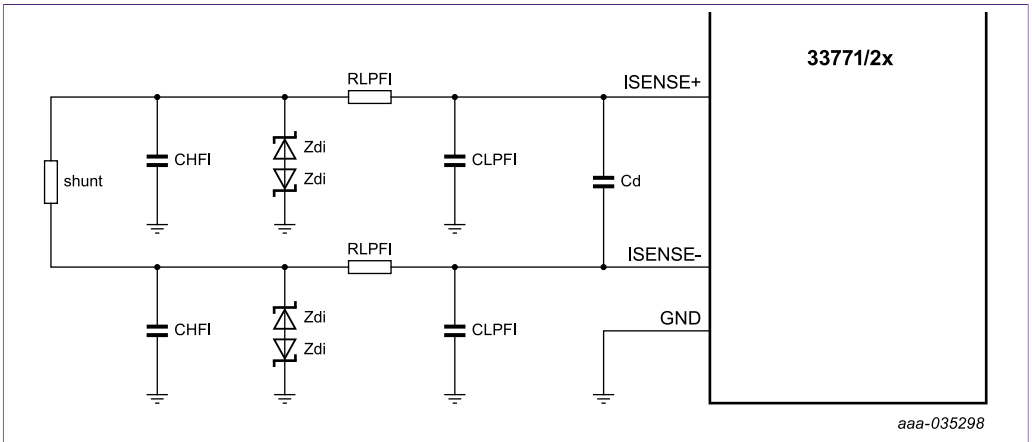

Figure 13. Current sense channel circuitry

Table 4. Current sense channel circuitry parameter

ID	Value	Units	Comments
Cd	6.8	µF	This example value has been chosen to get fCUTI = 91.8 Hz and tDIAG ≤ 31.7 ms. Use 5 % tolerance.
CHFI	47	nF	This component serves to withstand ESD gun and its value must not be changed
CLPFI	47	nF	Value is chosen in order to get: 91.8 Hz, tDIAG ≤ 31.7 ms and fICM = 26.67 kHz. Use 5 % tolerance.
RLPFI	127	Ω	***Caution:*** *Do not exceed 200 Ω. Use 5 % tolerance resistors.* Used value is to get both fCUTI = 91.8 Hz and fICM = 26.67 kHz.
Zdi	2.0	V	To protect during hot plug, in case one of the $I_{SENSE+/-}$ pins is connected before GND of the device. Recommended MMSZ4679T1G.

Note: *If Isense function is not used, $I_{sense+/-}$ should be connected to GND.*

4.1 Current sense protection mechanism

The worst hot plug sequence is:

1. V_{PWR} connected

2. Isense pins connected

When the voltage between GND and I_{SENSE} exceeds 3 V, the charging current will be amplified and latch up may occur. The I_{SENSE} channel may be damaged by the charging current. Therefore, the voltage between GND and I_{SENSE} should be managed so that GND – I_{SENSE} is less than 3 V, a lower risk.

4.1.1 Scenario 1: Zener is not applied

When the Zener diode is not applied, voltage between GND and I_{SENSE} is not limited. The rush current may cause EOS damage to the I_{SENSE} channel. See Figure 14.

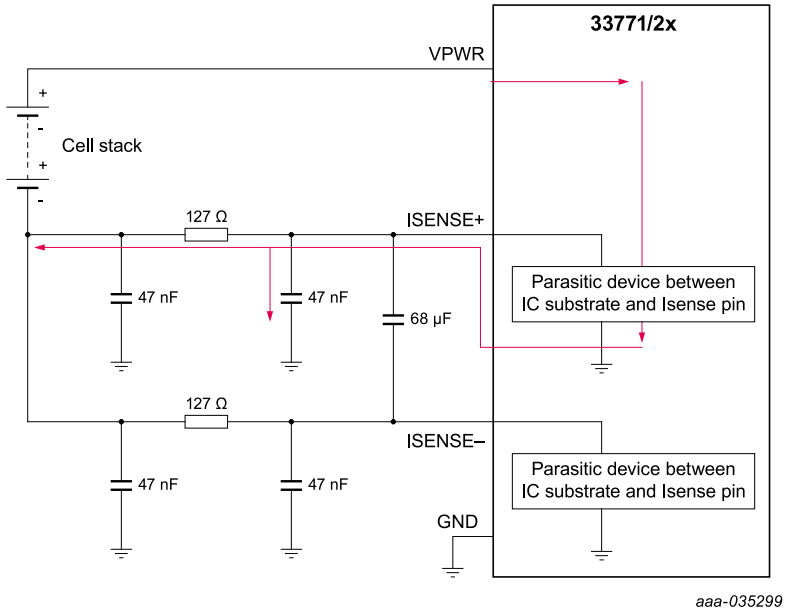

Figure 14. Current path without Zener between I_{SENSE} and GND

4.1.2 Scenario 2: Zener is applied

When the Zener (Zdi) is applied, the voltage between GND and I_{SENSE} is clamped. The supply current travels into the internal structure and out from the GND of the IC. The current returns back to battery from the external Zener and does not go through the I_{SENSE} channel, protecting the I_{SENSE} channel.

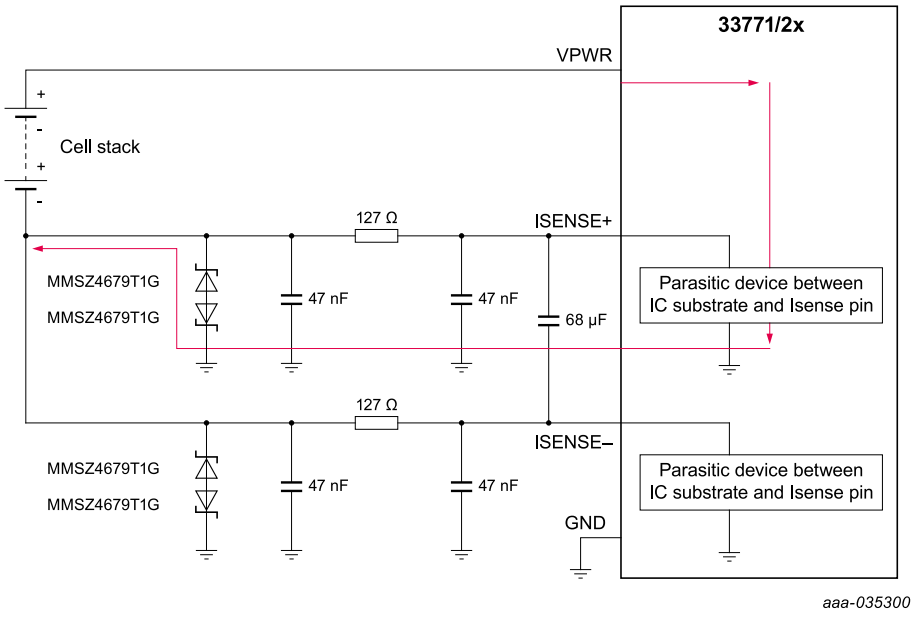

Figure 15. Current path with Zener between I_{SENSE} and GND

5 TPL line protection when capacitive coupling used

5.1 Capacitive coupling for HV system (33771C only)

For capacitive isolation in a centralized system, the schematic is split into two segments. In high-voltage system applications, a high voltage isolation transformer is recommended between the master node and first slave node. Capacitive isolation can be used between slave nodes.

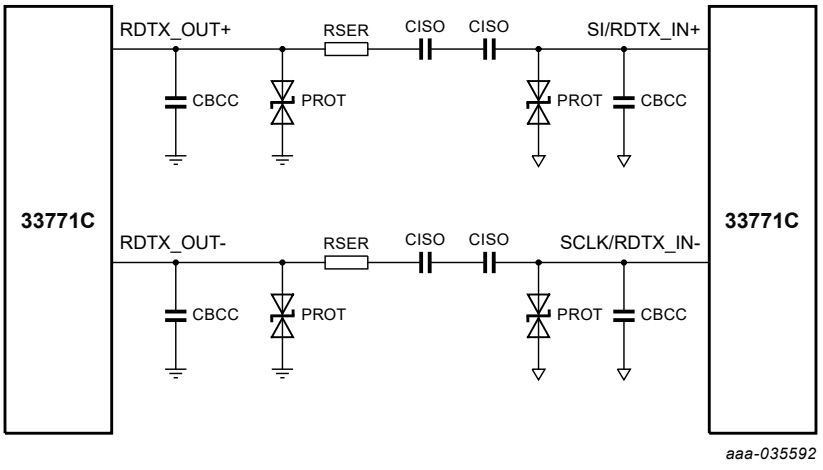

Figure 16. Capacitive isolation circuit

Table 5. Daisy chain capacitive isolation circuit parameter

ID	Value	Units	Comments
CBCC	22	pF	Ceramic capacitor
RSER	62	Ω	Series resistance

ID	Value	Units	Comments
CISO	10	nF	Isolation capacitor
PROT	8	V	ESD protection. Use PESD5V0F1BB or equivalent. The indicated voltage is the nominal breakdown voltage.

5.2 Capacitive isolation hot plug protection mechanism

The potential between two nodes usually could achieve tens of volts, therefore, the hot plug current path is different between transformer isolation and capacitive isolation:

- **Transformer isolation:** Consider the hot plug current path for one node, according to Voltage sense circuitry and Current sense circuitry. There are no current paths between two nodes.
- **Capacitive isolation:** The current path of daisy chain should be considered because of the charging current for the isolation capacitor.

One node connected, the hot plug current will go into the TPL pin of the IC through the TPL line when the next node is connecting.

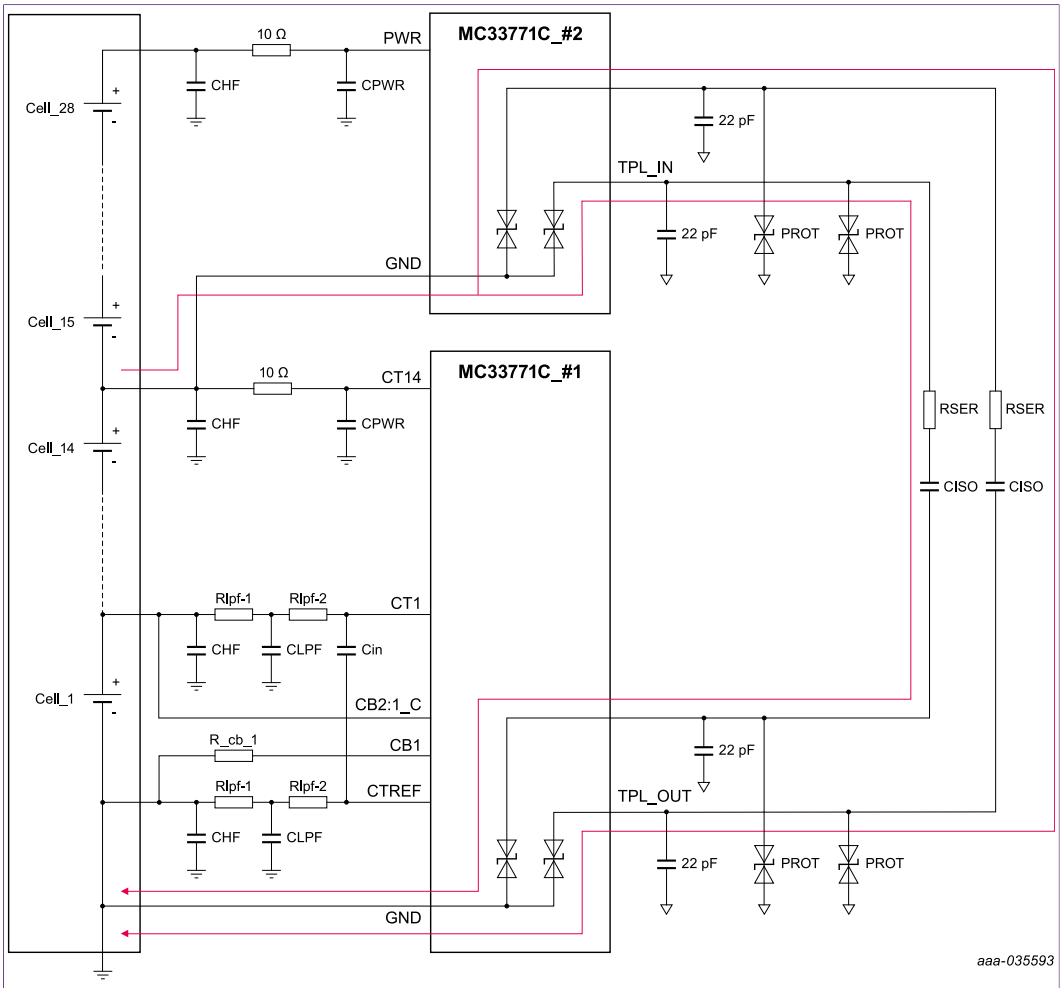

Figure 17. Capacitive isolation hot plug current path

According to Figure 17 where IC #1 is connected, the current path will go out of the #2 TPL_IN pins and go into the TPL_OUT pins through the TPL line when IC #2 is connecting.

To limit the hot plug current grade between 2 nodes, RSER and CISO value should not be changed.

6 Hot plug test platform

6.1 The hot plug test platform

NXP designed a validation tool to evaluate hot plug performance and reliability as shown in Figure 18.

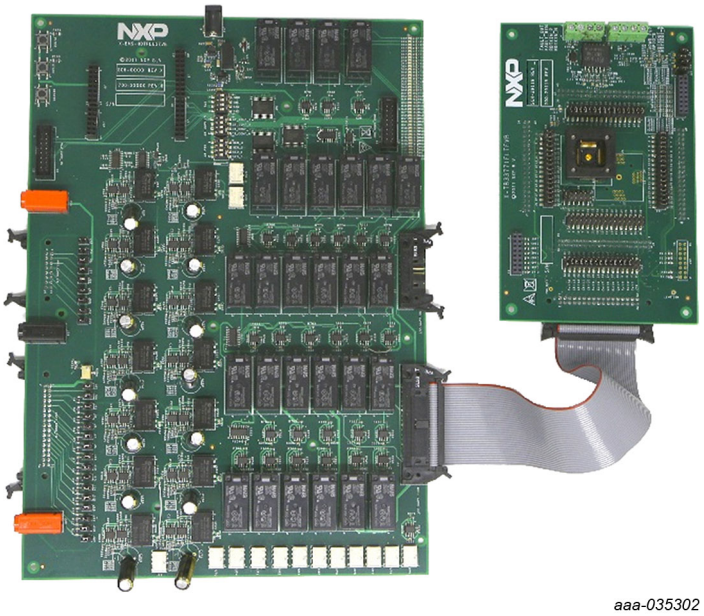

Figure 18. Hot plug platform

The connection sequences/combinations can be simulated by relay matrix which is shown in Figure 19. All sequences can be programmed by a GUI and performed by microcontroller.

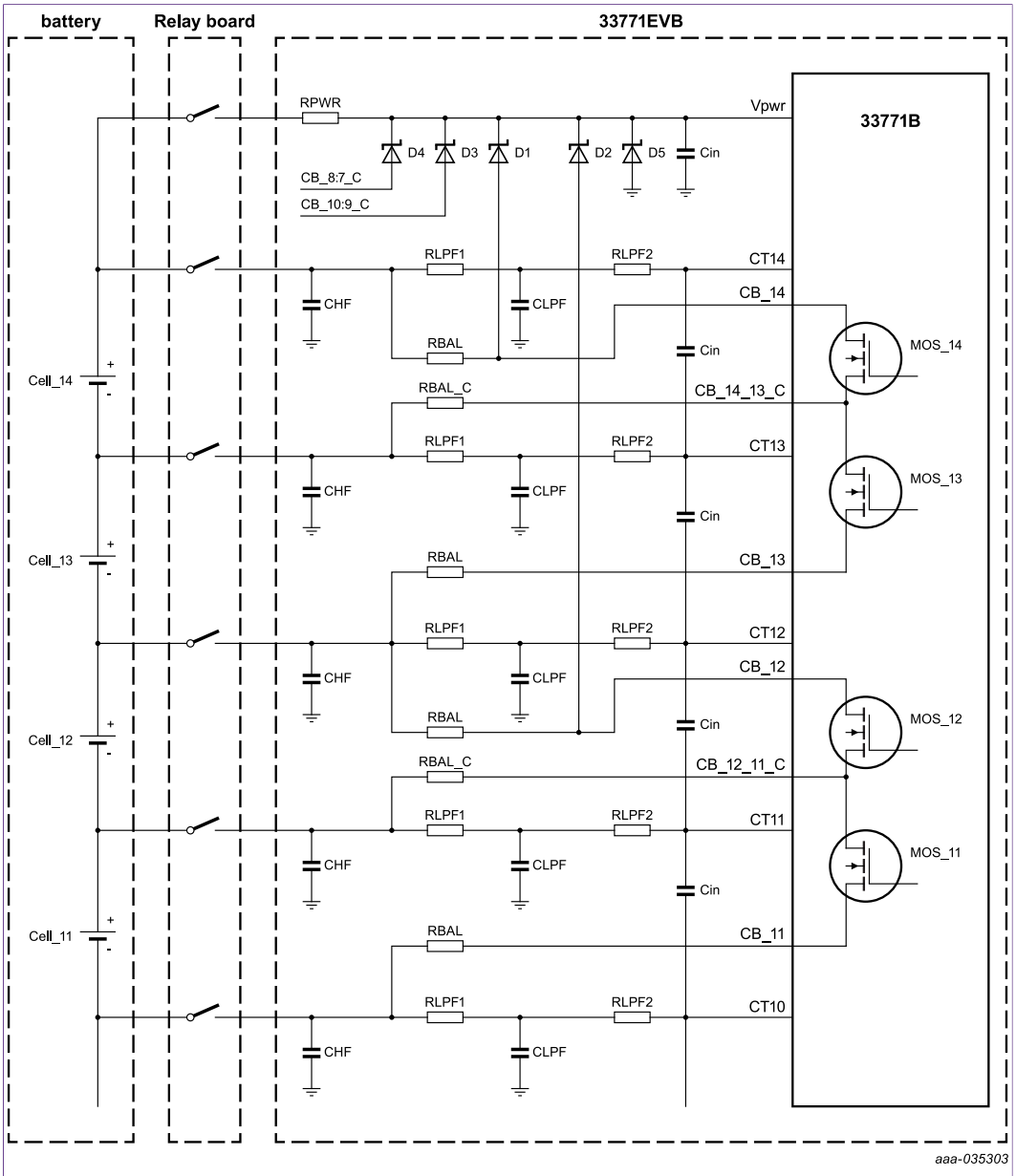

Figure 19. Hot plug platform scheme

6.2 The sequence determination for hot plug test

Nineteen pins connect to the battery:

V_{PWR}, Cell1, Cell2, …, Cell14, GND, battery negative_REF, ISN+, ISN–

The charging current for hot plug is generated after at least two pins are connected and the riskiest situation happens at this moment. The risk diminishes when a third pin is connected because the external capacitors have been precharged. Subsequent pins have less risk than the third pin, and so on. Therefore, all possible combinations with three pin connections are judged as high risk and fully validated.

7 How to mitigate hot plug risk

There are several prevention measures to mitigate hot plug risk. There is no hot plug risk for customers using the schematic shown in the data sheet.

- **Reducing C_{equ}**
  Reducing charging energy by decreasing the value of external capacitors could reduce the hot plug risk. Applied in many scenarios, it is effective and cost effective.
- **Reducing charging current by resistor**
  Reducing charging current by resistor is a compromise method to mitigate hot plug risk. Applied in many scenarios, it is effective and cost effective.
- **By-pass the current path by Zener or TVS**
  Changing the charging path for external capacitors and avoiding the current flowing through the IC could reduce hot plug.

7.1 End of line testing suggestions

It is possible to run some diagnostics, internal to the IC, during line testing. These allow detecting some pre-damaged structure in the ASIC due to some event that may have exceeded the IC's maximum ratings. Below is a list of the most efficient diagnostics that NXP suggests implementing at the end of line after the module has been attached to the battery.

#	Safety mechanism	Parametric Yes/No
SM01	OV and UV Functional verification	Yes
SM02	CTx Open Detect and Open Detect Functional Verification	Yes
SM03	Cell Voltage Channel Functional Verification	Yes
SM04	CTx Cell Terminal Leakage Monitor	Yes
SM36	Diagnostic of open between shunt and PGA	Yes
SM38	Diagnostic of measurement chain with minimum PGA gain	Yes
SM40	Cell balance open load detection	No
SM41	Cell balance shorted resistor detection	No
SM44	Cell Voltage plausibility test at system level	Yes
SM45	VPWR comparison to sum of cell voltages	Yes

8 Hot plug on system level for 12/48V battery

During assembly, disassembly, and during tests in a specific case, the BCC can be damaged by a high current (pulse) flow thorough the internal ESD structure.

The description is only valid for the following 12/48V BMS HW Architecture features:

- Shunt is soldered on the BMS PCB
- BMS main ground (power consumption) is connected to the shunt on the PCB
- BMS is powered from the Li-Ion battery, no galvanic isolation, one ground

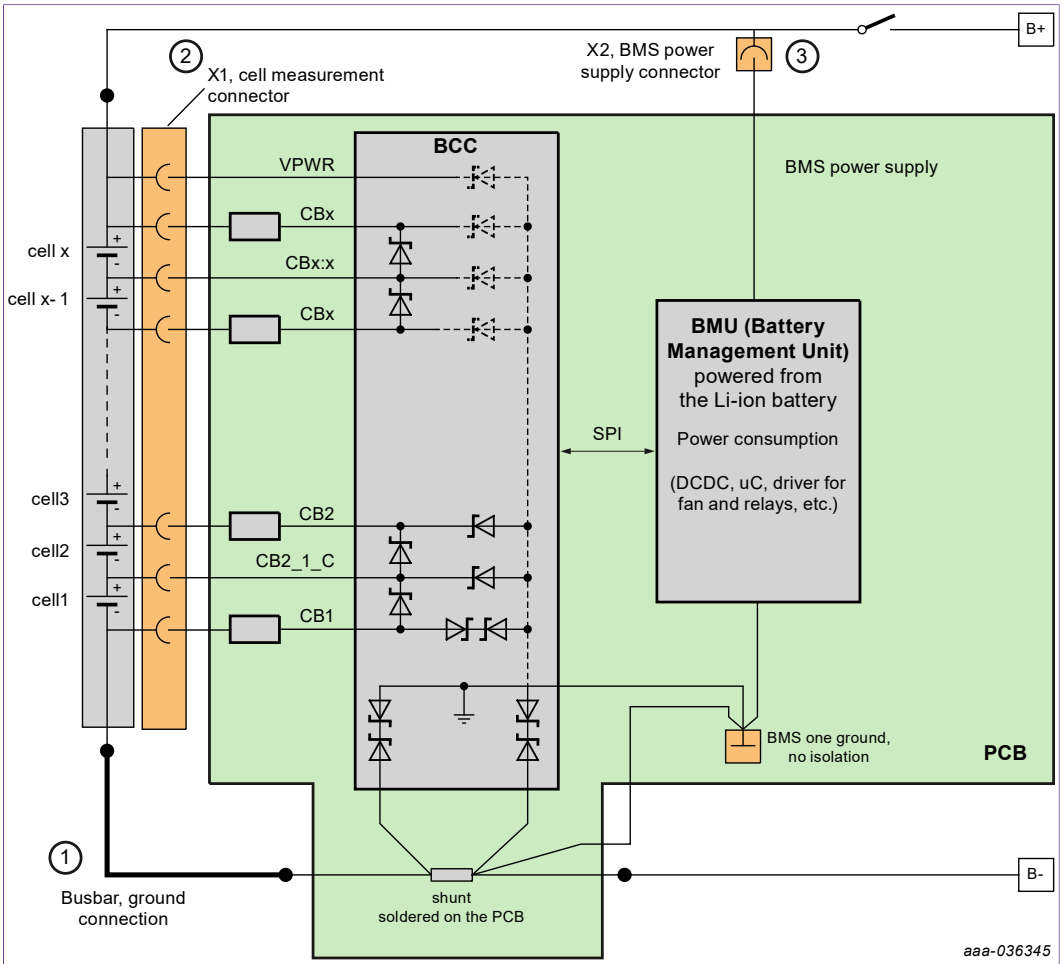

Figure 20. BMS HW architecture

8.1 Kind of the damage

The MC3377x is badly damaged, EOS on the following outputs: CB1, and/or CB2_1_C, and/or CB2, and/or CB3 and so on.

8.2 When does the damage happen?

Damage to the chip might occur during the following:

- Plugging the cables into the X1 or X2 connectors without a busbar between cell1 minus and the shunt
- Testing or software debugging without a busbar between cell1 minus and the shunt

8.3 Damage root cause

While the busbar between Cell1- and the shunt is interrupted, ground loops redirect the current consumption of the BMS through the BCC ESD structure. The current flows through the CB outputs to the cells. Depending on the current consumption or the height of the inrush current of the BMS, the cell balancing outputs and (ESD structure) will be badly damaged (EOS). In some cases, pre-damage is possible and could cause damage later in the fields.

The highest inrush current is usually during the hot plug. Depending on the architecture, up to ~100 A amperes peak could flow thorough the BCC ESD structure

Damage is also possible if the BMS operating current exceeds the maximum balancing current of 300 mA

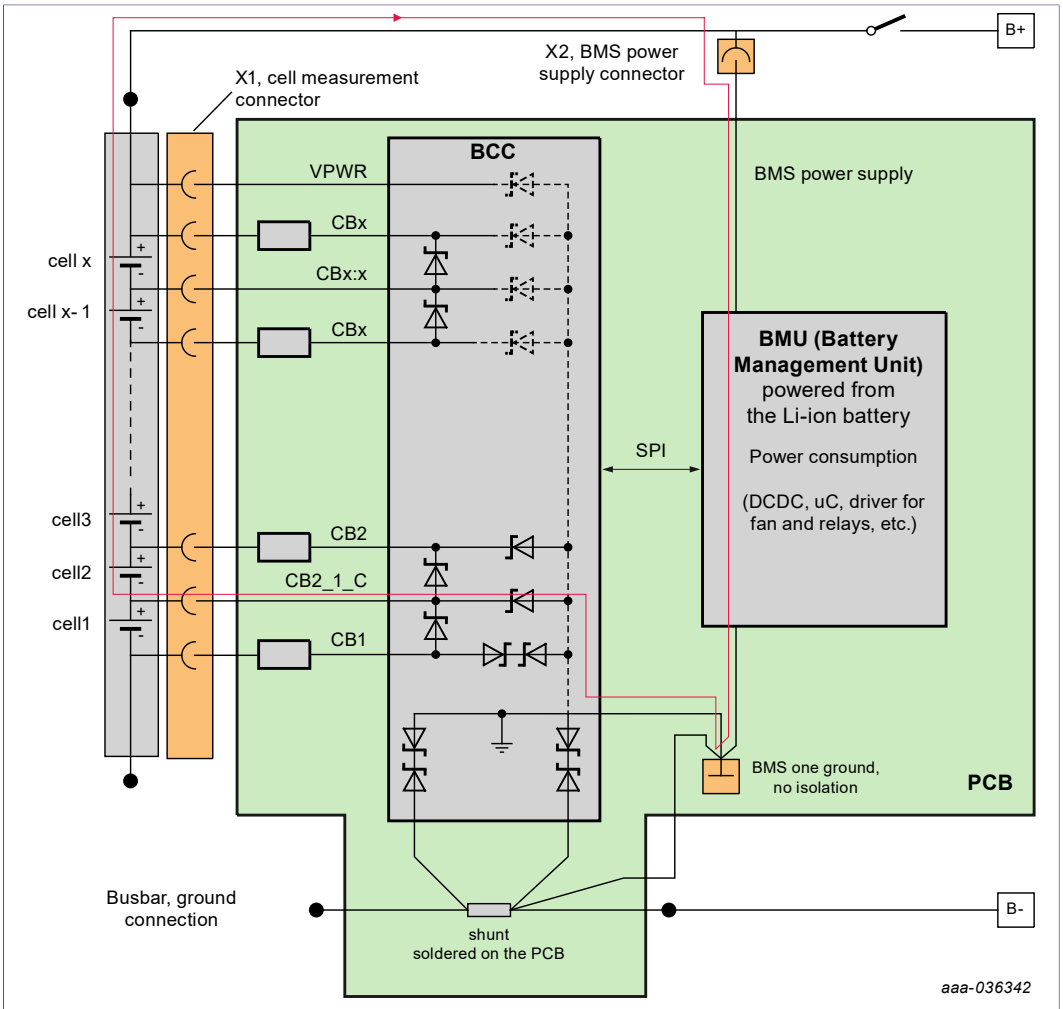

Figure 21. Current path that damages the chip

8.4 How to avoid damage during hot plug

During assembly of the battery, the busbar between the shunt and CELL1– must be connected at first, then all other connectors could be connected. NXP recommends connecting the BMS power supply connector as the last step.

During dismount of the BMS from the battery pack, first remove the power connectors, then remove all other connectors.

8.5 Assembly instructions

To avoid any damage to the BCC, follow these instructions during assembly or when connectiing the BMS to the battery pack:

1. Always connect the busbar beween CELL1- and the shunt on the BMS PCB prior to any other steps.
2. Connect the cell votage measurement connector to connection X1.
3. As the final step, connect the power supply connector to X2.

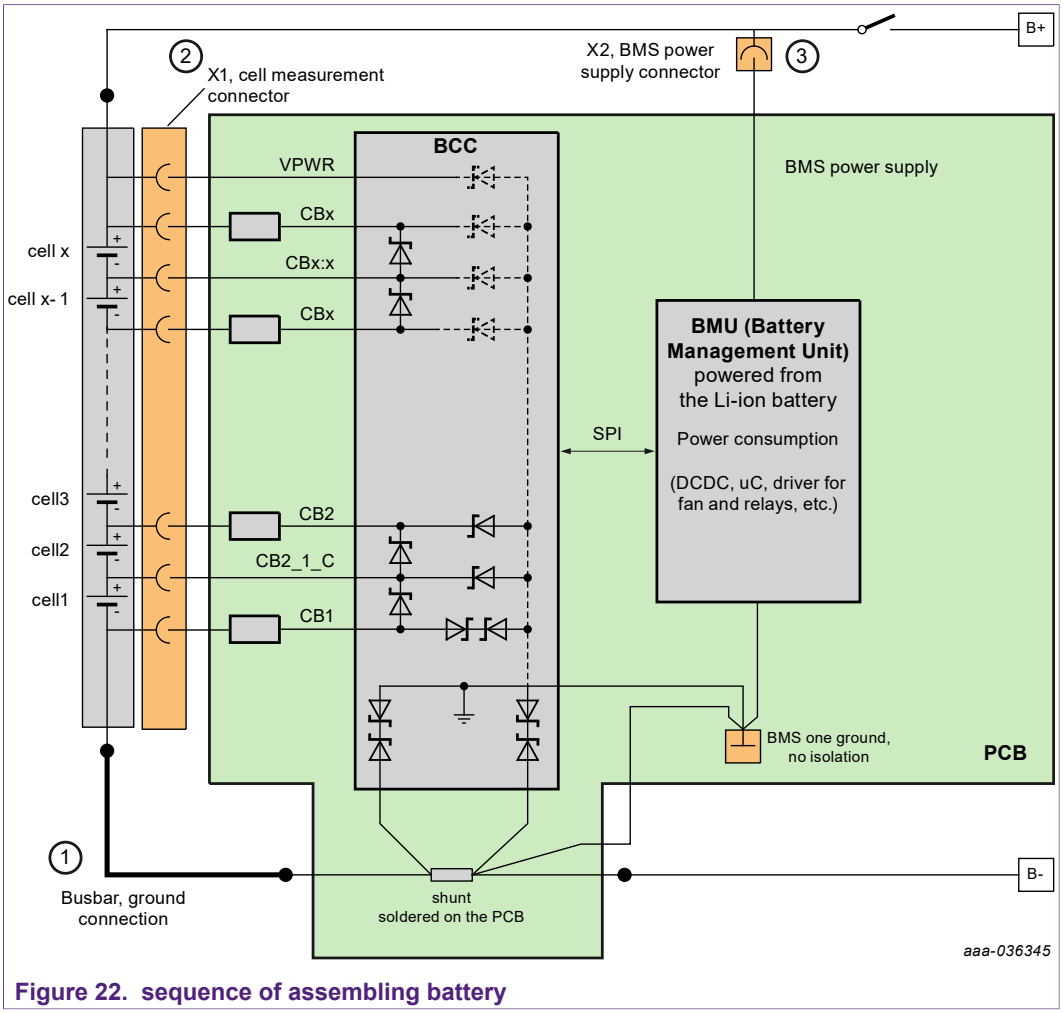

Figure 22. sequence of assembling battery

8.6 Dismount and disasembly instructions

To avoid damage to the BCC, follow these instructions during dismount or disconnection of the BMS from the battery pack.

1. Disconnect the power supply connector X2 prior to any other steps.
2. Disconnect the cell voltage measurement connector at X1.

3. Disconnect and remove the busbar between CELL1- and the shunt on the BMS PCB. Always perform the disconnection and removal of the busbar as the final diassembly step.

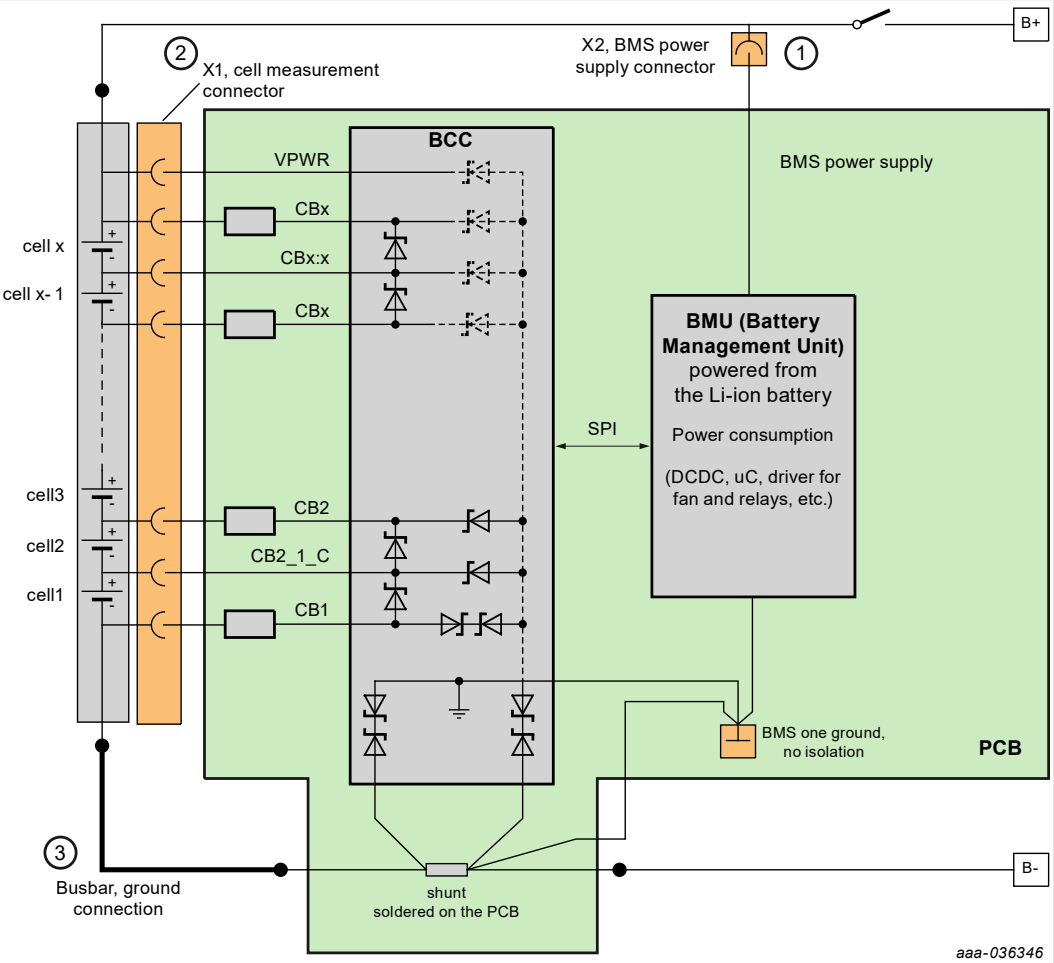

Figure 23. Sequence of disconnecting battery

8.7 Analysis, hot plug during assembly

During assembly, the following incorrect sequence will cause damage during the hot plug:

1. The busbar between Cell1- and the shunt is interrupted.
2. X2, BMS power supply connector is connected at first.
3. X1, Cell measurement connector is connecting at next, in worst case the connector pin CB1:2 is going to connect at first in the connector X1.
4. High Inrush current or the BMS operating current will flow through the BCC ESD structure.

The internal ESD structure of the BCC could be damaged as a result of the wrong sequence of assembly.

8.8 Analysis, hot plug during disassembly

During the disassembly, the following incorrect sequence will cause damage during the hot plug:

1. The busbar between Cell1- and the shunt is interrupted. If the BMS is in operating mode, depending on the operating current, the internal ESD structure of the BCC could be damaged.
2. X1, Cell measurement connector disconnecting at next, in worst case the connector pin CB2:1 is going to disconnect at last in the connector X1.
3. X2, BMS power supply connector is disconnected at last.

The internal ESD structure of the BCC could be damaged or predamaged as a result of the wrong sequence of assembly.

9 Conclusion

The hot plug prevention measure for MC33771/2x devices is accomplished by diverting the current path from the internal ESD structure. Some methods are:

- The internal ESD structure is strong enough to withstand the hot plug stress. Adding protection for hot plug on CT1 to CT7 is not necessary.
- for MC33771x (CT8 to CT14), four Zener diodes are needed to mitigate hot plug risk.
- A TVS is required between VPWR and CT14 pin when the V_{PWR} exceeds 55 V. If the V_{PWR} is lower than 55 V, the TVS is not necessary.
- NXP validates all hot plug components. Contact NXP if component modifications are needed to meet specific application needs.
- The current sense channel hot plug protection Zener is a back-to-back diode. Carefully design the circuitry according to the product data sheet.
- Special instructions for the assembly and dismount of the battery pack in a 48 V system must be strictly followed to avoid any damage to the BCC.

10 References

[1] **MC33771B**, Battery cell controller IC product data sheet. Contact your sales representative or FAE.

[2] **MC33771B**, Safety Manual. Contact your sales representative or FAE.

[1] **MC33771C**, Battery cell controller IC product data sheet. Contact your sales representative or FAE.

11 Revision history

Table 6. Revision history

Rev	Date	Description
1	20200413	Initial release

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