AN12377

Tuning I2C Timing In Slave Mode

Rev. 1 — April 2019 Application Note

1 Introduction

The I²C module is popular in most applications. Kinetis MCUs provide strong features on the I²C module, which is compatible with the I²C-bus specification and easy to interface with other devices. However, incorrect configuration may cause potential timing issues. This document shows how to configure the I²C timing of a slave device to meet application needs which apply to Kinetis parts that contain I2C IP instead of LPI2C.

2 Overview

The I²C specification defines detailed timing specifications to enable the I²C device to follow the same standard and make different devices working together. Figure 1. on page 1 shows the timing definition for tSU:DAT.

Contents

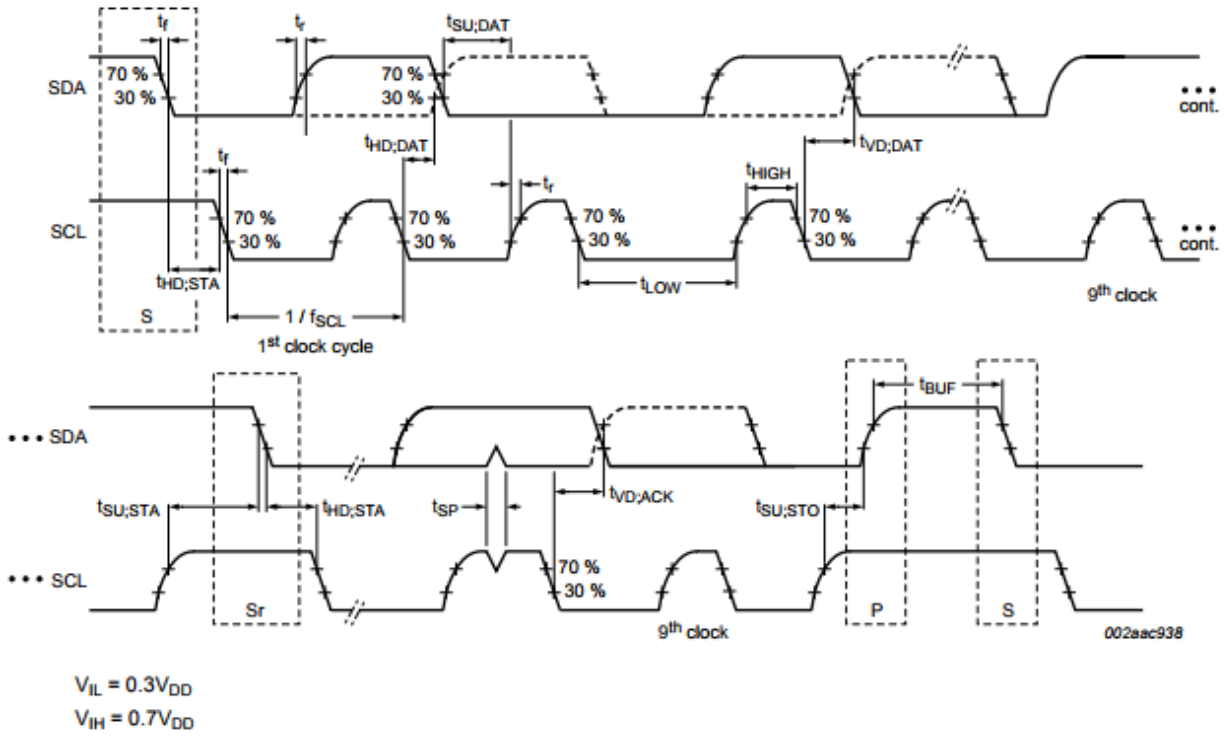

Figure 1. Definition of I2C timing

The Kinetis IP provides register I2Cx_F to tune the timing. The reference manual provides the reference table on how to impact the I²C baud rate and data hold time. For the slave mode, this register also heavily impacts the timing and incorrect settings may

cause timing issues. There might not be a clear explanation in the reference manual, but it must be consulted to get a correct configuration.

3 Timing issues caused by incorrect settings

When configuring the I^2C for a master device, most users know how to configure the I2Cx_F register to get the expected baud rate. However, when enabling it in the slave mode, users are not aware of the I2Cx_F function during the timing tuning and do nothing with the I2Cx_F register. In most customer applications, this possibly causes a timing issue. For example, when it works in the slave mode after events (interrupt of receiving new data or transmitting complete) occur, the slave device drives the SCL low by clock stretching and waits to handle I^2C events. It releases the SCL together with the SDA after writing/reading the I^2C data register when the I2Cx_F is set to 0. This causes the master to detect a wrong signal and fail to meet the SDA setup time requirement.

Figure 2. on page 2 shows the captured waveform.

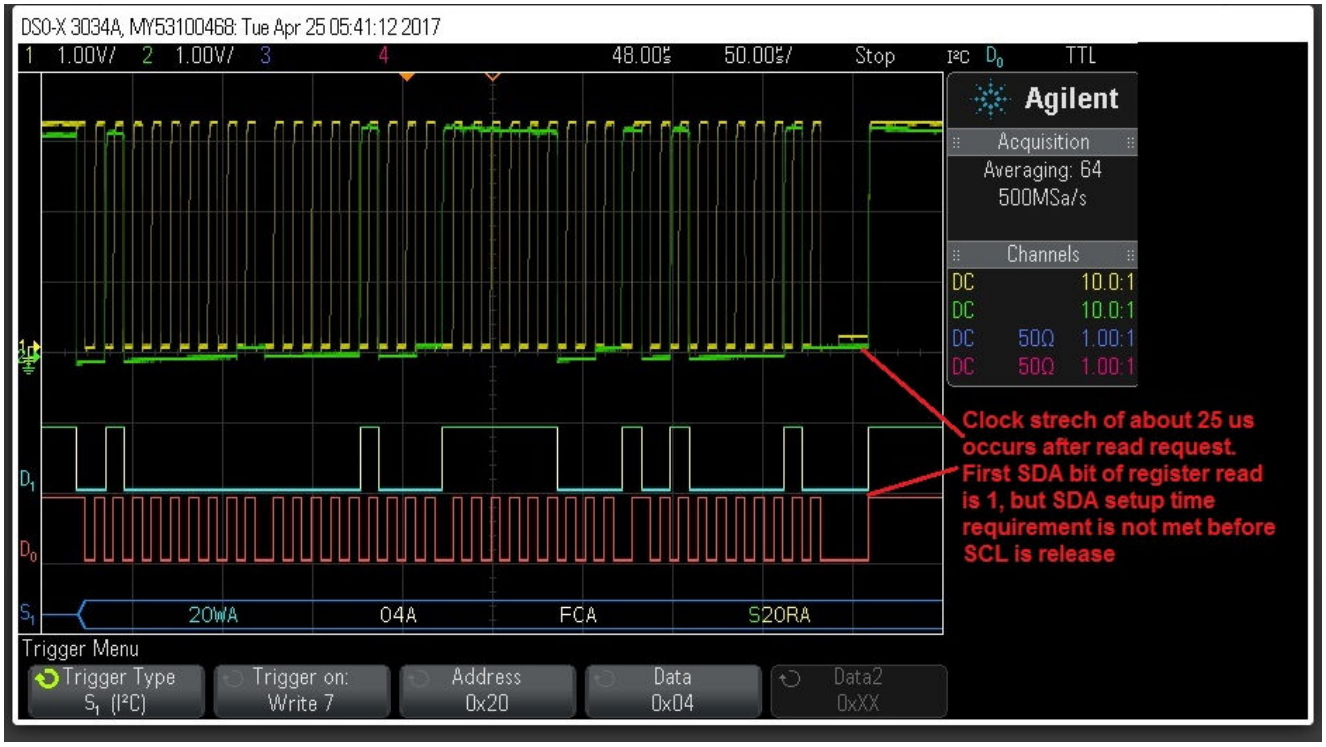

Figure 2. I2C signals with clock stretching

Figure 3. on page 3 shows the clock stretching timing.

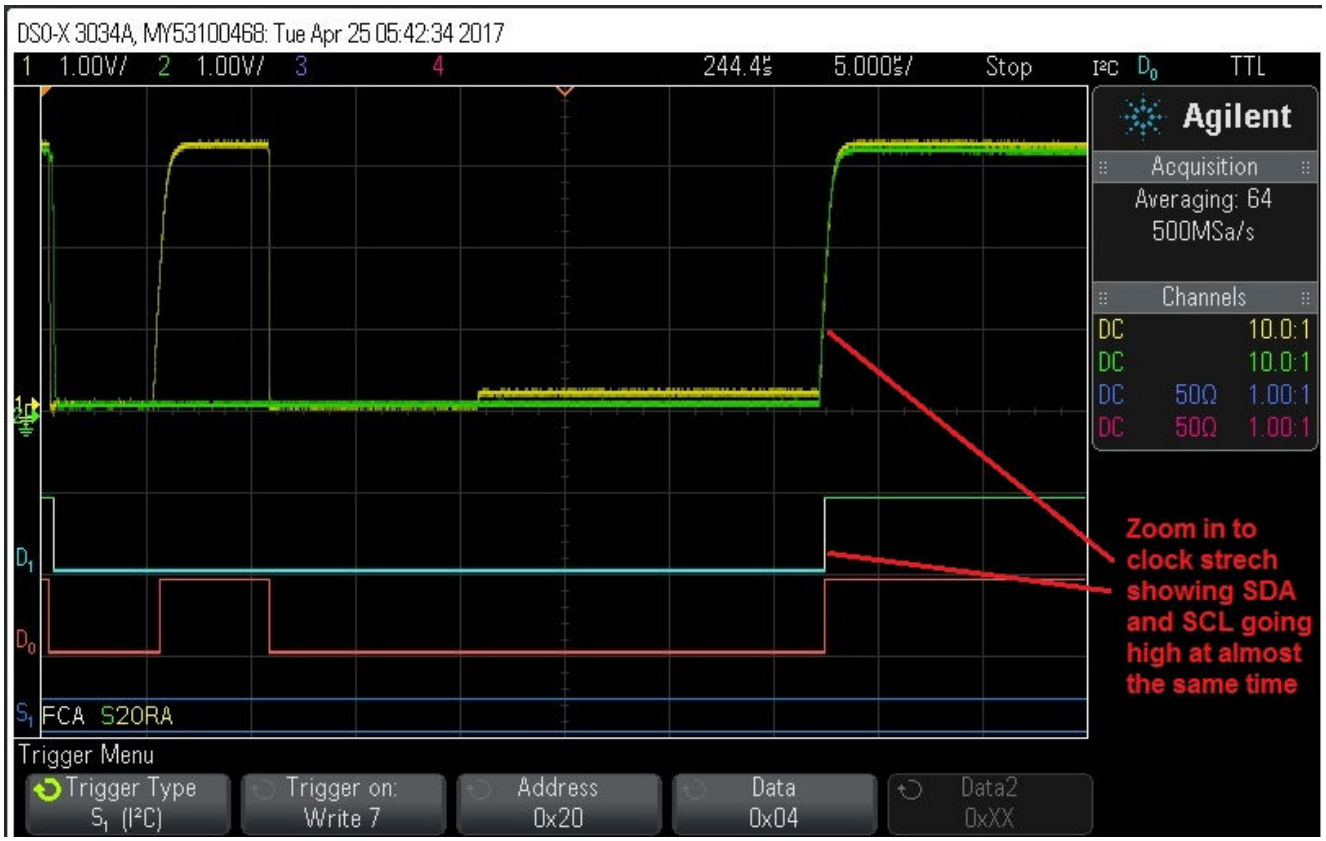

Figure 3. Clock stretching timing

Figure 3. on page 3 shows the SDA and SCL release at almost the same time. For the I²C timing definition to match the values in Figure 4. on page 3, the tSU:DAT minimum value must be around 100 ns in the fast mode and 250 ns in the standard mode. Therefore, the above timing violates the specification.

The tSU:DAT timing and the I²C specification give the characteristic parameters shown in Figure 4. on page 3.

Symbol	Parameter	Standard-mode		Fast-mode		Fast-mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
tSU:DAT	data set-up time	250	-	100	-	50	-	ns
Note	A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement tSU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr(max) + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.							

Figure 4. Characteristics of tSU:DAT

4 Tuning the timing using register I2Cx_F

Configure the I2Cx_F register to fix the timing issue and get the tSU:DAT using this formula:

SDA setup time = I2C module clock period (s) x mul x SDA setup value

Note to keep the SBRC bit field to be 0 in the I2Cx_C2 register when using this solution. Get the SDA setup value from Table 1. I2C setup value on page 4.

Table 1. I2C setup value

ICR (hex)	SDA Setup Value	ICR (hex)	SDA Setup Value	ICR (hex)	SDA Setup Value	ICR (hex)	SDA Setup Value
0	2	10	16	20	64	30	256
1	3	11	20	21	80	31	320
2	3	12	20	22	80	32	320
3	4	13	24	23	96	33	384
4	4	14	24	24	96	34	384
5	5	15	28	25	112	35	448
6	6	16	32	26	128	36	512
7	9	17	44	27	176	37	704
8	6	18	32	28	128	38	512
9	8	19	40	29	160	39	640
0A	10	1A	40	2A	160	3A	640
0B	12	1B	48	2B	192	3B	768
0C	12	1C	48	2C	192	3C	768
0D	14	1D	56	2D	224	3D	896
0E	16	1E	64	2E	256	3E	1024
0F	22	1F	88	2F	352	3F	1408
ICR : register value of bit field ICR of I2C_F							
SDA Setup Value : number of I2C function clock							

NOTE

Table 1. I2C setup value on page 4 is just for reference. Set the I2Cx_F to have a sufficient margin to meet the I^2C timing.

For example, when the I2CxF is set to 0x02 and the I^2C module clock frequency is 48 MHz, the setup time is calculated as:

Setup time = 1/48 MHz * 1 * 3 = 62.5 ns

When the I2Cx_F value and the setup time value are bigger, they can get a longer margin by setting the big value to I2Cx_F. However, this causes the I^2C bus to drop due to clock stretching. Clock stretching happens in the below condition. At the start of a single-bit communication, the master sends the first SCL clock on the bus and the slave samples this pulse and compares it with its own I2Cx_F configuration. If the slave's baud rate is lower than the master's baud rate, I^2C IP begins to stretch the bus. For example, if the master's baud rate is 400 kHz and the slave's baud rate is configured to be 100 kHz by the I2Cx_F register, the final I^2C SCL bus period is composed by the slave's 100-kHz SCL low period time and master's 400-kHz SCL high period time. The bus period is 0.5 * (1 / 100 K + 1 / 400 K) seconds, so the SCL bus is about 160 kHz.

It is recommended to set the slave's baud rate higher than the master baud rate and give a sufficient margin to meet the I^2C timing.

5 Conclusion

This document introduces a way to tune the I²C timing and meet the specifications by setting I2CxF correctly, which helps customers to solve I²C timing issues.

6 References

- I²C-bus Specification, Version 6.0, 4th of April 2014
- *KL16 Sub-Family Reference Manual with Addendum* (document KL16P80M48SF4RM)
- *Kinetis KL03 reference manual* (document KL03P24M48SF0RM)

7 Revision history

Table 2. Revision history on page 5 summarizes the changes done to this document since the initial release.

Table 2. Revision history

Revision number	Date	Substantive changes
0	03/2019	Initial release
1	04/2019	Updated Tuning the timing using register I2Cx_F on page 3.

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