AN12364

NTAG 5 - Bidirectional data exchange

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Document information

Information	Content
Keywords	Data transfer, SRAM, PHDC, arbitration
Abstract	How to transfer data, Pass-through, SRAM, PHDC, memory arbitration

Revision history

Rev	Date	Description
v.1.0	20200109	First official released version

1 Abbreviations

Table 1. Abbreviations

Acronym	Description
EEPROM	Electrically Erasable Programmable Read-Only Memory
GPIO	General-purpose input/output
I^2C	Inter-Integrated Circuit
NFC	Near field communication
PHDC	Personal Health Device Communication
POR	Power On Reset
PWM	Pulse width modulation
RF	radio frequency
SRAM	Static random-access memory

2 Introduction

NTAG 5 offers many ways for bidirectional data exchange. One of it is the "pass-through mode", which allows the NTAG 5 to be used for bidirectional data transfer from an NFC device to an I^2C-bus Host (e.g. a microcontroller).

The pass-through mode provides the SRAM for data communication and triggering mechanisms for the synchronization of the data transfer.

2.1 Potential applications

- Read out of data collected in an embedded device (logging data)
- Upload new data in the embedded device (e.g. firmware update of the microcontroller)
- Bidirectional communication with exchange of commands and data (e.g. execute functions in the microcontroller or execute authentication schemes)

3 Interface Arbitration for memory access

Interface Arbitration logic is provided to give access to RF interface and I^2C interface to access memory, without collisions. Two session register bits are provided to indicate which interface booted up successfully and it is available: RF_BOOT_OK and VCC_BOOT_OK.

Note: Tag can be "externally powered" by itself using energy harvesting, if V_{OUT} and V_{CC} are shorted.

Memory consist of EEPROM, SRAM and Session registers. SRAM is available only when tag is supplied by V_{CC} (VCC_SUPPLY_OK = 1b) and SRAM_ENABLE configuration bit is set to 1b. EEPROM and Session register are available when any of the supply sources is available.

Arbitration mode is applicable for I^2C slave use case mode only. For I^2C Master and GPIO/PWM use cases, no memory arbitration is done / needed.

There are four (4) arbitration schemes:

1. Normal mode [Section 4]
2. SRAM Mirror mode [Section 5] - shall be used when frequently changing data is passed over NDEF message. E.g., Host is reading temperature from temp. sensor and writing the value to the NTAG 5 User Memory Area, at the end of NDEF URL every 0.5 s, like: http://www.desireddomainwithSensorData.com/temp=023344&t1=25C. While SRAM provides unlimited write endurance, SRAM Mirror is better to use instead of writing to EEPROM. So host would be writing temperature to SRAM instead of EEPROM. Arbiter takes care that only one interface access the SRAM at the time.
3. SRAM Pass-through mode [Section 6] - for bulk data exchange (up to 256 B in one pass). Usually Host ↔ NTAG 5 ↔ NFC.
4. PHDC mode [Section 7] - for data exchange with Personal Health Care Device (e.g. blood pressure device, body temperature measurement device). SRAM Mirror on the first pages of User Memory is used for bulk data exchange, with help of arbitration mechanism.

Also [TNEP] mode is supported.

Note: NFC Forum defined TNEP is used where no special arbitration is needed on IC level.

4 Normal Mode

ARBITER_MODE [1:0] = 00b indicates normal mode. Memory is accessible by both the interfaces by “First come first serve” principle.

The arbiter locks to I^2C interface in following occasions:

- If the NTAG 5 is correctly addressed for the memory access on the I^2C interface, then set I^2C_IF_LOCKED = 1b if NFC_IF_LOCKED = 1b.
- If I^2C_IF_LOCKED = 1b then I^2C interface can access EEPROM and SRAM.
- RF reader can access (read/write) the NTAG 5 status registers via RF commands at any time. Any RF commands accessing EEPROM/CONFIGURATION memory will be returned with NAK.

I^2C_IF_LOCKED will be cleared if

- I^2C host writes to clear the register bit.
- If this is not done by the host, this bit will be automatically reset to 0 if Watch Dog Timer expires.
- At POR (all power sources).
- If I^2C supply switches off.

Note: If Watchdog timer is disabled, bit will not be cleared until transactions ends.

The arbiter locks to RF interface:

- If the NTAG 5 receives valid RF command and correctly addressed for memory access, then set NFC_IF_LOCKED = 1b if I^2C_IF_LOCKED = 1b.
- If NFC_IF_LOCKED = 1b then RF interface can access NTAG 5 memory.
- I^2C host can access (read/write) the TAG status registers via I^2C commands. Any I^2C commands to access memory will be returned with data NAK.

NFC_IF_LOCKED will be cleared automatically after:

- Completion of current valid RF command.
- At POR (all power sources).
- If RF field is switched OFF.

In Normal mode SRAM can be made available as part of memory or can disabled by configuring SRAM_ENABLE bit.

If NTAG 5 is VCC supplied VCC_SUPPLY_OK = 1b and SRAM_ENABLE = 1b, then SRAM is mapped at memory:

- I^2C interface: SRAM available at 2000h-201Fh.
- RF Interface:
  - Can be only accessed by SRAM_READ and SRAM_WRITE Commands.
  - Not mapped to any Block address from RF perspective.

If NTAG 5 is VCC supplied VCC_SUPPLY_OK = 1b and SRAM_ENABLE = 1b, then SRAM is not available for both the interfaces.

5 SRAM Mirror Mode

ARBITER_MODE [1:0] = 01b indicates SRAM Mirror mode. Memory is accessible by both the interfaces by “First come first serve” principle.

The arbitration scheme remains same as Normal mode.

To make this mode work, the tag needs to be powered by both RF and VCC.

- RF_FIELD_OK = 1b
- VCC_SUPPLY_OK = 1b
- SRAM_ENABLE = 1b

SRAM Mirror mode maps SRAM onto User memory (EEPROM) space. This enables unlimited writes to NDEF area. This mode is not used for bulk data transfer as the "pass through" mode [Section 6].

In this mode SRAM is mapped to Block 0h of EEPROM memory, for both RF to I^2C interfaces. Therefore underlaying EEPROM is not accessible when SRAM is mirrored.

In this mode the SRAM is mapped at memory:

- I^2C interface:
  - BLOCK0h to BLOCK3Fh
  - 2000h-203Fh
- RF Interface:
  - Can be accessed by SRAM_READ and SRAM_WRITE Commands.
  - READ_BLOCK, READ_MULTIPLE_BLOCK, WRITE_BLOCK commands to blocks BLOCK0h to BLOCK3Fh.

Mirrored SRAM area can be populated with pre-defined data on boot-up. Specified bytes of SRAM NDEF data get loaded into the SRAM. In this case, boot-up time gets extended.

6 SRAM Pass-Through Mode

ARBITER_MODE [1:0] = 10b indicates SRAM Pass-Through mode.

In this mode, the tag transfers data from RF to I^2C or vice versa using SRAM. SRAM is available only if the tag is VCC powered.

Conditions to be met that Pass-through mode is working:

- RF_FIELD_OK = 1b
- VCC_SUPPLY_OK = 1b
- SRAM_ENABLE = 1b

In Pass-through mode the SRAM is mapped at memory:

- From I^2C perspective: 2000h-203Fh (SRAM not mirrored on EEPROM)
- From RF perspective: 00h-3Fh SRAM memory address. Memory can be only accessed by SRAM_READ and SRAM_WRITE Commands (SRAM not mirrored on EEPROM).

The data transfer direction can be decided by the PT_TRANSFER_DIR session register bit:

- PT_TRANSFER_DIR = 0b, Data transfer direction is from I^2C host to RF reader.
- PT_TRANSFER_DIR = 1b, Data transfer direction is from RF reader to I^2C host.

Arbiter locks to only one interface at time. Since both the interfaces (RF and I^2C) are not active concurrently, a Terminator block mechanism is used to transfer the control from one interface (RFI/I^2C) to another interface (I^2C/RF).

Examples of pass-through mode (with source code) are described in:

1. AN12381 - NTAG 5 Firmware development for KW41Z [Application note]
2. AN12380 - NTAG 5 Android App [Application note]

6.1 Data Transfer mechanism RF to I²C Data transfer (RF reader to I²C host)

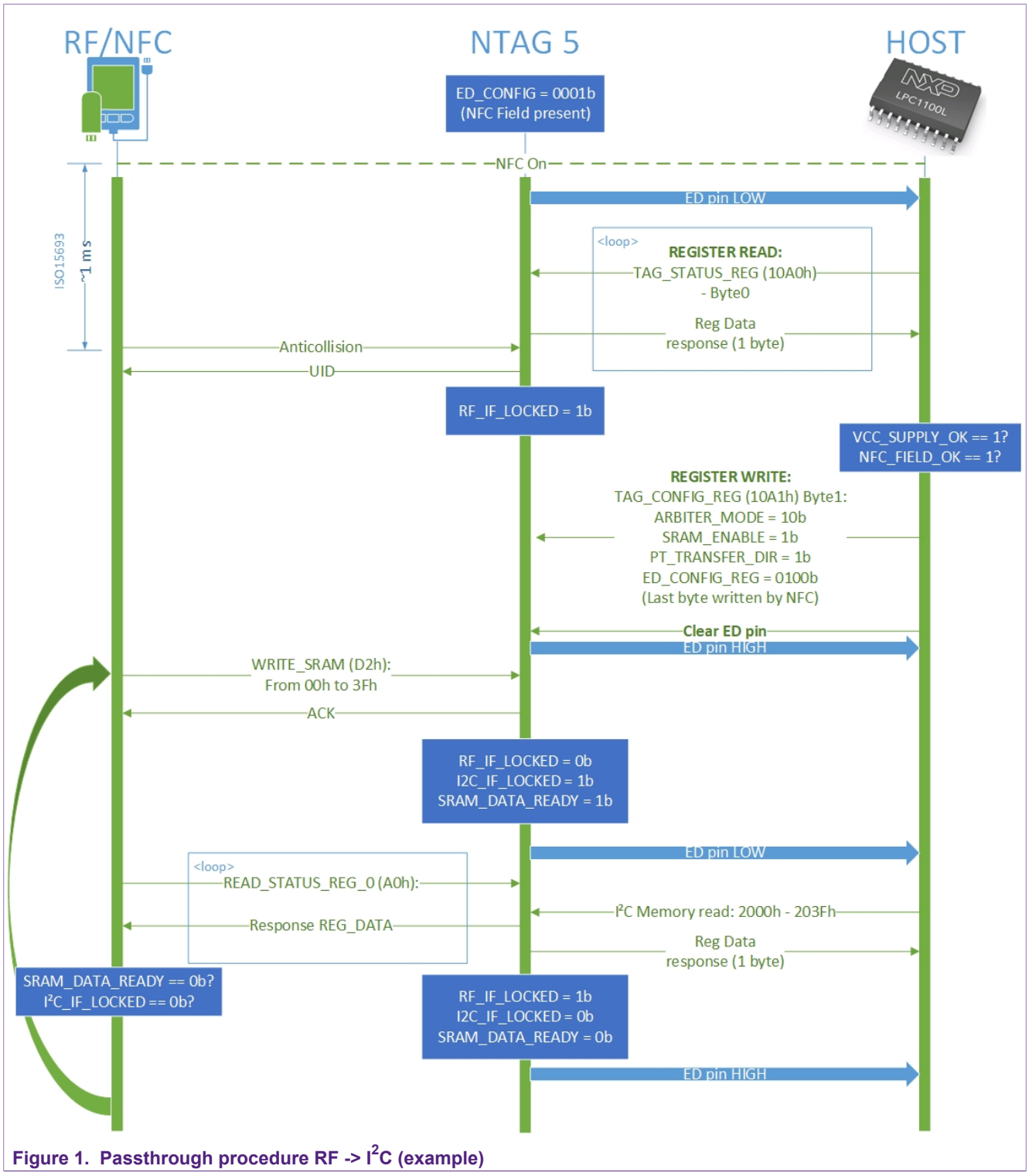

Figure 1. Passthrough procedure RF -> I²C (example)

Steps:

1. NTAG's configuration (start-up behavior) is set that ED pin will go LOW once NFC field is present
2. NFC field is present, 1 ms guard time (ISO15693) for NTAG to boot up
3. In the mean-time ED pin goes LOW
4. µC queries (sends I^2C commands in loop) for VCC and NFC field presence status registers
5. If both 1b, move on
6. µC reset Session registers (current session):
   - ARBITER_MODE: SRAM pass through
   - Enable SRAM memory
   - Pass-through direction: NFC->I2C
   - ED goes LOW when last byte (Byte3 – block 3Fh) of SRAM is written (ED_CONFIG_REG = 0100b)
7. Clear ED pin (ED pin is cleared i.e. released when writing 01h to the ED clear register ED_INTR_ CLEAR_REG (10ACh))
8. NFC can start writing to SRAM
9. When the last page of SRAM is written, ED pin is pulled LOW
10. NFC polls if data was read from SRAM and/or arbiter still keeps access locked to I^2C interface
11. I^2C side was notified through interrupt – ED pin, that data is waiting in SRAM. SRAM Memory can be read now
12. ED pin goes low, when last byte has been READ by I^2C interface (ED_CONFIG_REG = 0100b)
13. Arbiter unlocks access from I^2C interface and sets SRAM_DATA_READY bit to 0b. NFC polls for those and can restart SRAM WRITE loop with new data.

6.2 Data Transfer mechanism I²C to RF Data transfer (I²C host to RF reader)

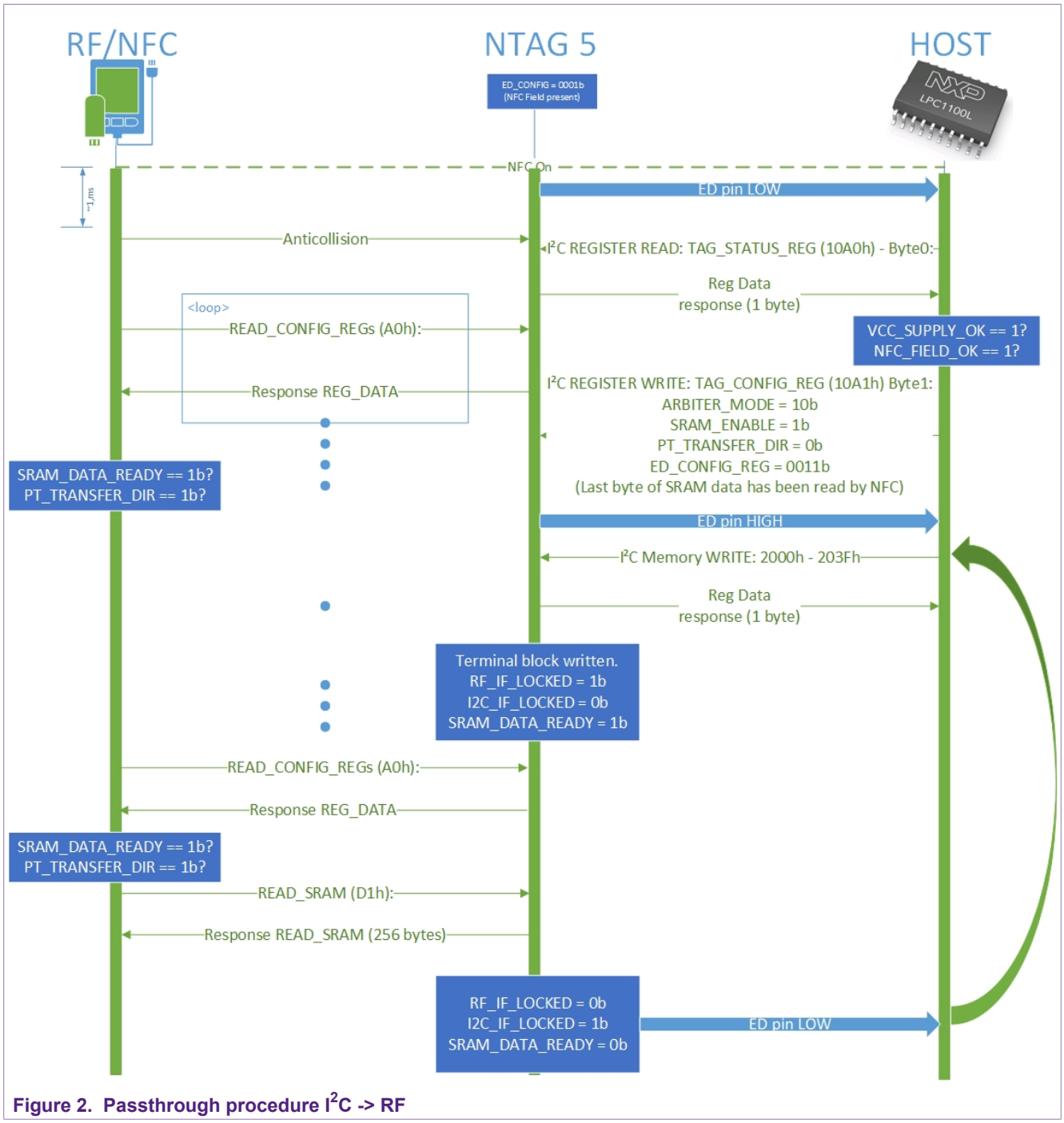

Figure 2. Passthrough procedure I²C -> RF

Steps:

1. NTAG's configuration (start-up behavior) is set that ED pin will go LOW once NFC field is present
2. NFC field is present, 1 ms guard time (ISO15693) for NTAG to boot up
3. In the mean-time ED pin goes LOW
4. RF polls when data is ready in SRAM (SRAM_DATA_READY)
5. I^2C host sets NTAG 5s session registers:
   - arbiter mode: pass-through
   - enable SRAM memory
   - transfer direction: $I^2C \rightarrow$ RF
   - configure ED pin to go low when last byte of SRAM page is read by NFC
6. I^2C host writes to SRAM memory (2000h - 203Fh)
7. When last byte of SRAM is written, Arbiter locks interface to RF and releases I^2C interface. SRAM_DATA_READY bit is set to 1b on NTAG 5.
8. SRAM_DATA_READY is 1b, RF interface can read SRAM now
9. When last byte of SRAM is read by NFC, Arbiter locks to I^2C interface and SRAM_DATA_READY bit is set back to 0b.
10. ED pin is pulled low
11. I^2C host can start to write another chunk of data or stop the pass-through.

7 PHDC mode

This mode is defined by NFC Forum to be used in Personal Health Device Communication. For more info, refer to [PHDC]. NFC Forum Reader/Writer Mode is used.

ARBITER_MODE [1:0] = 11b indicates SRAM PHDC mode.

The arbitration scheme remains same as Normal mode with exception of SRAM access for read.

To make this mode work, the tag needs to be powered by both RF & VCC.

- RF_FIELD_OK = 1b
- VCC_SUPPLY_OK = 1b
- SRAM_ENABLE = 1b

PHDC mode would map SRAM in user memory (EEPROM) space. SRAM is always mirrored to block0h. In PHDC mode the SRAM is mirrored on to Block 0h of EEPROM memory for both RF to I^2C interfaces.

In this mode the SRAM is mapped at memory:

- I^2C interface:
  - Can be accessed at BLOCK0h to BLOCK3Fh or
  - Can be accessed at 2000h-203Fh
- RF Interface:
  - Can be accessed by read or write commands to SRAM mirrored blocks BLOCK0h to BLOCK3Fh. NFC Forum commands which are used are specified in [PHDC]: NFC read and NFC write
  - Can be accessed by SRAM_READ and SRAM_WRITE Commands

SRAM access condition differs from Normal mode.

- I^2C Interface accessing SRAM
  - I^2C_IF_LOCKED =1b
  - I^2C SRAM read/write ongoing
  - IF RF requests for SRAM access.
    - RF read/write access:
      - The current ongoing I^2C access is halted and I^2C clock is stretched after completing the current Byte read or write access of I^2C interface.
      I^2C_IF_LOCKED = 0 and NFC_IF_LOCKED =1
      - RF gets the access to read/write SRAM.
      - After RF reads/writes SRAM, I^2C transaction is resumed.
      I^2C_IF_LOCKED = 1 and NFC_IF_LOCKED =0

8 Configuration and SRAM memory password security

SRAM and EEPROM used for bidirectional data exchange can be optionally also password protected. More details can be found in [Application note].

9 References

[1] NFC Forum specification, Tag NDEF Exchange Protocol - Technical Specification Version 1.0 2019-04-24 [TNEP] NFC Forum™
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[3] AN12366 - NTAG 5 Memory Configuration and Scalable Security, doc.no. 5305xx
https://www.nxp.com/docs/en/application-note/AN12366.pdf

[4] RM00221 - NTAG 5 Android Application development, doc.no. 5318xx
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[5] RM00222 - NTAG 5 KW41 firmware development, doc.no. 5319xx
https://www.nxp.com/docs/en/reference-manual/RM00222.pdf

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