AN11775

NXQ1TXH5/101 one-chip 5 V Qi wireless transmitter

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Document information

Info	Content
Keywords	NXQ1TXH5/101, NXQ1TXL5/101, wireless charger, A11 Qi coils, low power, WPC
Abstract	This application note describes the NXQ1TXH5/101 wireless charger solution designed for A11 Qi coils. It is based on the NXP Semiconductors NXQ1TXH5/101 fully integrated wireless power transmitter product for Qi compliant 5 V low-power transmitters.

Revision history

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1. Introduction

Fig 1. NXQ1TXH5/101 IC

This application note describes the NXQ1TXH5/101 wireless charger solution designed for A11 Qi coils. It is based on the NXP Semiconductors NXQ1TXH5/101 fully integrated wireless power transmitter product for Qi compliant 5 V low-power transmitters.

The NXQ1TXH5/101 comes in a 5 mm × 5 mm HVQFN32 package. It implements all the logic and power electronics required to realize a compact ultra-low component count 5 W Qi power transmitter application. To complete the whole application, only a handful of small passive components and a transmission coil are required. The application operates from a 5 V power supply (e.g. a USB adapter).

In this application note guidelines are given for the implementation of a fully operating wireless power transmitter. Electrical, thermal and compliance aspects are covered. Recommendations for tuning and potential customizations are explained.

1.1 Features

- Single-chip WPC 1.2 Qi-compliant device for A5/A11/A12/A16 5 V single-coil low-power transmitter
- Operates from 5 V supply
- Integrated high efficiency full-bridge power stage with low EMI radiation meeting EN55022 radiated and conducted emission limits
- Very few external components required, minimizing cost and board space
- Extremely low-power receiver detection circuitry by integrating an analog ping circuit; standby (wait-state) power 10 mW (typical)
- Power stage protected against overcurrents and overtemperature
- Dual-channel Amplitude Shift Keying (ASK) demodulation
- Demodulates communication packets from Qi-compliant receivers
- PID regulation for power drive and control
- Internal 1.8 V digital supply generation
- LED (×2) and buzzer outputs
- NTC input for external temperature check and protection
- On-chip thermal protection

- Small HVQFN 32-pin package (5 mm × 5 mm) with 0.5 mm pitch
- FOD with WPC receiver versions 1.2 and 1.1 and for legacy receiver support; when a WPC 1.0 receiver is detected, FOD is switched off automatically
- The FOD configuration can be adjusted using external resistors to compensate for application differences to meet Qi certification requirements
- Smart Power Limiting (SPL) function to adapt to power-limited 5 V supplies
- Static Power Reduction (SPR) function to limit power consumption
- Peak efficiency > 75 %
- Excellent low power (< 2 W) transfer efficiency. Ideal for charging wearables

1.2 Powering an NXQ1TXH5/101 application

The power supply that provides the power to the NXQ1TXH5/101 wireless power transmission application must be able to supply a stable and sufficiently high voltage to the application board. Especially when the wireless power transmitter operates at a relatively high power level, the stable and sufficient high voltage is required. Some commonly available USB adapters come with a thin (and sometimes long) USB cable. At high current, the voltage drop across that cable may cause the voltage arriving at the NXQ1TXH5/101 application board to drop well below 5.0 V and to vary significantly with current consumption. This voltage drop can cause the NXQ1TXH5/101 application to enter a fault state prematurely.

Use a good quality 5 V 2 A USB adapter. It must be compliant with the USB specification and equipped with at least an AWG24 power cable (not longer than approximately 1 m). Adapters with built-in cable compensation can also overcome the problem of thin (and long) wires.

2. Functional description

2.1 Circuit description

In this section, aspects relating to the NXQ1TXH5/101 application and the circuitry are described and explained. For more information about the IC, see the NXQ1TXH5/101 *data sheet* (Ref. 2).

2.1.1 Power transfer

The power transfer section is on the right-hand side in the circuit diagram. The NXQ1TXH5/101 IC contains a full (4-MOSFET) power bridge that drives the series-resonant network. The network consists of capacitance C_p (realized by connecting capacitors C3, C4, C5, and C6 in parallel) in series with the transmitter coil L_p (connected to terminals IND1 and IND2). The combination of C_p and L_p is also called the LC resonant tank.

The NXQ1TXH5/101 regulates the amount of power that the coil transmits by varying the switching frequency of the bridge. At high frequency (e.g. 205 kHz), power transfer is low and at low frequency (e.g. 110 kHz), power transfer is high.

If at 205 kHz switching frequency the power transfer is still higher than required by the load (Qi receiver), the NXQ1TXH5/101 IC reduces the operation duty cycle to arrive at the required power transfer level. During the on-period of the duty cycle, the switching frequency is 205 kHz.

To limit ElectroMagnetic Interference (EMI), snubber networks are connected from the two bridge-output nodes to ground (resistor R1/capacitor C1 and resistor R2/capacitor C2). Supply decoupling of the power stage is implemented using capacitors C7, C8, C9, and C10.

Pins ASEN1, ASEN2, and VSEN monitor the behavior of the LC resonant tank. To do the monitoring properly, the LC-tank midpoint voltage is rectified, filtered, and attenuated before the signal is fed to these pins. Capacitors C15 to C18, diode D1, and resistors R13 to R18 make up the interface circuit.

Internally, the NXQ1TXH5/101 DSP core processes the signals. FOD and ASK information is derived from it.

2.1.1.1 Optimizing the LC resonant tank

According to Wireless Power Consortium (WPC) Qi specification (Ref. 1), values have been specified for both the inductance (L_p) and the capacitance (C_p) in the resonant tank.

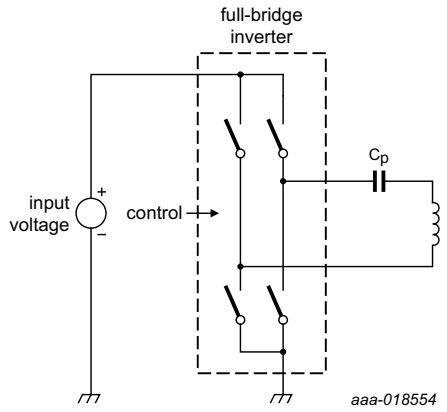


Fig 2. Qi power transmitter principle - full-bridge inverter plus resonant tank

The assembly of the inductor coil and the shielding and accessories must have an inductance (L_p) of 6.3 μH (±10 %). The capacitance (C_p) of the series capacitor must be 0.4 μF (±5 %). The input voltage to the full-bridge inverter must be 5 V (±5 %). The combination of L_p and C_p is intended to give the tank a target resonant frequency of:

$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L_p \cdot C_p}} \approx 100.26\ kHz\ (\pm 8\ \%) \quad (1)$$

Under various conditions, tuning the resonant tank to perform optimally can be an option. For example, when the inductance of a specific transmitter coil assembly is high, a lower value for the capacitance can be chosen to shift the resonant frequency towards the target resonant frequency. The result of failing to do so can be that the inverter/resonant tank combination cannot transfer the required amount of power at the lowest operating frequency (110 kHz). Tune the C_p capacitance value through a small series of practical experiments. When C_p consists of a number of capacitors in parallel, make sure that the individual capacitances have approximately the same value (preferably not more than 20 % difference). This way of tuning leads to the best performance when a specific transmitter coil is chosen.

When the resonant frequency of the resonant tank is shifted slightly upwards (e.g. 105 kHz), realizing maximum power transfer can be easier. When transferring power to a critical receiver, a slightly upward frequency shift is beneficial. However, the resonant frequency must never be so close to 110 kHz that the spread in component values causes it to be higher than 110 kHz.

2.1.2 Crystal oscillator

The NXQ1TXH5/101 uses an external low-cost 32.768 kHz crystal with a better than 1 % accuracy. The crystal must support a load capacitance of approximately 12 pF (the load capacitance is embedded in the NXQ1TXH5/101). It is connected to the oscillator input pin (XTAL_IN) via a 2.2 pF series capacitor. To prevent oscillations or overtones, the length of the crystal connections must be approximately 1 cm. Do not connect the crystal to the NXQ1TXH5/101 using vias. Connect it directly on the top layer of the PCB. If possible, shield the crystal by connecting the casing to ground.

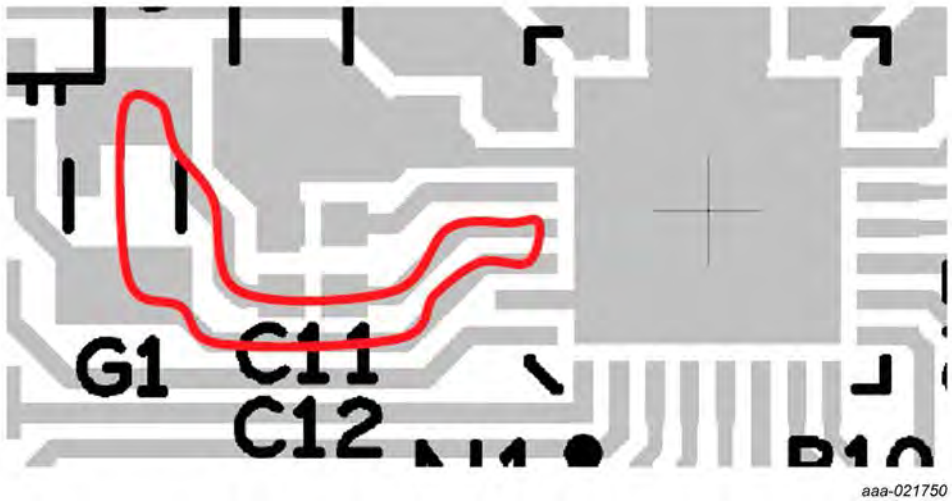


Fig 3. Crystal to NXQ1TXH5/101 IC typical connection layout

2.1.3 NXQ1TXH5/101 configuration

The NXQ1TXH5/101 operation behavior is set with 5 resistors: R7 to R11. The IC ‘reads’ its configuration by the pulling the CNF1, CNF2, CNF3, and CNF4 outputs low, while measuring the voltage that is being produced on pin CNF_IN. In this way, the resistor combinations R7/R11, R8/R11, R9/R11 and R10/R11 define the NXQ1TXH5/101 operating characteristics.

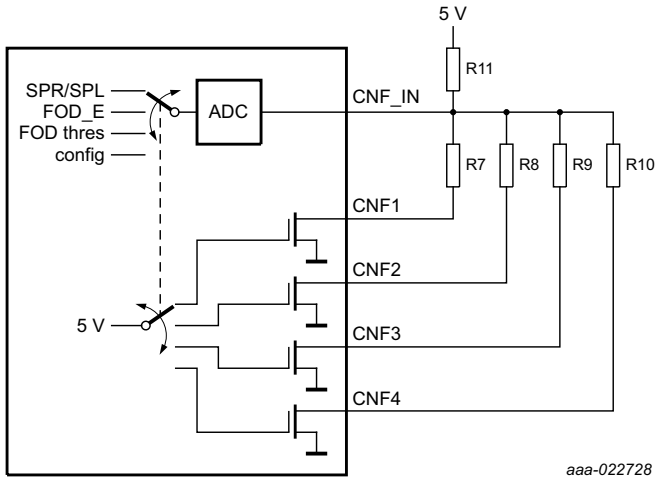


Fig 4. NXQ1TXH5/101 configuration

2.1.3.1 Static Power Reduction (SPR) and Smart Power Limiting (SPL) (CNF1 pin)

Resistor combination R7 and R11 sets SPR and SPL behavior of the NXQ1TXH5/101 IC. The SPR/SPL operational behavior is read by measuring the voltage on the CNF_IN pin while CNF1 is low.

$$V_{CNF\_IN} = \frac{R7}{R7 + R11} \cdot V_{DDP} \quad (2)$$

Table 1 lists the SPR level and SPL status that result from a certain V_{CNF_IN} voltage. In the table, V_{DDP} (the supply voltage) is assumed to be 5.0 V. However, levels are automatically compensated for deviations/changes in V_{DDP}.

Table 1. SPR and SPL

Input voltage on pin CNF_IN (CNF1 is active)	SPR	SPL
V_{CNF_IN} < 0.04 V	off (maximum 2 A)	off
0.085 V < V_{CNF_IN} < 1.29 V	SPR = (V_{CNF_IN} / 1.2) + 0.43 (A)[1]	on
1.335 < V_{SPR} < V_{DDP} (V_{DDP} is maximum input level)	off (maximum 2 A)	on

[1] This formula assumes V_{DDP} = 5 V; the results are automatically adjusted to compensate for changes in the supply voltage level. CNF_IN in V.

SPR limits the supply current independently of the supply voltage. This feature can be used, for example, when the supply is taken from a limited USB source. To detect if the SPR setting via the CNF1 pin has changed, the CNF_IN pin is sensed every 3 s after start-up. The NXQ1TXH5/101 limits the power accordingly.

Not mounting resistor R7 (leave the connection open) disables SPR. In that case, SPL remains functional. SPR can also be disabled by connecting the CNF1 pin directly to the CNF_IN pin (which is equivalent to R7 = 0 Ω). Connecting the CNF1 pin directly to the CNF_IN also disables SPL functionality.

SPL limits the supply current when the 5 V supply (V_{DDP}) drops below the SPL threshold (4.2 V). Even if the receiver requests more power, SPL continues to limit the output power until the supply voltage recovers.

SPL can be disabled by connecting the CNF1 pin directly to the CNF_IN pin (which is equivalent to R7 = 0 Ω). Connecting the CNF1 pin directly to the CNF_IN also disables SPR functionality.

A proprietary application that e.g. operates from a 3.6 V battery source (e.g. low-power application for wearables) can be realized by disabling SPL. However, to protect the power supply, SPL is mandatory for a Qi certified application.

The SPR and SPL are relatively slow power limiting mechanisms. They are intended to prevent long-term overload conditions on the supply adapter. If the supply voltage of a power adapter collapses near instantly because of an overload condition, the SPR and SPL mechanism may not be fast enough to prevent the collapse.

2.1.3.2 FOD (CNF2 and CNF3 pins)

The NXQ1TXH5/101 features FOD functionality according to the WPC 1.2 and WPC 1.1 standard. When the NXQ1TXH5/101 IC notices that too much power is lost in the wireless power transfer path (e.g. a metal object like a coin), the NXQ1TXH5/101 enters the FOD fault state.

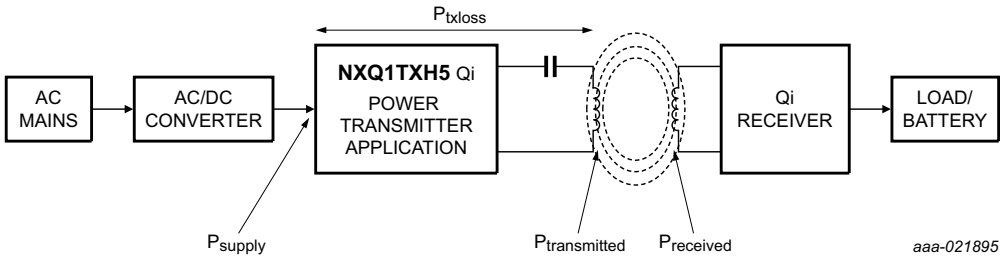


Fig 5. Power transfer chain

The NXQ1TXH5/101 can calculate the amount of power it is transmitting with Equation 3:

$$P_{transmitted} = P_{supply} - P_{txloss} \quad (3)$$

Where:

- P_{supply} is calculated from the input voltage and the input current that the IC measures
- P_{txloss} is the amount of power loss in the wireless transmitter electronics (IC and peripheral circuit)

P_{txloss} must be calculated. To estimate/calculate the power loss in the transmitter electronics, the NXQ1TXH5/101 uses Equation 4:

$$P_{txloss} = I_{RMS(coil)}^{2} \cdot FOD\_E \quad (4)$$

Where:

- $I_{RMS(coil)}$ is the RMS current that flows in the transmission coil. The NXQ1TXH5/101 IC calculates the magnitude of this current internally
- FOD_E is an equivalent loss resistance, consisting of the internal resistance in the IC, the PCB resistance, and the AC resistance of the transmission coil.

The FOD_E value is read by measuring the voltage on the CNF_IN pin while CNF2 is low. So, FOD_E is set with resistor combination R8/R11.

$$V_{CNF\_IN} = \frac{R8}{R8 + R11} \cdot V_{DDP} \quad (5)$$

The default value for FOD_E is selected by connecting pin CNF2 directly to pin CNF_IN (which is equivalent to R8 = 0 Ω).

Table 2. CNF2: FOD_E parameter

Input voltage on pin CNF_IN (CNF2 is active)	FOD_E
V_{CNF_IN} < 40 mV	default value for FOD correction (280)
85 mV < V_{CNF_IN} ≤ 1.29 V	400 × (V_{CNF_IN}/ 1.5) + 135[1]
1.335 V < V_{CNF_IN} ≤ V_{DDP} (V_{DDP} is maximum input level)	reserved

[1] This equation assumes V_{DDP} = 5 V. The results are automatically adjusted to compensate for changes in the supply voltage level.

Details about FOD configuration can be found in the NXQ1TXH5/101 FOD configuration document (Ref. 4). This document is available through your NXP sales representative.

In addition to the transmitted power ($P_{transmitted}$), the NXQ1TXH5/101 IC also knows the power that was received by the Qi receiver ($P_{received}$). That information is communicated from the Qi receiver to the Qi transmitter with Amplitude Shift Keying (ASK) modulation of the absorbed power (by the Qi receiver).

It is not uncommon that some power is lost in the wireless transfer from Qi transmitter to Qi receiver. Only when power loss gets too high, for example because power is being absorbed by a metal object (typically a coin or similar), it can be desirable to halt power transfer. A foreign object like that can heat up considerably and jeopardize safety. The power loss level that is considered acceptable can be set with the FOD threshold level through CNF3.

The FOD threshold level (FOD_T) is read by measuring the voltage on the CNF_IN pin while CNF3 is low. Thus, with resistor combination R9/R11, the FOD threshold is set.

$$V_{CNF\_IN} = \frac{R9}{R9 + R11} \cdot V_{DDP} \quad (6)$$

FOD can be disabled by connecting pin CNF3 directly to pin CNF_IN (which is equivalent to R9 = 0 Ω).

Table 3. CNF3: FOD_T parameter

Input voltage on pin CNF_IN (CNF3 is active)	FOD_T level
V_{CNF_IN} < 40 mV	no FOD
250 mV < V_{CNF_IN} ≤ 1.29 V	V_{CNF_IN} / 1.5 (W)[1]
1.335 V < V_{CNF_IN} ≤ V_{DDP} (V_{DDP} is maximum input level)	350 mW (default value)

[1] This equation assumes V_{DDP} = 5 V. The results are automatically adjusted to compensate for changes in the supply voltage level.

When FOD is enabled, the following rule applies:

if $P_{transmitted} - P_{received} > P_{FOD\_threshold}$
then {halt power transfer, enter fault state}
else {normal operation}

2.1.3.3 LED and buzzer mode (CNF4 pin)

The LEDs (H1 and H2) and the optional buzzer implement an elementary visual and audial user interface. The application works without implementing the LEDs and the buzzer. However, for Qi certification, at least one LED is required. Also, end users may appreciate some form of feedback regarding the operation and status of the application.

Resistor combination R10/R11 sets the LED and buzzer behavior of the NXQ1TXH5/101 IC. The mode is read by measuring the voltage on the CNF_IN pin while CNF4 is low.

$$V_{CNF\_IN} = \frac{R10}{R10 + R11} \cdot V_{DDP} \quad (7)$$

Table 4 lists the modes that result from a certain V_{CNF_IN} voltage. In the table, V_{DDP} (the supply voltage) is assumed to be 5.0 V, but levels are automatically compensated for deviations/changes in V_{DDP}.

Table 4. LED and buzzer configuration set via the CNF_IN pin (when CNF4 is active)

Input voltage on the CNF_IN pin (when CNF4 is active)	R10[1]	LED/buzzer mode
V_{CNF_IN} < 0.04 V	0 Ω[2]	1
0.085 V < V_{CNF_IN} < 0.165 V	10 kΩ	2
0.210 V < V_{CNF_IN} < 0.290 V	20.5 kΩ	3
0.335 V < V_{CNF_IN} < 0.415 V	32.4 kΩ	4
0.460 V < V_{CNF_IN} < 0.540 V	43.2 kΩ	5
0.585 V < V_{CNF_IN} < 0.665 V	56 kΩ	6
0.710 V < V_{CNF_IN} < 0.790 V	68.1 kΩ	7
0.835 V < V_{CNF_IN} < 0.915 V	82.5 kΩ	8
0.960 V < V_{CNF_IN} < 1.040 V	97.6 kΩ	9

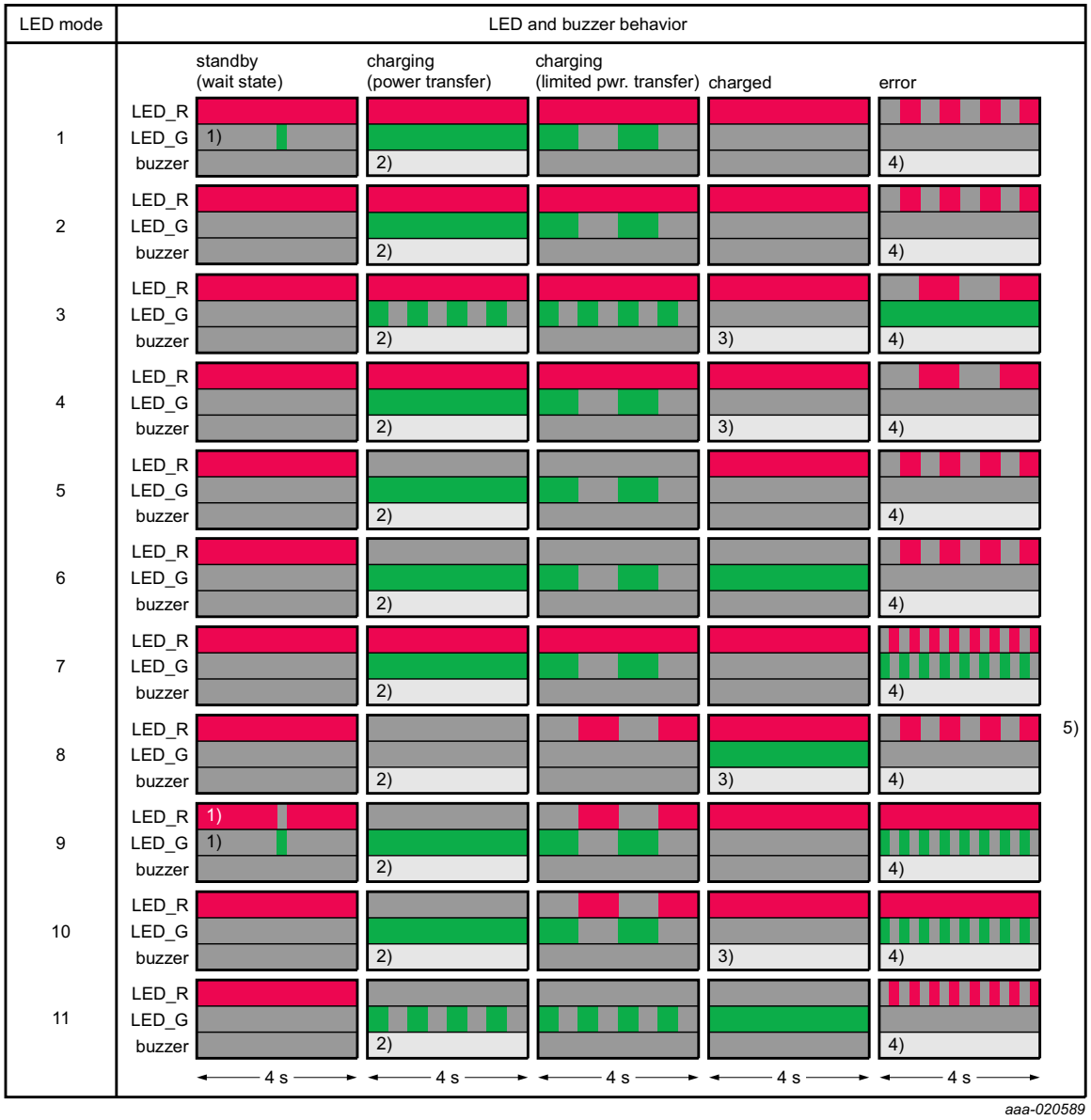
Table 4. LED and buzzer configuration set via the CNF_IN pin (when CNF4 is active)

Input voltage on the CNF_IN pin (when CNF4 is active)	R10[1]	LED/buzzer mode
1.085 V < V_{CNF_IN} < 1.165 V	113 kΩ	10
1.210 V < V_{CNF_IN} < 1.290 V	130 kΩ	11
1.335 V < V_{CNF_IN} < V_{DDP} (V_{DDP} is maximum input level)	-	reserved

[1] Resistor R10 is connected in series with 390 kΩ resistor (R11) to V_{DDP}; see application diagram (Figure 11). Different resistor values can be used provided the ratio between R10 and R11 is maintained; use 1 % tolerance. The resistance values are calculated assuming V_{DDP} = 5 V; to compensate for changes in the supply voltage level, the equation is automatically adjusted.

[2] Instead of a 0 Ω resistor, connect the CNF4 pin directly to CNF_IN.

Figure 6 shows the behavior (logic levels) for modes 1 to mode 11 LED_R, LED_G, and buzzer.



(1) Blink duration is 100 ms (not shown to scale) and is synchronized with digital ping.

(2) When going from standby (wait state) state to charging state, the buzzer beeps twice at 1 kHz

(3) When Charge state is entered, the buzzer beeps 4 times at 2 kHz

(4) One beep (4 kHz) every 4 s.

(5) Mode not recommended.

Fig 6. LED and buzzer modes for normal (non-inverted) green LED and inverted red LED

The LEDs can be connected to the respective LED_R and LED_G outputs in two ways: normal (not inverted) and inverted.

- Normal (not inverted; see Figure 7 (a))
- Inverted (Figure 7 (b))

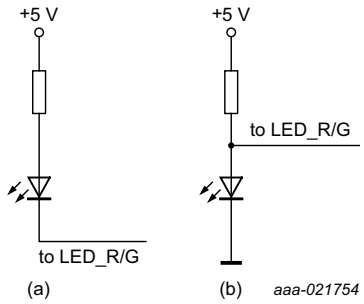


Fig 7. LED connection options; (a) normal, (b) inverted

LED (blinking) patterns for all modes and all LED connection options can be found in the NXQ1TXH5/101 data sheet (Ref. 2).

Remark: Not all modes and configurations lead to Qi certifiable applications.

2.1.4 Thermal protections

2.1.4.1 Built-in thermal protection mechanisms

The NXQ1TXH5/101 has a built-in temperature reduction mechanism that reduces the power transfer when the internal IC temperature exceeds the threshold level of 85 °C. Effectively, this mechanism limits the operating temperature of the device to maximum 85 °C. The output power level reduction allows a very small PCB design with limited cooling. The PCB can operate at full power when the receiver is aligned correctly, but gradually reduces the output power at a high misalignment level. For more information, see the NXQ1TXH5/101 data sheet (Ref. 2).

The built-in temperature reduction mechanism is disabled by connecting the NTC pin to ground. Disabling the temperature reduction mechanism allows designs that operate at device temperatures higher than 85 °C.

When the device temperature exceeds 110 °C, the output power is stopped. When the junction temperature drops to below 80 °C, power transfer is resumed. It is an OverTemperature Protection (OTP) to ensure safe device operation. It is always active, also when the NTC input pin is connected to ground. LED blinking indicates when a protection is triggered.

Additional hardware OTP is triggered when the junction temperature exceeds the temperature protection threshold of between 125 °C and 140 °C. In this case, the output stages are set floating. Because the temperature reduction mechanism reacts at lower temperatures, this additional hardware OTP is only triggered under abnormal load conditions (for example, when the application is heated-up by an external heat source). The hardware OTP acts as an extra safety mechanism.

2.1.4.2 External NTC protection mechanism

The NTC input pin is used to monitor the voltage level on an external NTC resistor network. If the input level on the NTC input pin drops below 0.8 V (V_{trip}), the NXQ1TXH5/101 stops delivering power. When the level exceeds 1.1 V (V_{resume}) again, the NXQ1TXH5/101 resumes operation. The NXQ1TXH5/101 automatically compensates these voltage threshold levels for variations in the 5 V supply (V_{DDP}).

If the voltage on the NTC input pin is below 60 mV (the NTC pin is considered grounded) when charging starts, the temperature sensing function via the NTC is disabled completely. The built-in temperature reduction mechanism (see Section 2.1.4.1) is also switched off.

The NTC input pin can also be connected to the V_{DDP} voltage level. In this case, NTC sensing is inactive, but the built-in temperature reduction mechanism (see Section 2.1.4.1) remains active.

The NTC input pin must always be connected to either V_{DDP}, ground, or an NTC network. A floating NTC pin can cause unpredictable operation.

One or more thermal tripping points can be implemented using the NTC pin of the NXQ1TXH5/101 IC. Figure 11 shows the implementation of a single temperature measurement point. NTC resistor R6 can be placed in the coil center. So the legacy devices with Qi 1.0 receivers can be supported and protected. The combination of resistors R6 and R5 determines at what temperature the thermal protection trips and at what temperature normal operation resumes.

For example, a 100 kΩ pull-up resistor (R5) in series with a 100 kΩ NTC (R6, 1 % thermistor with nominal β-parameter of 4500 K) causes the triggering of the thermal protection at 62 °C. When the temperature has dropped to 52 °C, the application resumes operation. This combination creates a hysteresis of 10 °C.

Capacitor C13 is used to suppress noise. Basically, a low-pass filter is created.

The trip temperature and the resume temperature of an NTC measuring network can be calculated with Equation 8 and Equation 9. The required input:

- The value of the pull-up resistor R5 (in this case 100 kΩ)
- The nominal resistance value (at T_{ref}) of NTC thermistor R6 (in this case 100 kΩ at 25 °C/298.15 K)
- The NTC temperature dependency parameter β: In this case 4500 K for R6.

$$T_{trip} = \frac{1}{\frac{1}{T_{ref}} + \frac{1}{\beta} \cdot \left(ln\left(\frac{V_{trip}}{V_{DDP} - V_{trip}}\right) + ln\left(\frac{R5}{R6}\right)\right)} \quad (8)$$

$$T_{resume} = \frac{1}{\frac{1}{T_{ref}} + \frac{1}{\beta} \cdot \left(ln\left(\frac{V_{resume}}{V_{DDP} - V_{resume}}\right) + ln\left(\frac{R5}{R6}\right)\right)} \quad (9)$$

Where:

- T_{ref} is the reference temperature of the NTC resistor in Kelvin
- ln() is the natural logarithm function
- V_{DDP} = 5.0 V
- V_{trip} = 0.8 V
- V_{resume} = 1.1 V

When R5 = 100 kΩ, R6 = 100 kΩ (at T_{ref} = 298.15 K), and β = 4500 K, the results are:

T_{trip} = 334.95 K (= 61.80 °C, rounded to 62 °C)

T_{resume} = 325.44 K (= 52.29 °C, rounded to 52 °C)

Table 5. Trip and resume temperature examples and associated component values

T_{trip}	T_{resume}	R5	R6
60 °C	50 °C	115 kΩ	100 kΩ; β = 4330 K
65 °C	55 °C	95.3 kΩ	100 kΩ; β = 4330 K
70 °C	60 °C	76.8 kΩ	100 kΩ; β = 4330 K
75 °C	65 °C	90.9 kΩ	150 kΩ; β = 4500 K
80 °C	70 °C	75 kΩ	150 kΩ; β = 4500 K
85 °C	75 °C	62 kΩ	150 kΩ; β = 4500 K

Figure 8 shows a solution to monitor the temperature of more than one location by using two NTC sensors. The lowest voltage is across the NTC resistor with the highest temperature. Two diodes are used to select this lowest voltage. This voltage + the diode forward-bias voltage is then across capacitor C13. The diode forward-bias voltage from diode D3C is subtracted from this voltage so that the voltage on the NTC pin is the voltage across the hottest NTC resistor.

Diodes D3A, D3B, and D3C must be in the same package (e.g. BAW56S), so that they are identical and all have the same temperature.

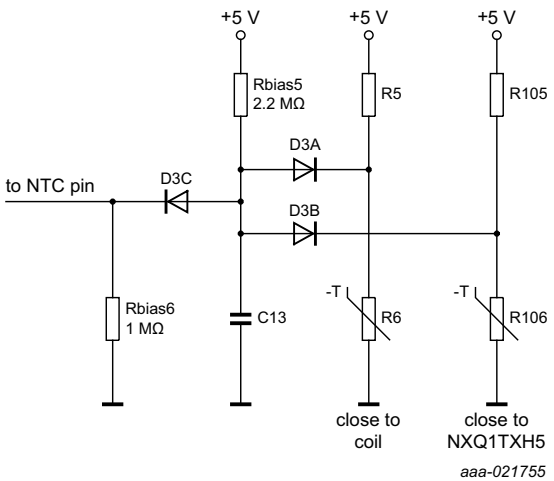


Fig 8. Multiple temperature protections using a diode-circuit

In a similar configuration, more than two temperatures can be monitored and used for tripping/resuming.

2.1.5 STBY - enable/disable operation

For normal operation of the NXQ1TXH5/101 IC, the STBY pin (pin 14) must be low (grounded). To disable operation, the pin must be set high (V_{DDP} level). This functionality can be used in non-standalone Qi wireless power transmitter applications.

2.1.6 Test - factory test

The NXQ1TXH5/101 TEST pin (pin 31) is only used in factory testing. The pin must be grounded in all Qi wireless power transmitter applications.

2.1.7 Support interface

An I^2C interface is provided with the SDA and SCL pins (pin 3 and pin 4). Communication with the NXQ1TXH5/101 processor core can take place through these pins.

To use the SDA and SCL I^2C lines, they must have a pull-up resistor to a 3.3 V (maximum 3.6 V) voltage level.

If I^2C communication is not required, make the I^2C pins available via test pads to allow support.

The detailed use of the I^2C interface is outside the scope of this application note. Contact NXP application support for assistance.

2.2 Input protection

Figure 9 shows a potential implementation of the power interface circuit.

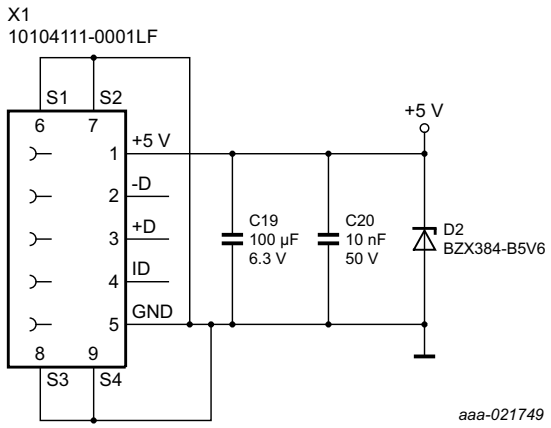


Fig 9. 5 V USB input power interface option

When an additional LED is required to indicate power-on state, use a high-ohmic series resistance to limit the impact on the low-power standby (wait state) properties of the application.

To protect the application against severe overvoltage (e.g. 12 V supplied via the micro USB connector), an alternative USB input power interface can be used (see Figure 10).

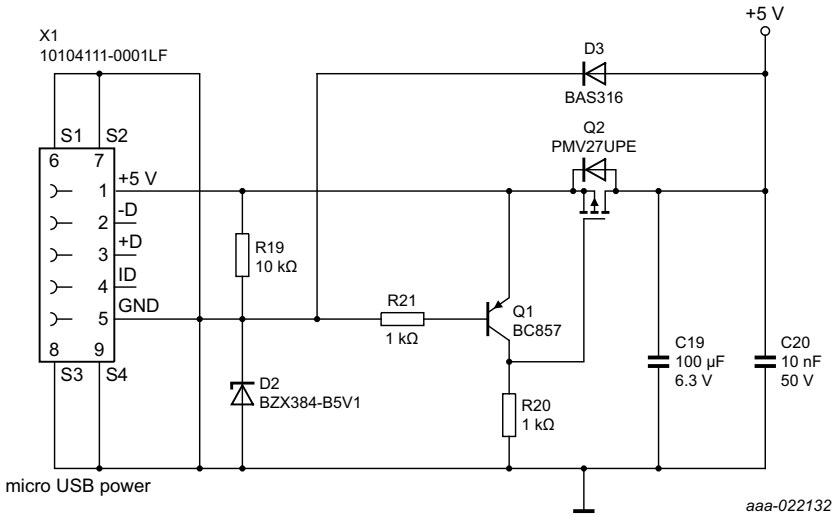


Fig 10. Alternative USB input power interface option

3. Schematic

Figure 11 shows a full basic circuit diagram for a NXQ1TXH5/101 wireless power transmitter application.

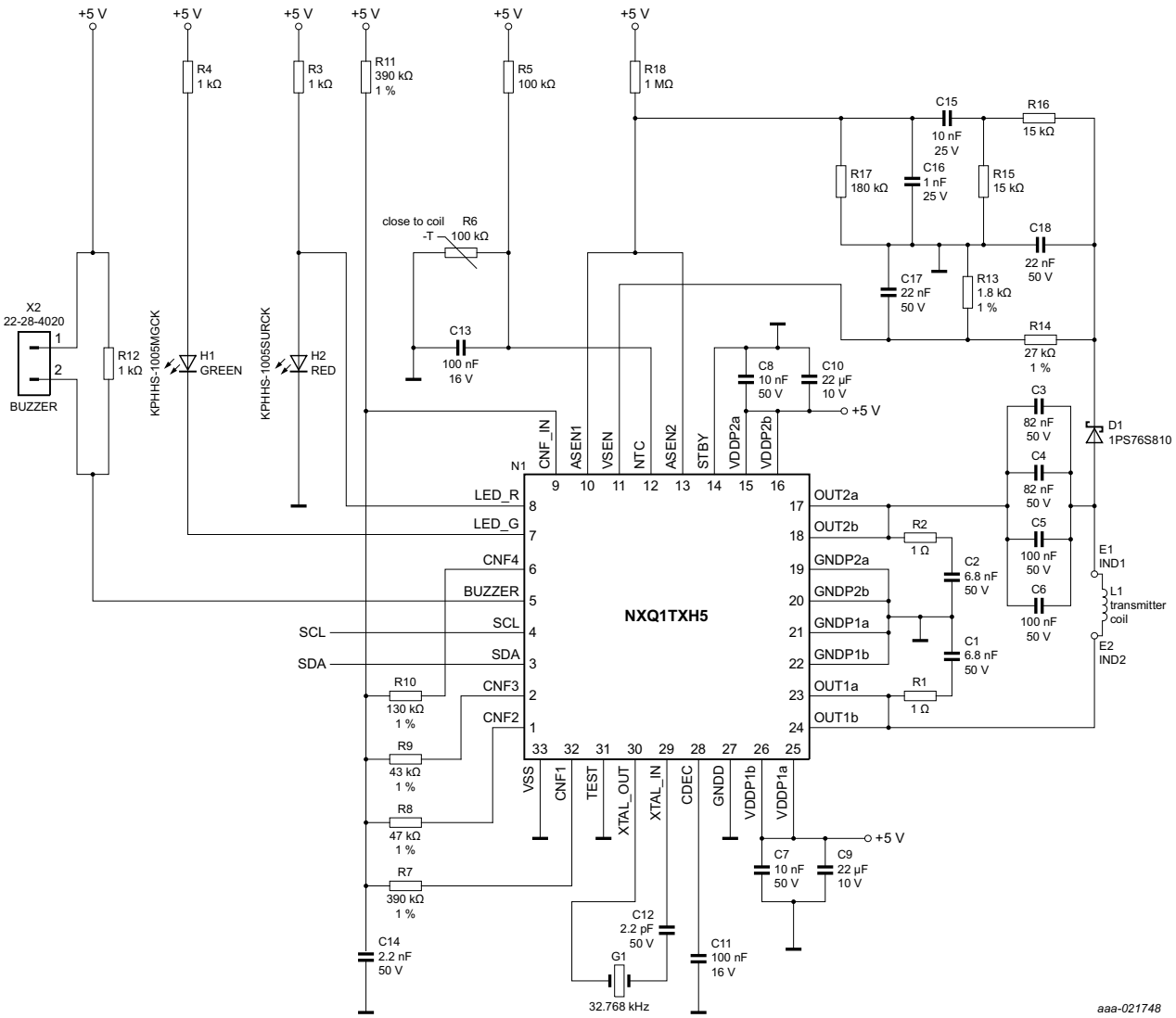


Fig 11. NXQ1TXH5/101 wireless power transmitter circuit diagram

The circuit diagram includes the status LED indicators and a connection for a buzzer. If the LEDs, the buzzer, and the temperature sensor functions are not required, they can be left out. In that case, the respective IC pins can be connected to GND. For Qi certification, at least one LED is required in the application. One or more sensors can be implemented in a specific application. However, it is also possible to omit the sensors and in this way ignore specific temperature information. In this case, only the NXQ1TXH5/101 internal temperature protection is functional.

4. Bill Of Materials (BOM)

Table 6 contains the component list for a basic stand-alone NXQ1TXH5/101 application. The bill of materials more or less corresponds with the NXQ1TXH5/101 reference application as described in the user manual *NXQ1TXH5DB1401 one-chip 5 V Qi wireless transmitter demo board* (Ref. 3).

Table 6. NXQ1TXH5/101 bill of materials

Reference	Description and values	Part number	Manufacturer
C1; C2	capacitor; 6.8 nF; 50 V; X7R	-	-
C3; C4	capacitor; 82 nF; 50 V; NP0	-	-
C5; C6	capacitor; 100 nF; 50 V; NP0 (see Section 2.1.1.1)	-	-
C7; C8	capacitor; 10 nF; 50 V; NP0	-	-
C9; C10	capacitor; 22 μF; 10 V; X5R	-	-
C11; C13	capacitor; 100 nF; 16 V; X7R	-	-
C12	capacitor; 2.2 pF; 50 V; NP0	-	-
C15	capacitor; 10 nF; 25 V; NP0	-	-
C16	capacitor; 1 nF; 25 V; NP0	-	-
C17; C18	capacitor; 22 nF; 50 V; X7R	-	-
D1	diode; Schottky; 30 V; 200 mA	1PS76PS10	NXP Semiconductors
G1	XTAL; 32.768 kHz	S3215-032768-12-20-NA	Yoke
		Q13FC13500004	Epson
		AB26TRQ-32.768kHz-T	Abracon
H1	LED (green)	-	-
H2	LED (red)	-	-
L1[1]	transmission coil; 6.3 μH;	Y31-60055F	E&E
N1	IC	NXQ1TXH5/101	NXP Semiconductors
R1; R2	resistor; 1 Ω; 5 %	-	-
R3; R4; R12	resistor; 1 kΩ; 5 %	-	-
R5	resistor; 100 kΩ; 5 %	-	-
R6	thermistor; 100 kΩ NTC; β = 4500 K	-	-
R7; R11	resistor; 390 kΩ; 1 %	-	-
R8[1]	resistor; 47 kΩ; 1 %	-	-
R9	resistor; 43 kΩ; 1 %	-	-
R10	resistor; 130 kΩ; 1 %	-	-
R13	resistor; 1.8 kΩ; 1 %	-	-
R14	resistor; 27 kΩ; 1 %	-	-
R15; R16	resistor; 15 kΩ; 5 %	-	-
R17	resistor; 180 kΩ; 5 %	-	-
R18	resistor; 1 MΩ; 5 %	-	-
X2	2-pole connector pins	-	-

[1] See Section 4.1.

4.1 Alternatives for coil L1

The choice of L1 depends on the requirements regarding efficiency and cost. Table 7 shows some commonly used transmission coils that can be used to meet these different demands. If a coil is not in this list, it does not mean that it cannot be applied with the NXQ1TXH5/101.

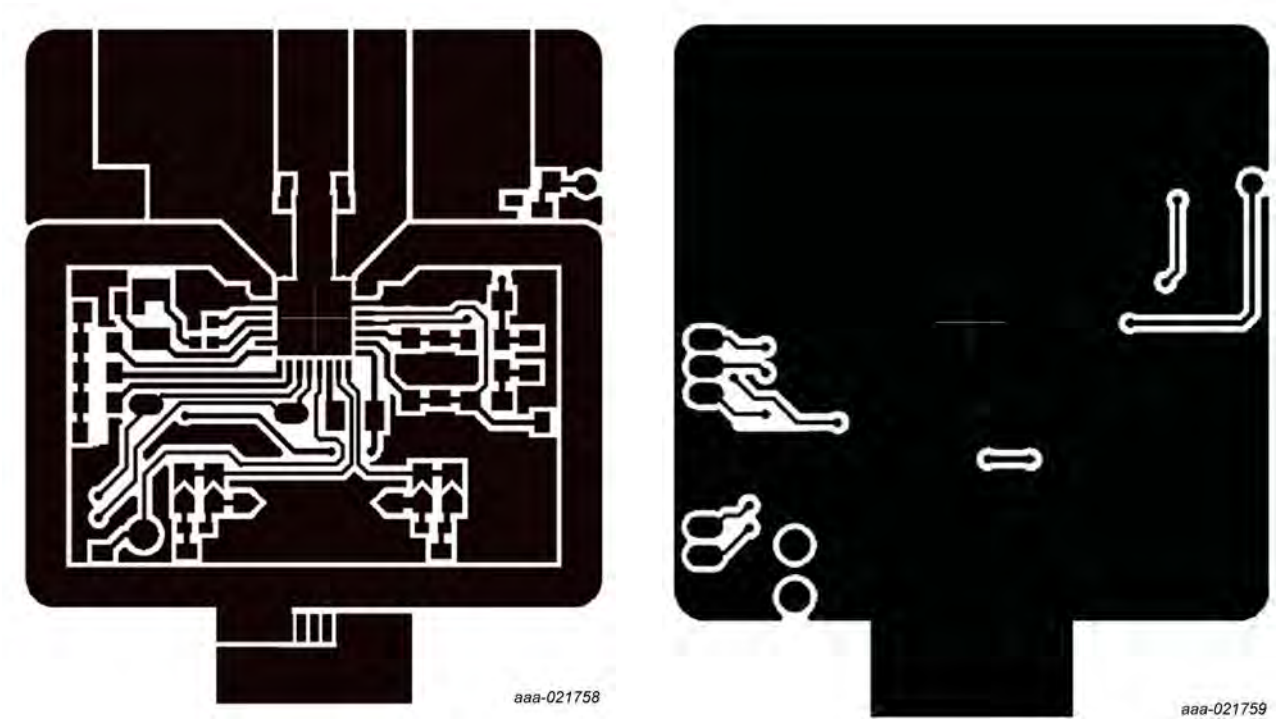
If L1 is changed, the value of R8 must be adapted to get the right value for FOD_E.

Table 7. Typical parameters and R8 recommendations for some commonly used transmission coils

Manufacturer	Type	Number of layers	Inner diameter (mm)	Outer diameter (mm)	Ferrite	ACR at 150 kHz (mΩ)	Typical R8 value (kΩ)
E&E	Y31-60055F	2	21	43	50 mm × 50 mm × 2.6 mm	65	47
	Y31-60081F	1	21	44	50 mm × 50 mm × 0.8 mm	64	47
	Y31-60187F	1	20	43	∅ 50 mm × 3.8 mm	60	47
MEC	31200043	2	20	44	53 mm × 53 mm × 2.5 mm	37	39
	31200057	2	20	44	50 mm × 50 mm × 1 mm	38	39
Shenzhen	SWA20N20H18C01B	2	6.3	17.4	20.4 mm × 20.4 mm × 0.5 mm	135	75
	SWA50N50H30C01B	1	21	44	∅ 50 mm × 1.25 mm	52	43
TDK	WT-505090-10K2-A11-G	1	21	43	∅ 50 mm × 0.9 mm	61	47
Würth Elektronik	760308101103	1	17	28	∅ 30 mm × 0.8 mm	150	82
	760308101104	2	11	20	∅ 20.5 mm × 0.8 mm	125	68
	760308111	2	21	43	54 mm × 54 mm × 2.5 mm	76	51

5. Layout

The layout of an NXQ1TXH5/101 wireless power transmitter application is critical from an electrical and a thermal point of view. Both aspects are covered. A two-sided layout is presented as an example. This layout is also used for the *NXQ1TXH5DB1401 one-chip 5 V Qi wireless transmitter demo board* (Ref. 3).



a. Top copper

b. Bottom copper

Fig 12. NXQ1TXH5/101 demo board layout

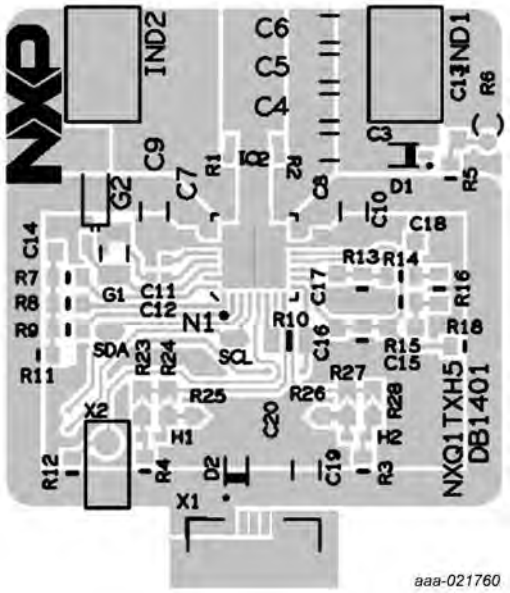
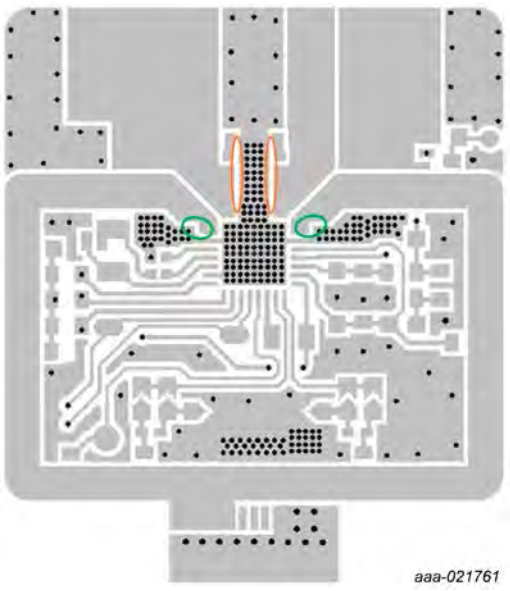


Fig 13. Top side copper with silk screen



Snubber current loops are highlighted in orange. Supply current loops are highlighted in green.

Fig 14. Top side copper with via pattern

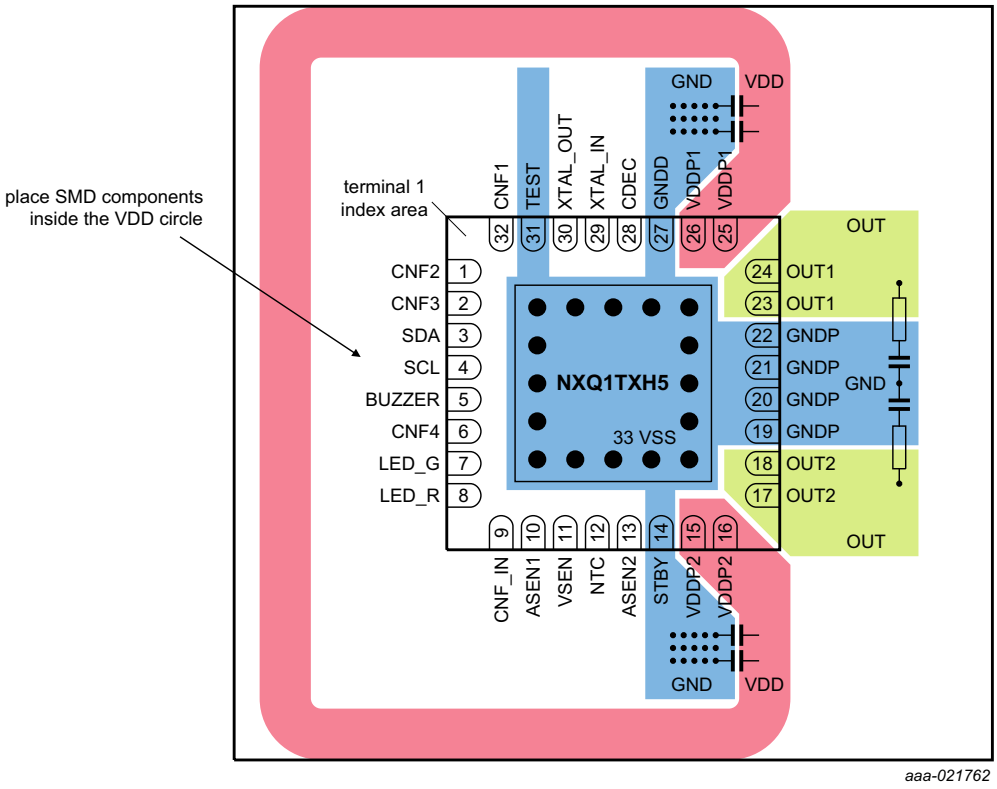
5.1 Electrical layout aspects

From the electrical perspective, the following points require special attention (see Figure 12 to Figure 14):

- To keep the current loops as small as possible, the snubber circuit capacitor C1, resistor R1, capacitor C2, and resistor R2 must be mounted close to the output pins (pins 17 and 18; pins 23 and 24). The GND connection of the snubber circuits must be close to pins 19, 20, 21, and 22. Figure 14 shows the current loops (highlighted orange).
- Decoupling capacitors C10 and C8 must be mounted close to pins 15 and 16. They must have a low-impedance connection to power GND. Capacitor C8 (10 nF) must be closest to pins 15 and 16. Figure 14 shows the current loop (highlighted green).
- Decoupling capacitors C9 and C7 must be mounted close to pins 25 and 26. They must have a low-impedance connection to power GND. Capacitor C7 (10 nF) must be closest to pins 25 and 26. Figure 14 shows the current loop (highlighted green).
- To prevent power loss because of the high current (in the order of 2 A), V_{DDP} power traces to pins 15 and 16 and pins 25 and 26 must be low-impedance/low-loss (wide traces).
- Traces from the output pins 17 and 18 and pins 23 and 24 must be very low-impedance/low-loss (wide traces).
- Decoupling capacitor C11 must be mounted close to pin 28. It must have a low-impedance connection to GND.
- To prevent overtones, traces leading to the G1 crystal in series with the C12 capacitor must be approximately 1 cm long.
- To prevent adverse effects in power transmission coil characteristics, solder the coil terminals directly to the PCB. Do not use extension wires.
- Shielding (non-current conducting) GND planes in the top copper layer must be stitched to the non-current conducting GND areas of the bottom layer GND plane. The stitching must be done with vias on the edges of the planes (see Figure 14).

5.2 Thermal layout aspects

The NXQ1TXH5/101 IC is the main dissipating component on the NXQ1TXH5/101 PCB. All thermal measures taken on an NXQ1TXH5/101 PCB must have one objective: Keep the NXQ1TXH5/101 IC as cool as possible. Figure 15 shows a sketch of the top layer of the board. The bottom layer is (almost) completely filled with copper.



Remark: The IC is placed in the center of the board.

Fig 15. Concept of a power-wise optimal layout for the NXQ1TXH5/101 IC

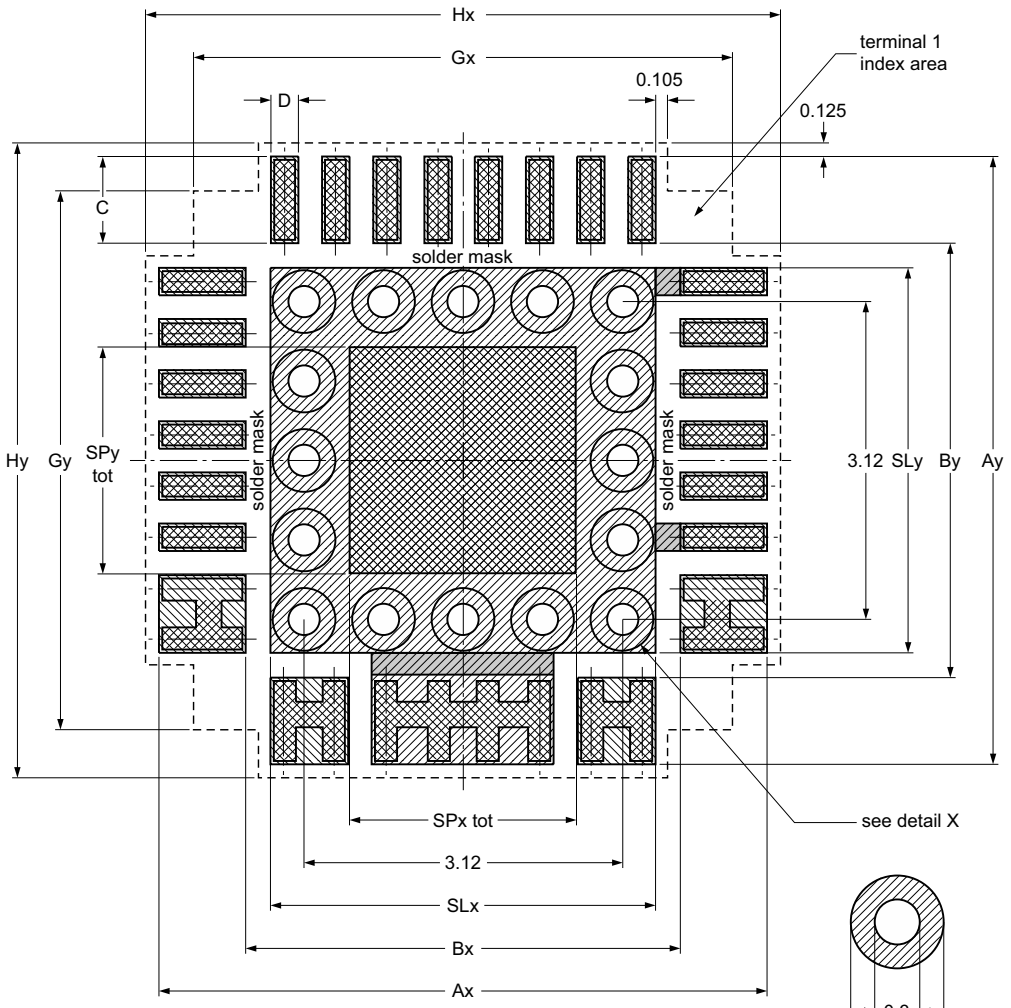
From the thermal perspective, the following points require special attention:

- The exposed die pad of the NXQ1TXH5/101 must be soldered to the top layer of the board.
- Underneath the NXQ1TXH5/101 IC, thermal vias must conduct heat from the top side to the bottom side of the PCB. The thermal connection from top to bottom must contain as much copper as possible. Standard double layer PCB manufacturing techniques offer resin-filled copper-capped vias. To allow as much copper as possible, it is better to use a high number of small resin-filled copper-capped vias than a low number of large ones.
- A shielding GND plane (in this case on the bottom layer) must be maximally uninterrupted.
- If signal traces must run in the main uninterrupted copper GND layer (the bottom layer in our example), ensure that they are as short as possible. Also ensure that they run in the direction of the heat flow. A long perpendicular trace obstructs the heat flow.

- Place the NXQ1TXH5/101 IC more or less in the center of the PCB. In that way, the IC benefits most from its cooling circle.
- Thin PCB material (e.g. 0.8 mm FR4) gives a shorter, and therefore better, thermal path from top to bottom than thick PCB material (e.g. 1.6 mm FR4).
- A thick copper layer (70 μm) conducts twice as good as a thin (35 μm) copper layer. A thick copper layer also enhances the thermal characteristics significantly. Use a 70 μm copper layer.
- Attach as much copper as possible to the grounded pins of the IC. Good thermal conduction from pins 33, 19, 20, 21, and 22 is important.
- Attach sufficient copper to the output pins 17, 18, 23, and 24. It is not only good for electrical conduction, but also results in thermal conduction benefits.
- Attach sufficient copper to the supply pins 15,16, 25 and 26. Figure 15 gives an idea of a power-wise optimal layout.
- Use high-thermal conductivity ceramic paste as the filling material for vias enhances thermal conductivity further. Unfortunately, the use of this kind of material is usually not a part of a standard PCB production flow.
- Do not use open vias underneath the NXQ1TXH5/101 IC. There is a risk that, most of the solder paste that must connect pin 33 (the exposed lead frame pad) to the PCB is sucked into these vias during the assembly process. It can result in a poor quality a negative influence on the quality of the thermal (and electrical) connection from pin 33 to the PCB.
- Figure 16 shows the recommended footprint (for reflow soldering) for the NXQ1TXH5/101 IC. The recommendation includes 16 thermal vias. However, the use of more vias, optionally in a different configuration, which increases the amount of copper between the top and the bottom layer underneath the IC is always encouraged.
- More thermal vias from the top GND layer to the bottom GND layer that surround the IC can improve the thermal connection from top to bottom.
- Thermal vias in remote areas (that is: relatively far from the dissipating element) do not really contribute to the thermal performance. The thermal gradient from top to bottom layer is already minimal in remote areas. So, connecting them with a low thermal impedance path does not bring much improvement. All remote vias shown in Figure 14 have an electrical (non-thermal) purpose.
- The bottom layer (or other inner layer if there is a multiple-layer PCB) must be a (nearly) uninterrupted copper layer. This layer spreads the heat over the PCB and, if the layer is the bottom layer, radiates the heat to the ambient.
- The outer layers (top and bottom layers) of the PCB must be covered with a high-emissivity coating. In most circumstances, normal solder resist is good enough because it has an emissivity of 0.9 to 0.95. Do not leave the copper blank or coat it with a reflective (e.g. gold) finish.

- A larger PCB larger enhances thermal performance of the application significantly. A PCB that is too small causes thermal issues for the application. To move heat out of the NXQ1TXH5/101 component and the PCB, thermal radiation is essential. To lose heat through radiation, the board surface area is more or less proportional to the capability of the board.Figure 17 shows a graph that gives an impression of how $R_{th(j-a)}$ (thermal resistance from the NXQ1TXH5/101 IC silicon to the ambient) varies with PCB area. Trend lines are shown for 2-layer/70 μm copper, 4-layer/35 μm copper, and 4-layer/70 μm copper.

Footprint information for reflow soldering of HVQFN32 package **NXQ1TXA5**



Recommended stencil thickness: 0.1 mm

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	nSPx	nSPy	Gx	Gy	Hx	Hy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	3.75	3.75	2.2	2.2	-	-	-	-	5.25	5.25	6.2	6.2

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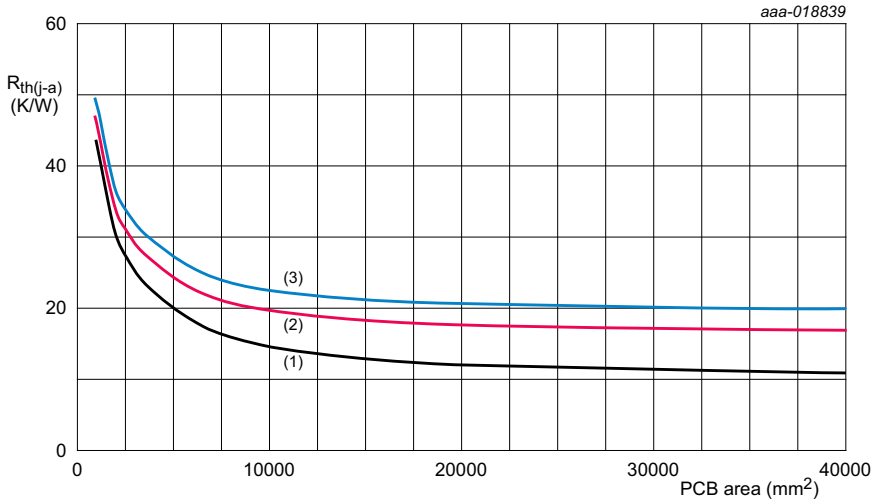
Fig 16. Application-specific reflow soldering footprint



(1) 4-layer: 70 µm

(2) 4-layer: 35 µm

(3) 2-layer: 70 µm

Fig 17. Typical trend lines for the $R_{th(j-a)}$ versus PCB area

The NXQ1TXH5/101 demo board used as illustration in this application note has a PCB area of approximately 900 mm^2. This PCB area gives the NXQ1TXH5/101 demo board an R_{th} value of approximately 45 K/W. Figure 17 shows that a smaller board can rapidly cause thermal issues for the assembly. It also shows that increasing the PCB area beyond a certain point (for this application say beyond 10,000 mm^2) only ensures minimal thermal improvement.

Figure 18 and Figure 19 show the preferred 2-layer and 4-layer PCB constructions.

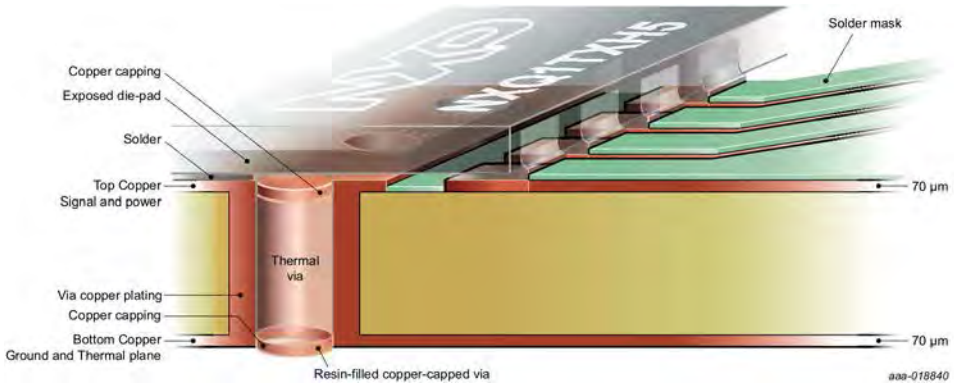


Fig 18. Preferred 2-layer PCB construction

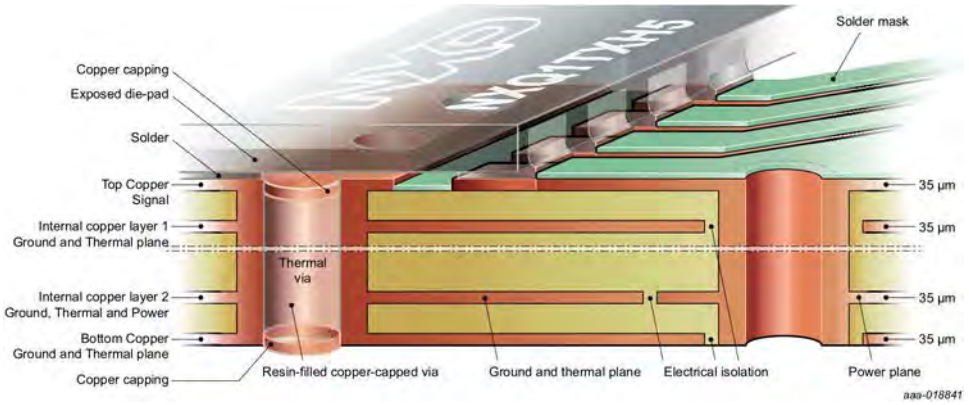


Fig 19. Preferred 4-layer PCB construction

6. Qi compliance testing

This section contains several guidelines for products that are targeted to be Qi certified.

6.1 Receiver rectified voltage during identification and configuration

During standby (wait state), the NXQ1TXH5/101 consumes very little power, which causes many USB power adapters to enter a low-power mode.

When the NXQ1TXH5/101 detects a receiver, it starts a power transfer. The power transfer causes the USB power adapter to wake up from low-power mode. As the output voltage of USB adapter can vary during wake-up, the input voltage to the NXQ1TXH5/101 application varies. The variation can cause issues with the Qi compliance test #8(a): The receiver rectified voltage change during identification and configuration phase may not exceed the limit of 200 mV. A USB cable with AWG20 wiring minimizes voltage variation at the input of the power stage.

6.2 Guaranteed power transfer test

To pass Qi compliancy test #23(b) (Guaranteed power transfer test with test power receiver #1 configuration b), sufficient voltage is required at the input circuit of the NXQ1TXH5/101. An AWG20 cable minimizes the voltage drop over the USB cable. It enables the transmitter to deliver the requested power to the receiver.

Use a USB adapter with cable compensation for Qi compliance testing.

7. Appendix: NXQ1TXL5/101

Fig 20. NXQ1TXL5/101 IC

The NXQ1TXL5/101 is a simplified version of the NXQ1TXH5/101 IC that allows a lower cost, reduced component count solution. The NXQ1TXL5/101 IC does not have the configuration options that the NXQ1TXH5/101 IC has. Preset configuration is similar to the default settings in NXQ1TXH5/101 and the LED/buzzer mode is mode 11. For more information, see the *NXQ1TXL5/101 data sheet* (Ref. 5).

Remark: It is not possible to realize a Qi certifiable application with the NXQ1TXL5/101 IC, because the device has reduced functionality. It does not differentiate between normal charging and limited power charging, it does not support FOD, and it has a fixed LED mode.

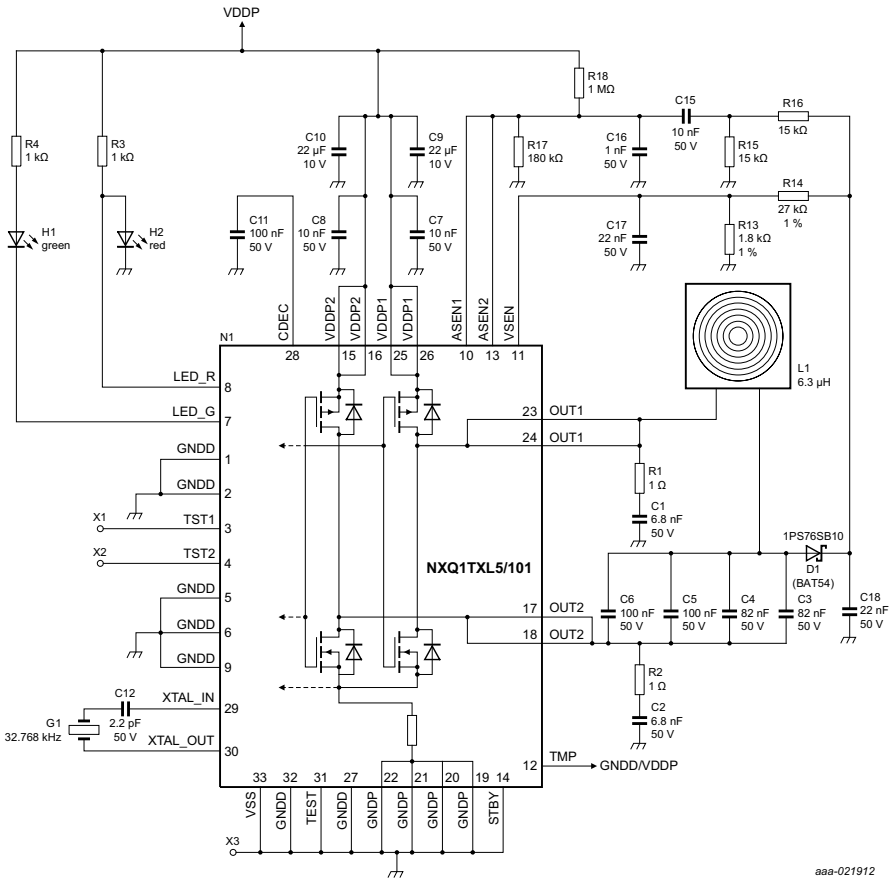


Fig 21. NXQ1TXL5/101 wireless power transmitter circuit diagram

7.1 BOM differences between NXQ1TXH5/101 and NXQ1TXL5/101

Table 8 gives an overview of the BOM differences.

Table 8. BOM differences between NXQ1TXH5/101 and NXQ1TXL5/101

Component	Value/comment
C13	open; TMP pin must either be connected to V_{DDP} or GNDD
C14	0 Ω; connect pin 9 to GNDD
R5	open (∞ Ω) or closed (0 Ω); TMP pin must either be connected to V_{DDP} or GNDD
R6	closed (0 Ω) or open (∞ Ω); TMP pin must either be connected to V_{DDP} or GNDD
R7	0 Ω; connect pin 32 to GNDD
R8	0 Ω; connect pin 1 to GNDD
R9	0 Ω; connect pin 2 to GNDD
R10	0 Ω; connect pin 6 to GNDD
R11	∞ Ω (open)
R12	∞ Ω (open); pin 5 must be connected to GNDD, but may be left floating[1]
X2	No buzzer connector mounted

[1] Not recommended for thermal reasons.

If an LED pin (LED_G, LED_R) is not used because the corresponding LED is not included in the application, the LED pin can be connected to GNDD. Connecting the unused LED pin to GNDD enhances the thermal performance of the application.

To allow application support, make the TST1 and TST2 pins available via test pads. When these pins are connected to GNDD, no application support is possible.

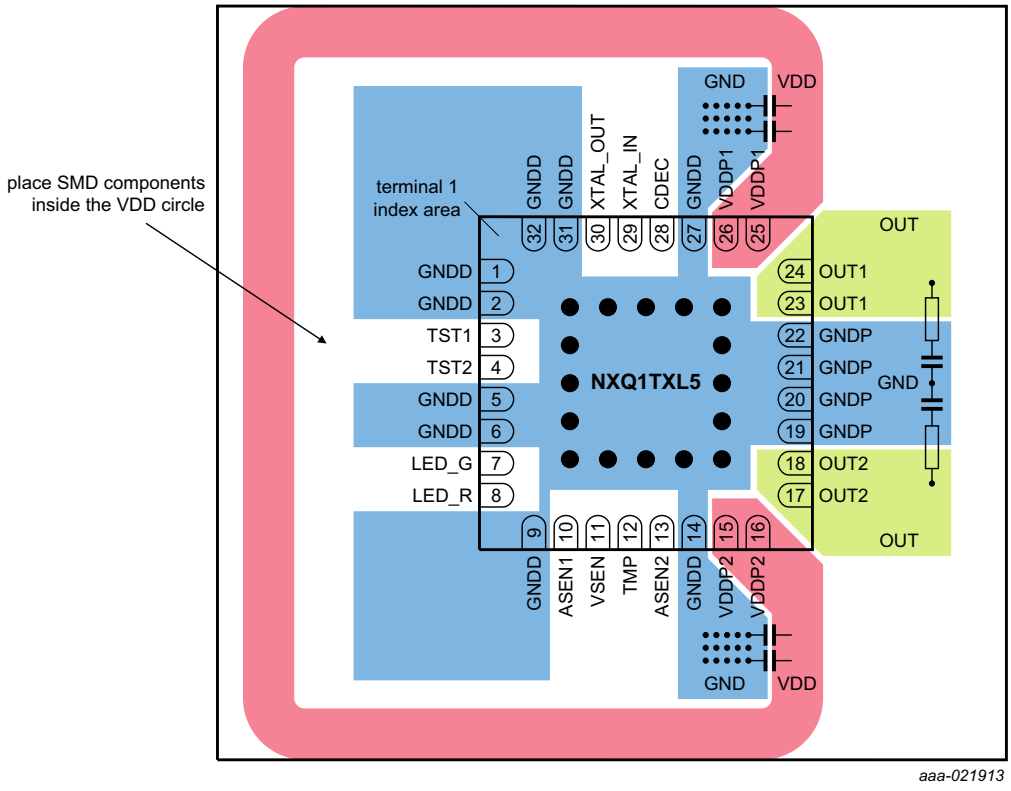
7.2 Layout

The set of layout rules and recommendations for the NXQ1TXH5/101 also apply for the NXQ1TXL5/101 application (see Section 5).

7.3 Thermal layout aspects

Many of the IC pins that are used for advanced settings and features in the NXQ1TXH5/101 are GNDD pins in the NXQ1TXL5/101. In this way, more pins of the IC are connected to the ground plane, which enhances the thermal performance of the application.

Figure 22 shows a typical layout of the top layer. The bottom layer is (almost) completely filled with copper. Please compare Figure 22 to Figure 15.



Remark: The IC is placed in the center of the board.

Fig 22. Typical NXQ1TXL5/101 power and GND layout pattern

8. Abbreviations

Table 9. Abbreviations

Acronym	Description
ASK	Amplitude Shift Keying
EMI	ElectroMagnetic Interference
FOD	Foreign Object Detection
LED	Light-Emitting Diode
NTC	Negative Temperature Coefficient
OTP	OverTemperature Protection
PCB	Printed-Circuit Board
PID	Proportional-Integral Derivative
RMS	Root Mean Square
SPL	Smart Power Limiting
SPR	Static Power Reduction
USB	Universal Serial Bus
WPC	Wireless Power Consortium

9. References

[1] **Qi System Description Wireless Power Transfer —** Volume I: Low Power, Part 1: Interface Definition, Version 1.2, June 2015

[2] **NXQ1TXH5/101 data sheet —** One-chip 5 V Qi wireless transmitter; 2016, NXP Semiconductors

[3] **UM10943 user manual —** 7NXQ1TXH5DB1401 one-chip 5 V Qi wireless transmitter demo board; 2016, NXP Semiconductors

[4] **NXQ1TXH5/101 FOD configuration —** Available from NXP Semiconductors; Please contact your NXP Semiconductors sales representative

[5] **NXQ1TXL5/101 data sheet —** Low-cost one-chip 5 V Qi compliant transmitter; 2016, NXP Semiconductors

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