AN11038

Fast Verification of PN512 and amplifier

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Application note
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Document information

Info	Content
Keywords	PN512, Amplifier, Functional Verification
Abstract	This application note explains important registers for reader mode only. A guided verification of signaling and register adjustments is given.

Revision history

Rev	Date	Description
1.2	20121003	Section License updated
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1.0	20110301	First release

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1. How to use this document

This document is intended to give a practical guideline on functional verification of a reader system based on PN512 and amplifier based on [1]. The first two chapters cover explanations on verification of the transmitter and receiver circuitry, including subchapters of troubleshooting and FAQ.

Another chapter includes the description of mandatory registers for the reader application.

The last chapter concludes with a Troubleshooting Guide, which shall guide the user in finding the root cause by a step by step procedure.

2. TX Verification

2.1 13.56MHz Basic RF Field check

This is the very first basic check. Switch ON the RF field to measure the RF field (13,56MHz).

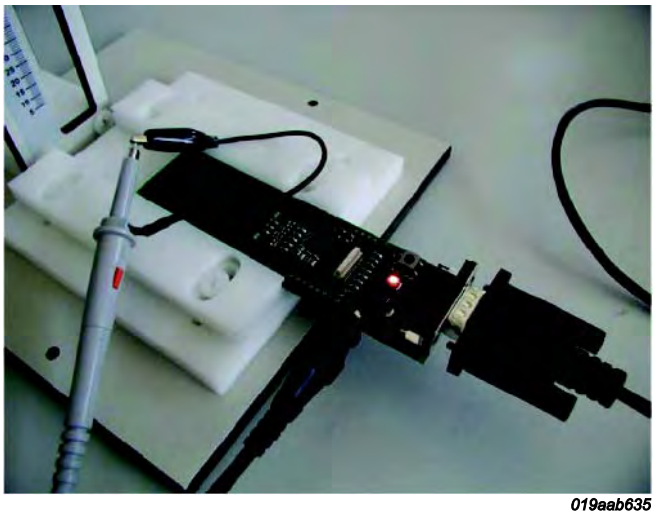


Fig 1. Basic check with field probe

This shows how to establish the test setup with a field probe. It is the standard probe with 12pF capacitance. In case you use an ESD-mat or a desk which influences the magnetic field (iron inside or under the surface) please use some spacer for your measurements e.g. some card box of height 10cm. This should de-couple the desk's magnetic influence.

Start a REQA command – the RF-Field is switched on and still running after finishing the command. The RF-Field is seen on the oscilloscope:

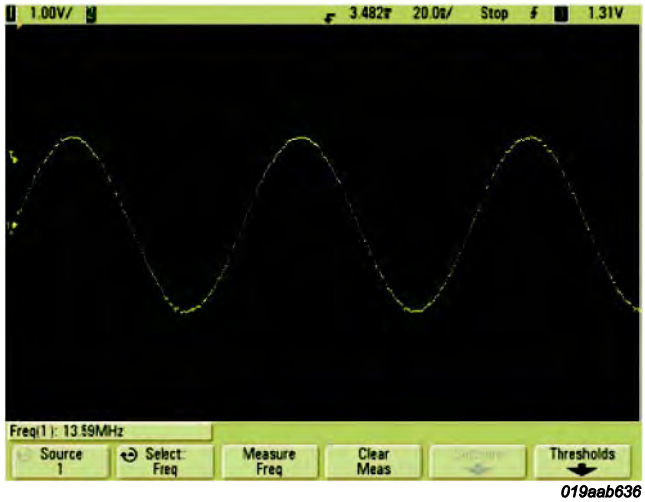


Fig 2. 13.56MHz carrier measured with an oscilloscope

Please take into account that the absolute amplitude may change due to the coupling factor achieved by the field probe. Of only interest is the existence of the 13,56MHz field.

2.2 13.56 MHz RF-field – ASK check

Second step is to verify the correct pulse shaping of the Reader/ Writer Device. The 100% ASK of the SENSE_REQ or REQA is used for this measurement. By adjusting the trigger to Pulse-Width this can easily be observed.

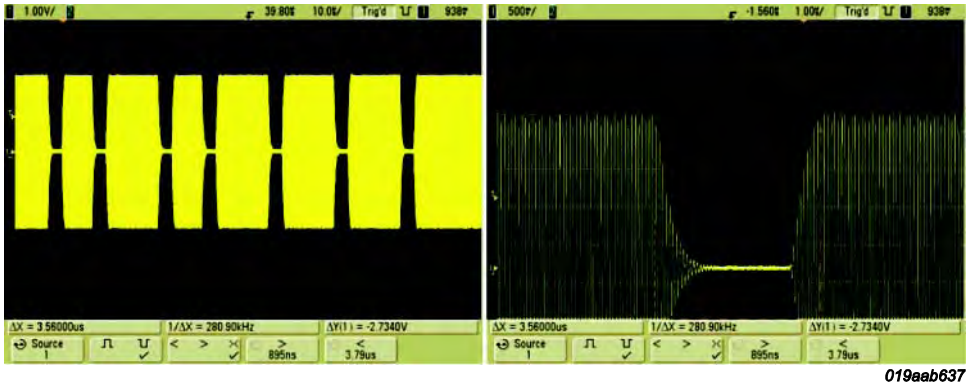


Fig 3. ASK Verification

The signals from Fig 3 were taken with an oscilloscope loop and give a first feeling of the shaping.

For comparison with ISO18092-envelope shaping you need to measure with the Reference PICC specified in the corresponding ISO standard.

This is the Pulse-Shaping given in the ISO18092 page 8. Of special interest are the given values of Rise/ Fall Time and Over/Undershoots. If the times are not OK, the Q-factor of the antenna might be to High / Low as it controls mainly the rise time and the resulting overshoot.

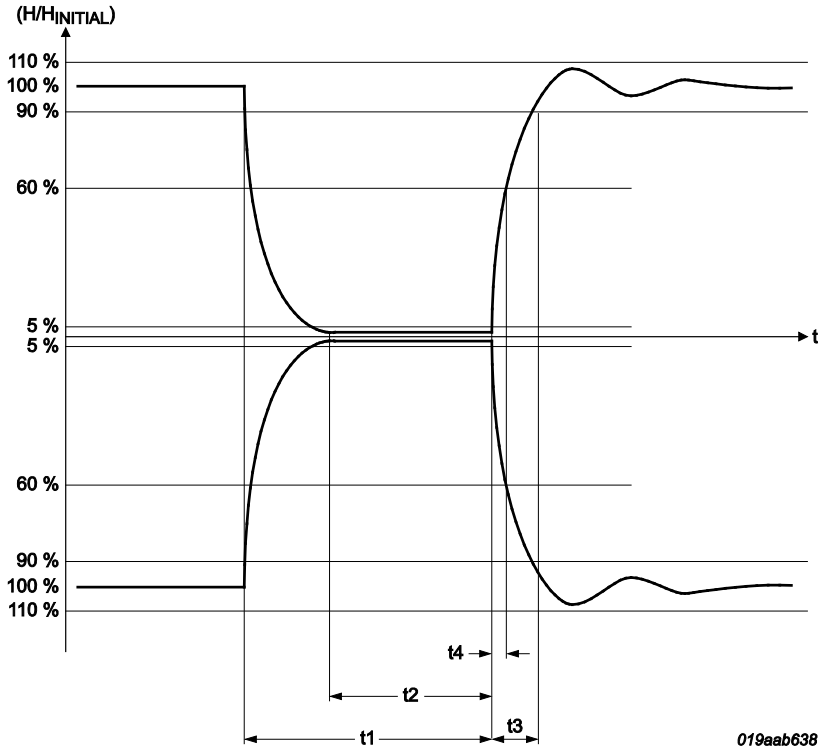


Fig 4. ISO18092 Envelope Check

If the shaping is OK we move on to the next step and have a look on the antenna tuning.

2.3 TX and collector measurement point

Within this measurement the tuning of the antenna and the switching behaviors of the transistors can be interpreted. In principle the measurement can be done on TX1 or TX2 and on the collector of the transistors.

The testpoints for the measurement can be depicted from Fig 5 marked with TP1, TP2, TP3 and TP4. For measurements close to the antenna try to avoid magnetic coupling influences into the oscilloscope's probe loop by good ground connection which is close to the test-points (TP1, TP2, TP3 or TP4).

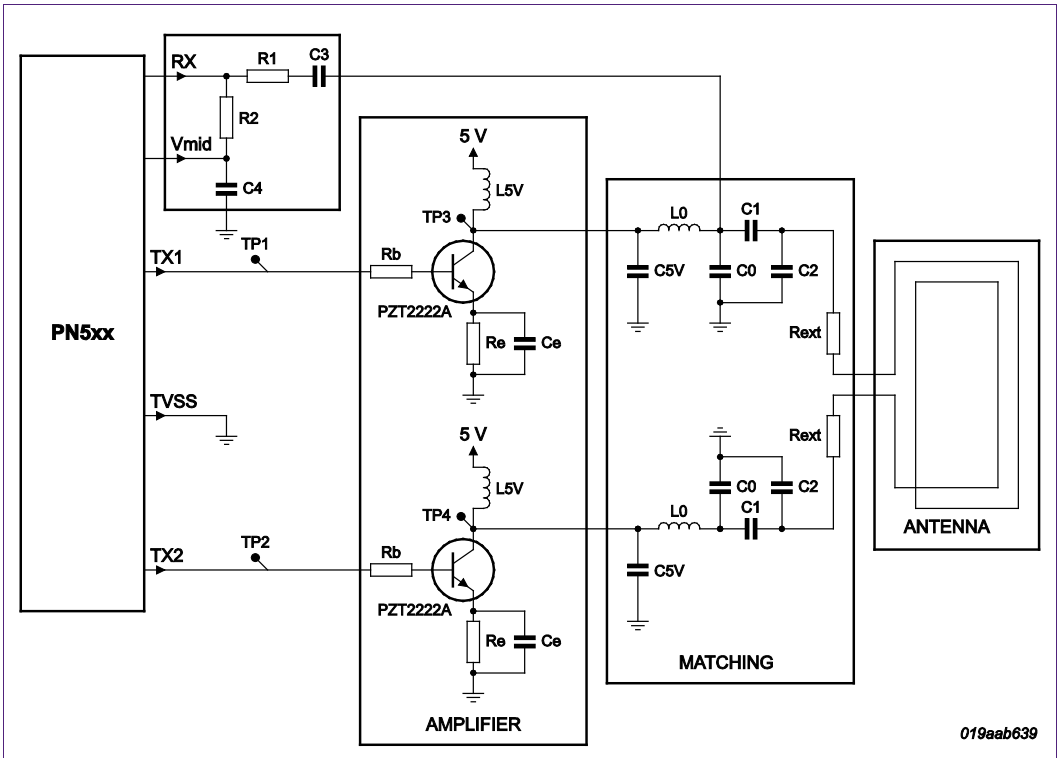


Fig 5. TX Measurement Setup

This measurement is taken with a standard probe. Only the 13.56 MHz carrier needs to be switched on to evaluate the signals.

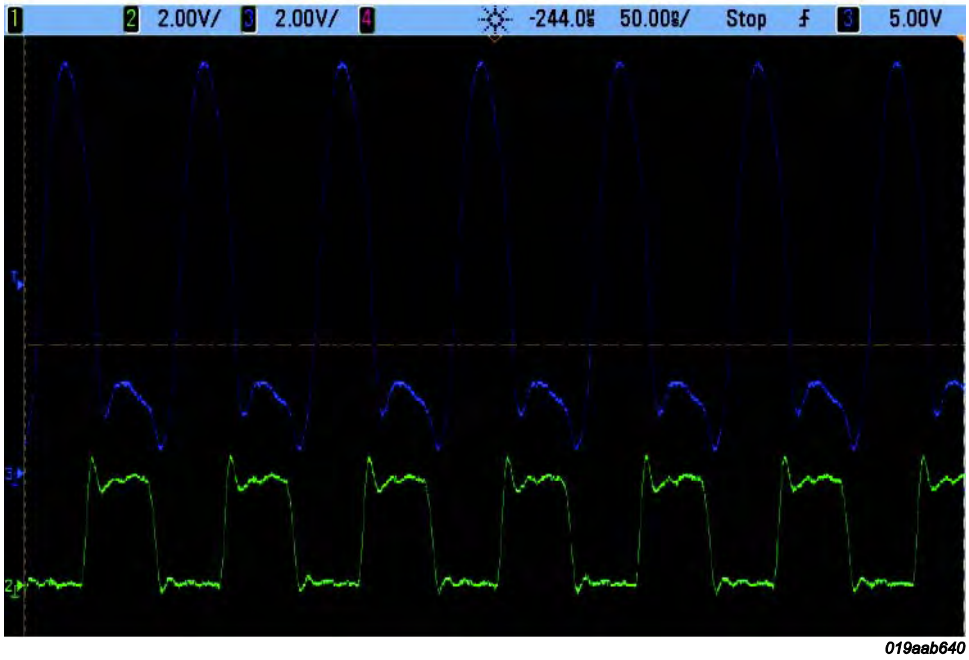


Fig 6. Transistor collector and TX verification with standard probe and tuned antenna

From this picture we take the information that the switching of the transistors is done in an optimum way. The blue signal in Fig 6 shows the signal on the collector, the green one is measured directly at the driver TX of the PN512.

Only the signals on the collectors are relevant for evaluating the matching. The driver signals (TX1 and TX2) are not highly affected by a mismatch. They are shown just for completeness to check if the drivers of PN512 are working and deliver the 13.56 MHz signal.

2.4 Measurement with a Non-Perfect Antenna

The same measurement at the collector of the transistor and the driver of PN512 has been done using a mis-matched antenna.

From Fig 7 is can be seen that the signal at the collector (blue signal) is not switched through in an optimum way. The impact on the system might be of low output power, overshoots, undershoots, EMI due to improperly matched antenna.

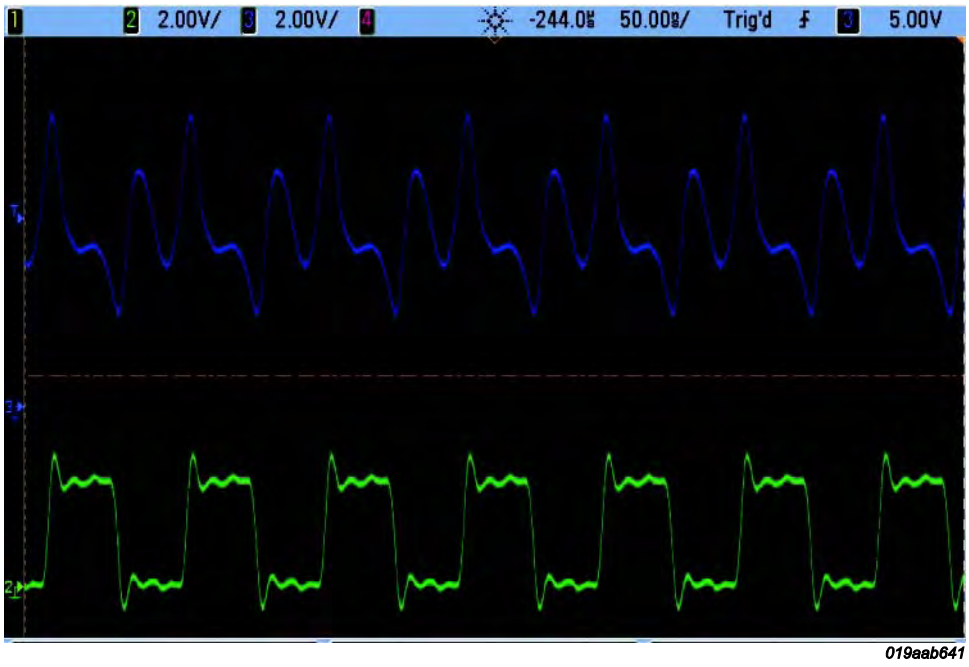


Fig 7. Transistor collector and TX verification with standard probe and mismatched antenna

Hence, the antenna has to be matched accordingly.

3. RX Verification with a Tag

We go on with our investigations in case the TX1 behavior is within the limits. We need to add a tag to the setup – in this case a MIFARE 1k card. The setup looks like this:

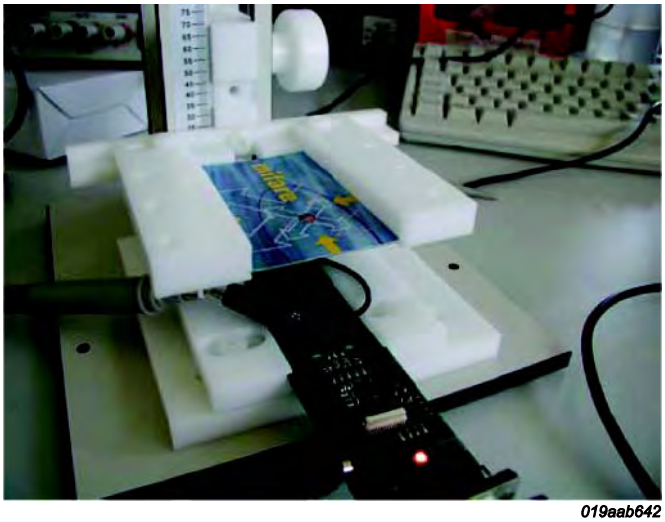


Fig 8. Verification on Tag Response

With the previously done measurement we shall be able to power up the card and send a SENSE_REQ or REQA. What we would like to see is the card's response. If this can be observed we know two things:

1. We are able to power up the Tag

2. We are able to send a command which is demodulated and understood by the card correctly

We try to find the 848kbps modulated carrier response of the tag:

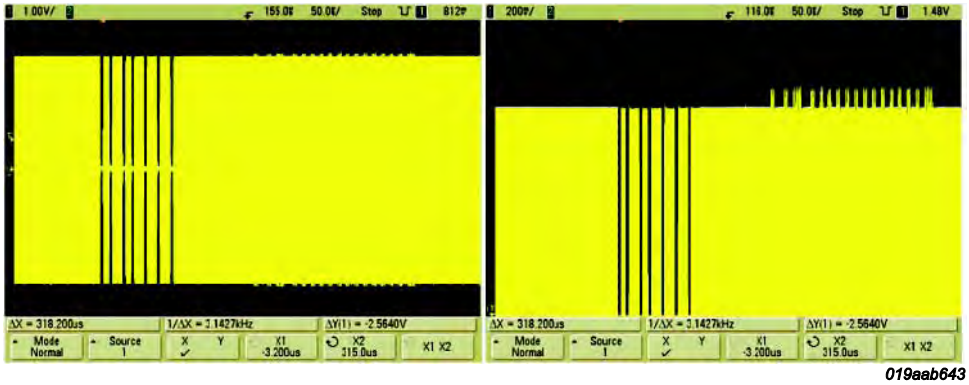


Fig 9. Tag Response Part1

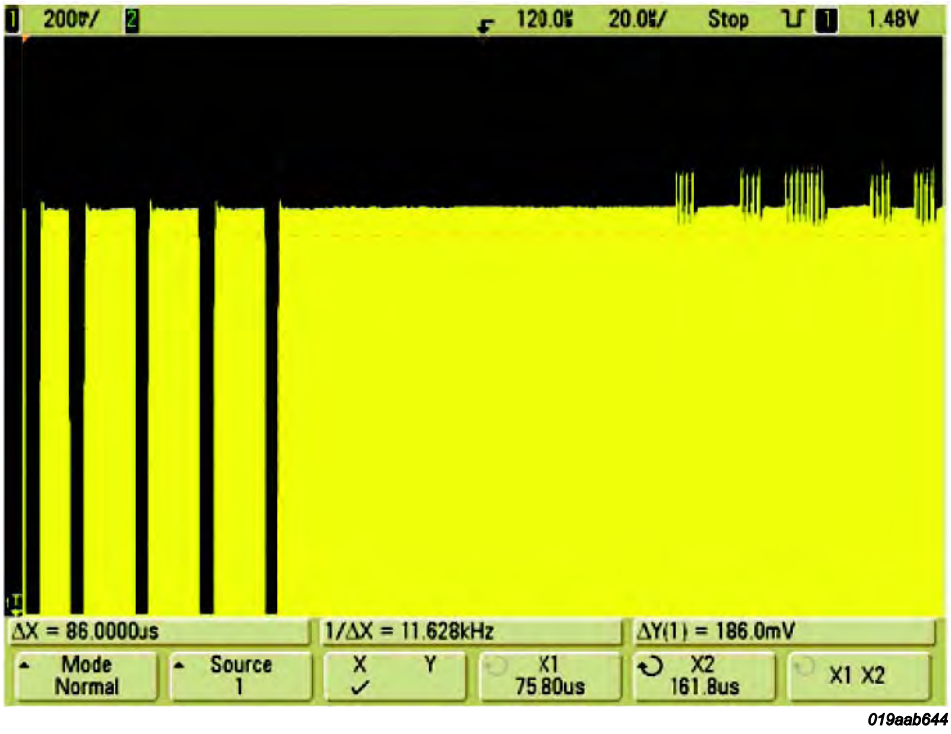


Fig 10. Tag Response Part2

The pictures show all the same Request / Response only the zoom factor is different. We can conclude that the card is powered correctly, the Request command could be decoded correctly – thus we see some response from the target.

To see the response nicely a good coupling factor is needed. For this measurement the distance between Reader / Writer and MIFARE card was about 1cm.

As a last step the RX signal needs to be verified by measuring directly at the RX pin with a low capacitance probe (typ. < 2pf), which has an impedance termination of 50 Ohm.

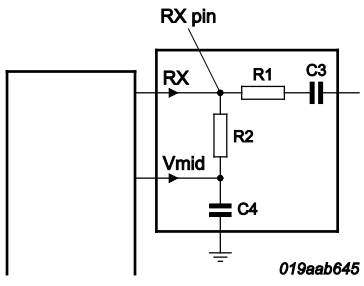


Fig 11. Setup RX path verification

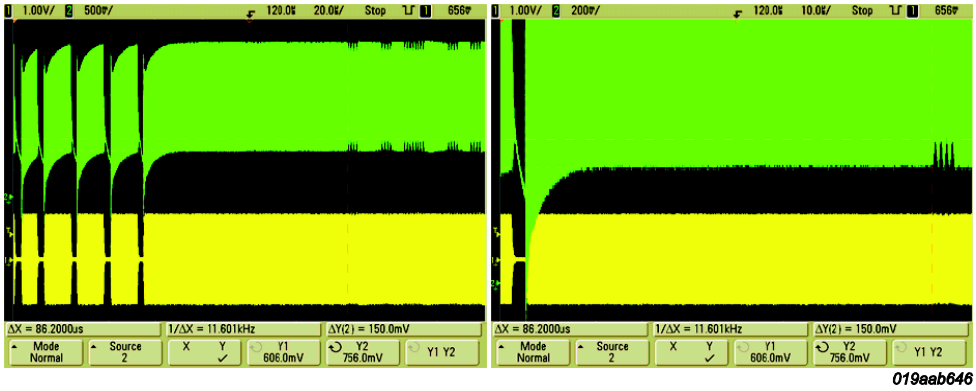


Fig 12. RX signal green colored, RF signal yellow

3.1.1 Troubleshooting and FAQ

Q: The PN512 has problems receiving the card response

A: Check the RX voltage levels with low cap probe. If the signal is too high and clipping at RX, the PN512 can not demodulate the answer. Ensure that the RX signals are within the limits also in the detuned case, when different cards are loading the reader antenna.

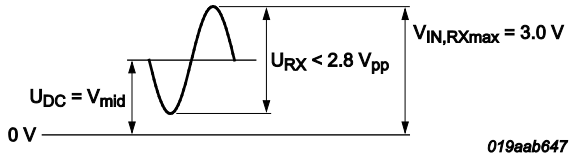


Fig 13. Signal limits at RX

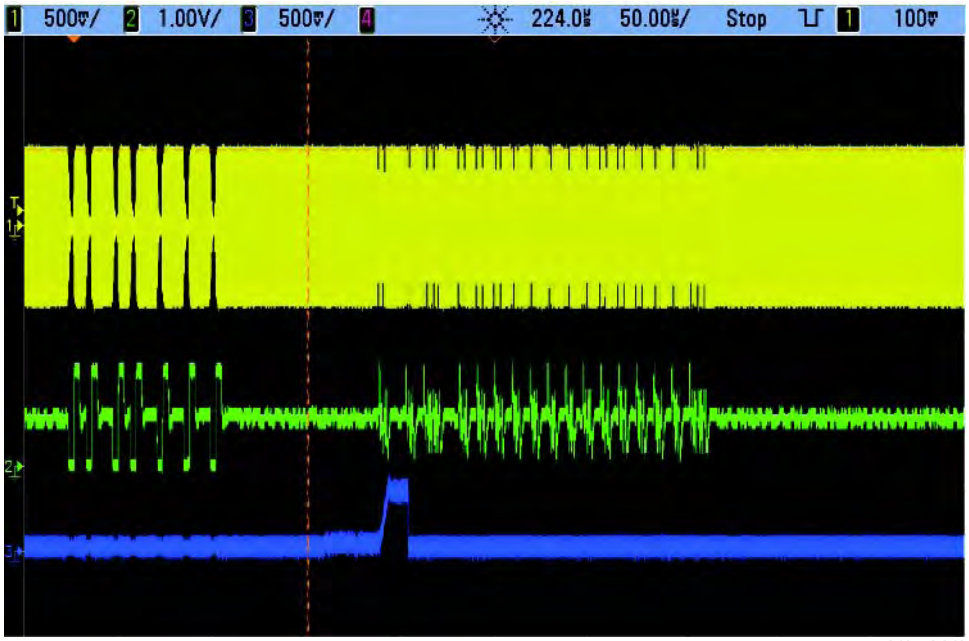
Q: The card is modulating back to the reader, but PN512 doesn't recognize answer

A: This can have different reasons:

- Signals at RX are out of specifications.
- RXGain not correctly set
- MinLevel not correctly set

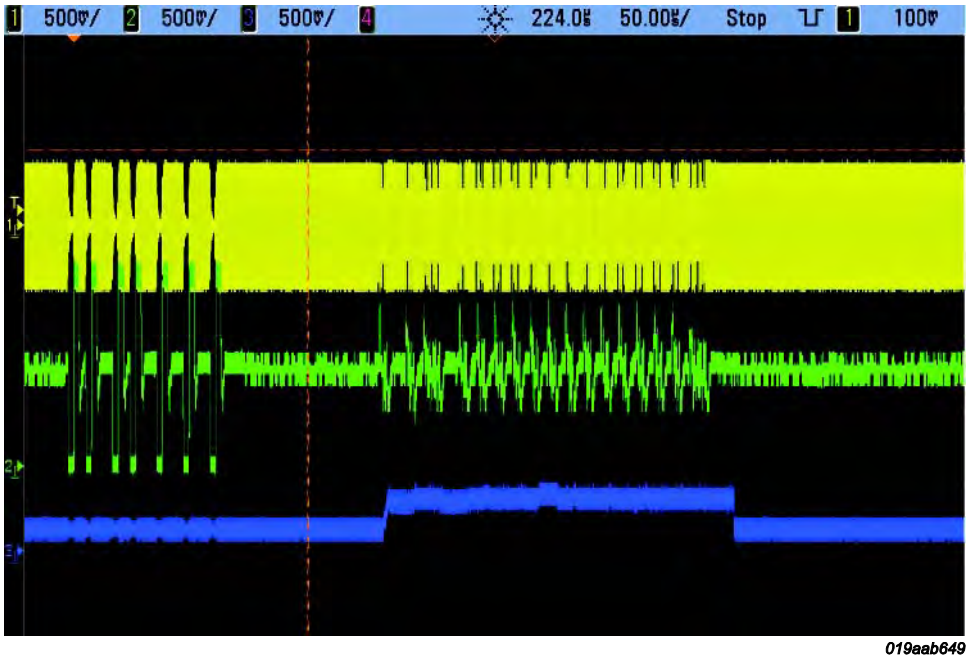
The following Fig 14 shows the MinLevel signal at a setting where it is too low, hence the answer of the card is not received correctly in the FIFO.

In Fig 16, the MinLevel was set to a higher level, such that the circuitry can decide between data bits and noise.



(1) Yellow signal is the RF signal, green depicts the ADC_I channel, blue is the MinLevel output

Fig 14. Representation of the MinLevel at AUX pin



(1) Yellow signal is the RF signal, green depicts the ADC_I channel, blue is the MinLevel output

Fig 15. MinLevel stays active during reception

3.2 Receiver Block Diagram

Fig 16 shows the block diagram of the receiver circuitry. The receiving process includes several steps. First the I/Q demodulation of the carrier signal of 13.56 MHz is done. The demodulated signal is amplified by an adjustable amplifier. A correlation circuit calculates the degree of similarity between the expected and the received signal. In the evaluation and digitizer circuitry the valid bits are detected and the digital results are sent to the FIFO register. Several tuning steps in this circuit are possible.

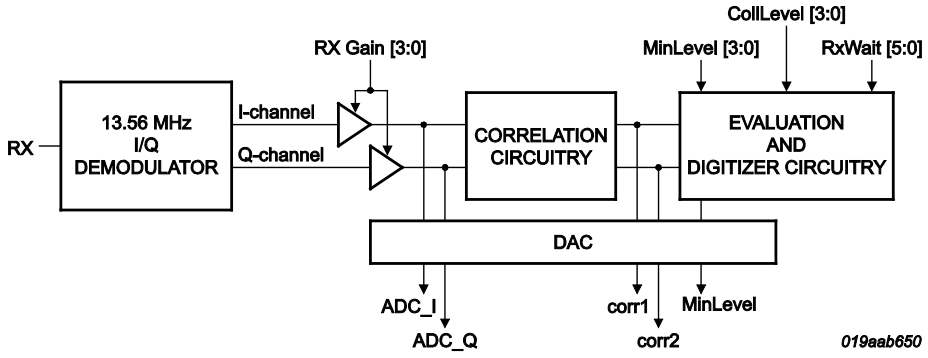


Fig 16. Block diagram of receiver cicuitry

The user may observe the signal on its way through the receiver as shown in the block diagram above. Two signals at a time may be routed to pin AUX1 and AUX2 using the AnalogTestReg-Register.

For each bit-half of the Manchester coded signal the correlation results are evaluated. The evaluation and digitizer circuit decides from the signal strengths of both bit-halves, whether the current bit is valid, and, if it is valid, the value of the bit itself or whether the current bit-interval contains a collision.

To do this in an optimum way, the user may select the following levels:

• MinLevel: Defines a threshold level for the internal decoder, which requires a signal that exceeds the noise by some amount to be detected.

• CollLevel: Defines the minimum signal strength that has to be exceeded by the weaker half-bit of the Manchester-coded signal to generate a bit-collision. If the signal's strength is below this value, a 1 and 0 can be determined unequivocally. CollLevel defines the minimum signal strength relative to the amplitude of the stronger half-bit.

After transmission of data, the card is not allowed to send its response before a certain time period, called frame guard time in the standard ISO14443. The length of this time period after transmission shall be set in the RxWait-Register. The RxWait-Register defines when the receiver is switched on after data transmission to the card in multiples of one bit-duration.

4. Overview of mandatory registers

Table 1 shows the configuration settings for different Reader/Writer modes. The register reset values represent the values after a power-up or reset. Please note that some settings may differ for different antenna configurations and tuning. The registers are described in the following chapter. The appended troubleshooting guide may help to track down and resolve technical problems.

Table 1. Default register setup during communication

Register Name and Address	Register Reset Value	ISO/IEC 14443A PCD	ISO/IEC 14443B PCD	Felica™ Reader	NFC Initiator
Bit Rate (kBit/s)		**106**	**106**	**212**	**106**
Control 0Ch	00h	10h	10h	10h	10h
TxMode 12h	00h	80h	83h	92h	81h
RxMode 13h	00h	80h	83h	92h	81h
TxControl 14h	80h	83h	83h	37h	88h
TxAuto 15h	00h	77h		37h	88h
RxThreshold 18h	84h	75h	75h	55h	55h
Demod 19h	8Dh	4Dh	4Dh	41h	61h
ModWidth 24h	26h	26h	26h	26h	26h
RFCfg 26h	48h	59h	59h	59h	59h
GsN 27h	88h	F4h	FFh	FFh	F4h
CWGsP 28h	20h	3Fh	3Fh	3Fh	3Fh
ModGsP 29h	20h	03h	03h	03h	03h

Remark:

For debugging purposes it would be advantageous to give access to the following register in Table 2.

Table 2. Registers for Debug Purpose

Register Name and Address	Description
TxSelReg 16h	Selects the in put for driver TX1 and TX2 and the input for the SIGOUT signal
TestSel1Reg 31h	Testbus can be propagated to SIGOUT
TestSel2Reg 32h	Selects the required signal for the testbus
TestPinEnReg 33h	Enables the TestPins
AnalogTestReg	Controls the AUX1 and AUX2 pins

4.1.1 TxModeReg (12h)

The TxModeReg is used to adjust the transmission baud rate and framing, respectively.

The baudrate and framing needs to be set by **TxSpeed** and **TxFraming** to the required protocol standard.

The **TxMix** bit is only set during communication with S2C connected devices. The signal coming through SIGIN is then feed to the internal coder of the PN512.

4.1.2 RxModeReg (13h)

The RxModeReg is used to adjust the reception baud rate and framing, respectively.

The baudrate and framing needs to be set by **RxSpeed** and **RxFraming** to the required protocol standard.

To counteract received noise in the datastream, the **RxNoErr** bit can be set to 1. A not valid data stream composed of less then 4 bits will be ignored. The receiver stays active.

The **RxMultiple** can be used to receive more than one data frame without switching off the receiver. If set to logic 0, the receiver is deactivated after receiving a data frame. If the bit is set to logic 1, it is possible to receive more than one data frame. This bit is only valid for 212 and 424 kbit to handle the Polling command. Having set this bit, the receive and transceive commands will not terminate automatically. In this case the multiple receiving can only be deactivated by writing any command (except the Receive command) to the CommandReg register or by clearing the bit by the host controller.

If set to logic 1, at the end of a received data stream an error byte is added to the FIFO. The error byte is a copy of the ErrorReg register.

4.1.3 TxControlReg (14h)

The TxControlReg is used to enable and adjust the Tx1 and Tx2 drivers.

The normal operating mode during a reader/writer application is when both drivers are switched on and deliver the signal 180 degree phase shifted.

This is accomplished by switching both drivers on, hence Tx1RFen and Tx2RFen are set to logic 1, and one driver needs to be inverted – InvTx2RFOn is set to 1. This is reflected in a register setting of

14h 83h

If the **CheckRF** is set to logic 1, Tx2RFEn and Tx1RFEn can not be set if an external RF field is detected. This is only valid when used in combination with bit Tx2RFEn or Tx1RFEn.

The **Tx2CW** is delivering the continuous wave 13.56MHz signal. This setting can be useful during debugging.

4.1.4 TxAutoReg (15h)

If **AutoRFOFF** is set to 1, all active antenna drivers are switched off after the last data bit has been transmitted according to NFCIP-1.

Force100ASK forces a 100% ASK modulation independent of the setting in register ModGsPReg.

CAOn is used for collision avoidance. The value n is set in accordance to the NFCIP-1 standard.

If the bit AutoWakeUp in the register TxAutoReg is set and an external RF field is detected, the Soft Power-down mode is left automatically.

When **InitialRFOn** is set to logic 1, the initial RF collision avoidance is performed and the bit InitialRFOn is cleared automatically, if the RF is switched on.

If Tx1RFAutoEN/Tx2RFAutoEN is set to logic 1, the driver Tx1/Tx2 is switched on after the external RF field is switched off according to the time TADT. If the bits InitialRFOn and Tx1RFAutoEn/ Tx2RFAutoEn are set to logic 1, Tx1/Tx2 is switched on if no external RF field is detected during the time TIDT.

4.1.5 RxThresholdReg (18h)

The DemodReg sets the threshold values for the bit decoder and is composed of MinLevel and CollLevel. The MinLevel defines the minimum signal strength at the correlator output that shall be accepted.

The **MinLevel** defines a threshold level for the internal decoder, which requires a signal that exceeds the noise by some amount to be detected. The lowest threshold value is

when the MinLevel is set to 0. Fig 17 shows the concept of two different settings for the MinLevel.

If MinLevel is set to 5 for example it can be seen that at time A and E – representing valid data bits - the signal is above the threshold. If the signal is only a short time over the threshold, it will not be detected (less than half bit length)

If the threshold level is chosen too low (represented by MinLevel set to 1), then the correlator output is too long over the threshold and noise can be detected as data bits.

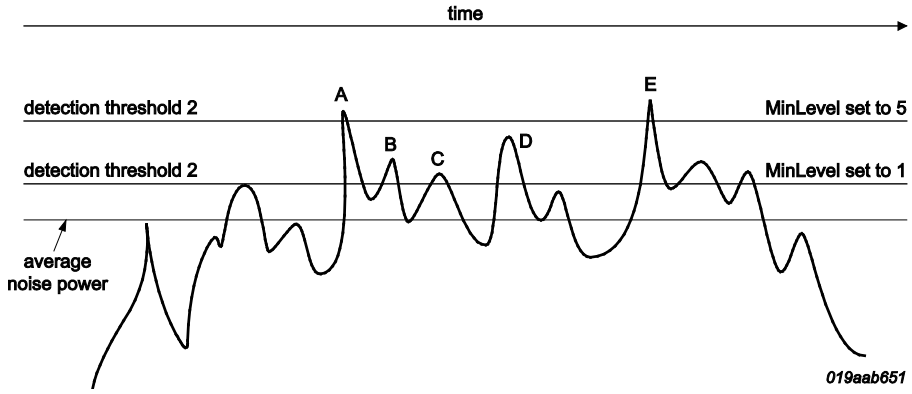


Fig 17. Threshold levels

The CollLevel (Collision Level) defines the minimum relation between the bit half with stronger signal and the bit half with the weaker signal.

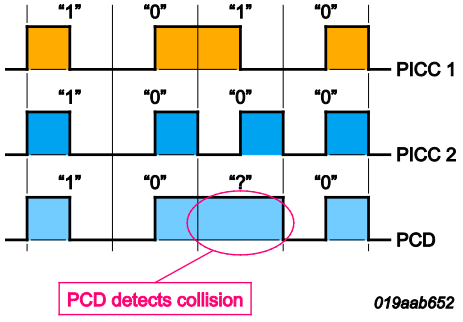


Fig 18. Collision is detected

4.1.6 DemodReg (19h)

The DemodReg defines different settings for the demodulator. This will be explained in the following section:

AddIQ defines the use of the I and Q channel during reception. The settings can only be adjusted if FixIQ has been set to logic 0. Since the receiver uses I/Q demodulator, different settings are available:

00	This settings selects the stronger channel during reception
01	Selects the stronger channel and freeze the selected during communication.
10	Combines the I and Q channel. This settings is only applicable for Type-A modulation.

FixIQ can be used to fix the reception on either channel I or Q.

The PN512 IC uses a phase locked loop (PLL) mechanism to lock on the preamble of the received card data. **TauRcv** and **TauSync** are used to adjust parameters of the PLL.

The TauSync parameter is required to synchronize on the preamble of the card. Therefore, a short so-called Tau value is needed to follow quickly the signal of the preamble.

Once the loop is phase locked, the PN512 switches to receiving mode and uses the value of TauRcv. A lower value of TauRcv is required to provide stability for input frequency changes and thus gives the ability to recapture the signal if the system is thrown out of lock by a noise transient.

4.1.7 ModWidthReg (24h)

The ModWidthReg defines the width of the Miller modulation.

4.1.8 RFCfgReg (26h)

RFCfgReg configures receiver gain and RF level detector sensitivity

The RF level detector is integrated to fulfill NFCIP1 protocol requirements (e.g. RF collision avoidance). Furthermore the RF level detector can be used to wake up the PN512 and to generate an interrupt.

The sensitivity of the RF level detector is adjustable in a 4-bit range using the bits RFLevel in register RFCfgReg. The sensitivity itself depends on the antenna configuration and tuning.

Possible sensitivity levels at the RX pin are listed in the datasheet

To increase the sensitivity of the RF level detector, an amplifier can be activated by setting the bit RFLevelAmp in register RFCfgReg to 1.

Remark: During soft Power-down mode the RF level detector amplifier is automatically switched off to ensure that the power consumption is less than 10 µA at 3 V.

Remark: With typical antennas lower sensitivity levels can provoke misleading results because of intrinsic noise in the environment.

Note: It is recommended to use the bit RFLevelAmp only with higher RF level settings.

4.1.9 GsNOnReg (27h)

GsNOnReg is used to define the output-N driver for times of modulation and for times of no modulation. Both values are left unchanged since only the P-drivers are used for modulation.

4.1.10 CWGsOReg (28h)

CWGsOReg defines the conductance of the P-driver during times of no modulation.

This may be used to regulate the output power and subsequently current consumption and operating distance.

Fig 19 and Fig 20 shows different values and the impact on the output power.

Remark: the values and results are based on a demoboard antenna and can not be taken as absolute values for reference. Hence, the output power will vary with the antenna.

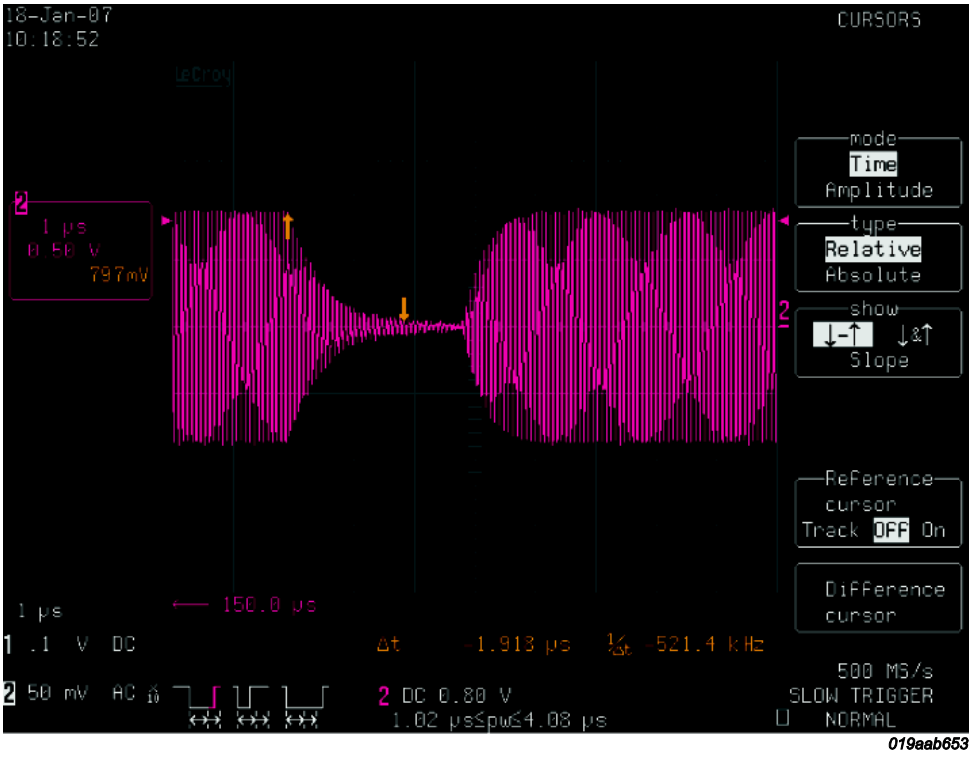


Fig 19. CWGSOReg set to 28 0F

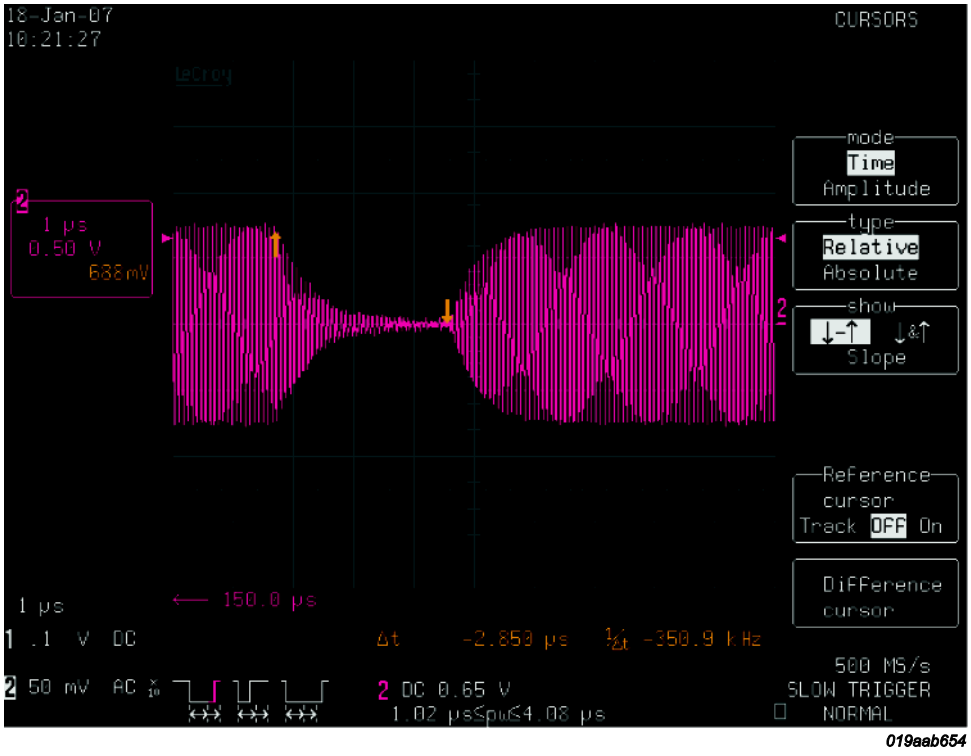


Fig 20. CWGSOReg set to 28 0A

4.1.11 ModGsPReg (29h)

The ModGsPReg defines the conductance of the output P-driver during modulation. It is mainly used to adjust the modulation index for Type-B. The value depends on the antenna tuning and the final environment.

A good starting value would be 04h and needs to be adjusted accordingly. The following Fig 21 and Fig 22 show the impact of modulation index when changing the register value. A lower value would increase the modulation index.

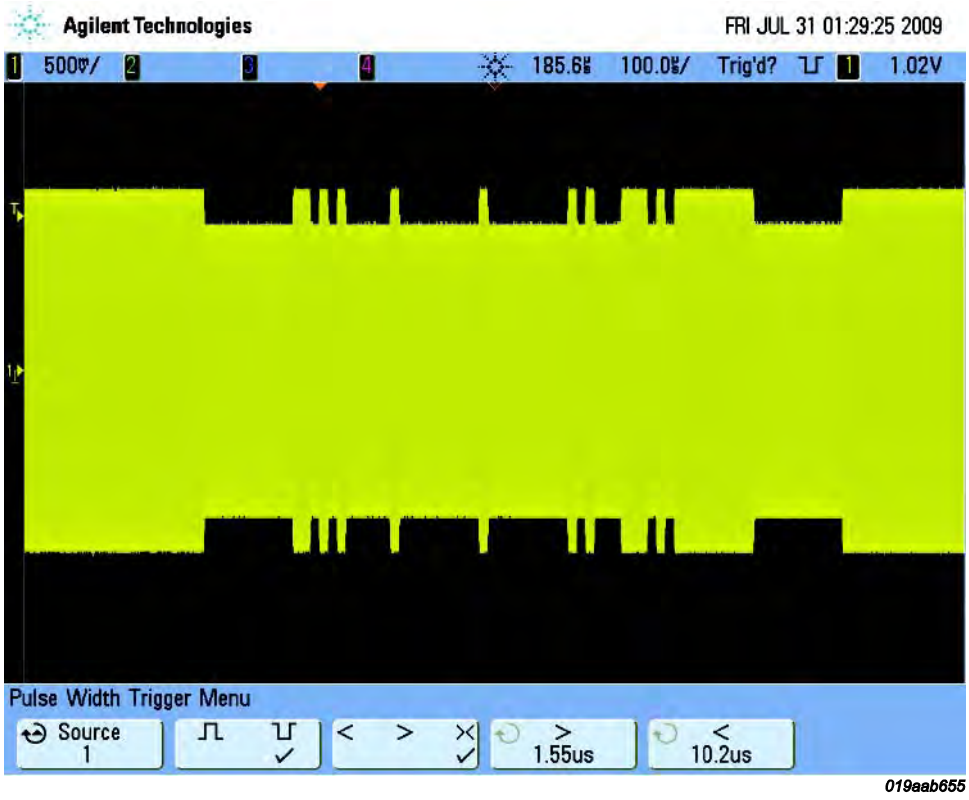


Fig 21. ModGsPReg set to 04h

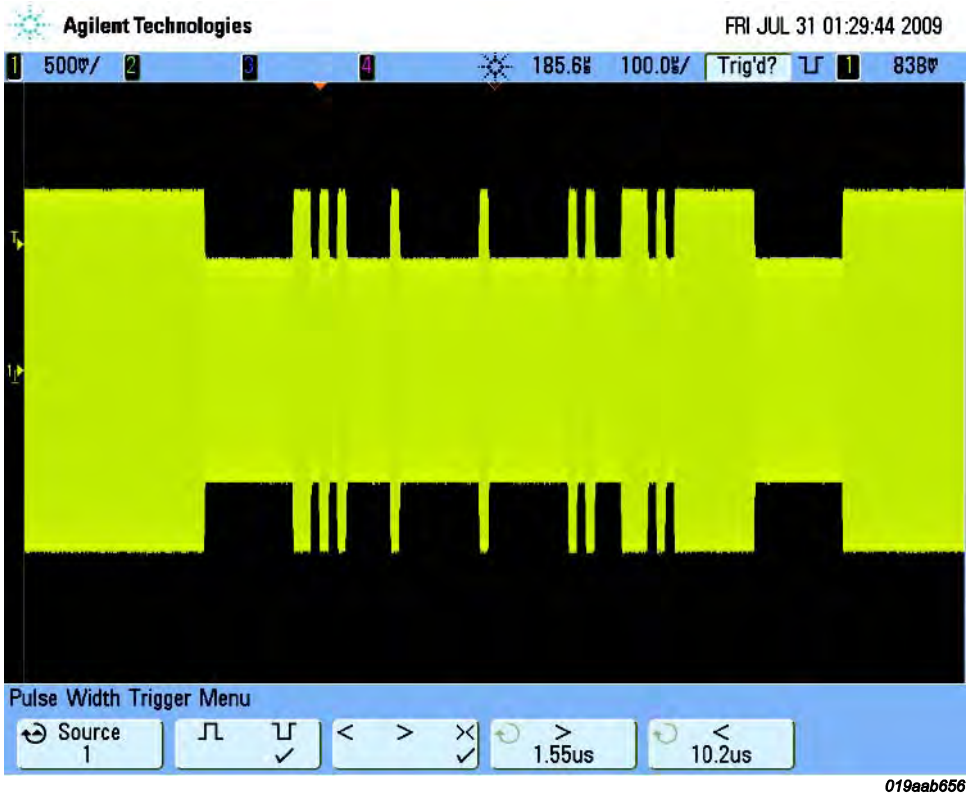


Fig 22. ModGsPReg set to 02h

4.2 Transmitter Pin Structure

For a better understanding of the modulation relevant register, the following Fig 23. depicts the transmitter structure.

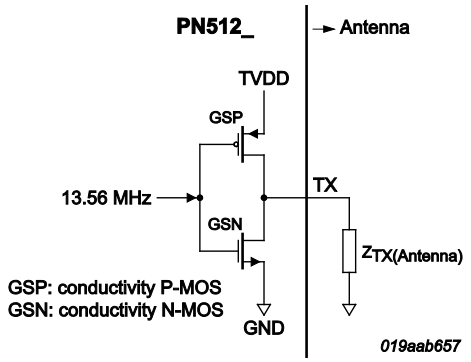


Fig 23. Transmitter structure

We also distinguish between modulation and no modulation in the register description, which shall be visualized in Fig 24.

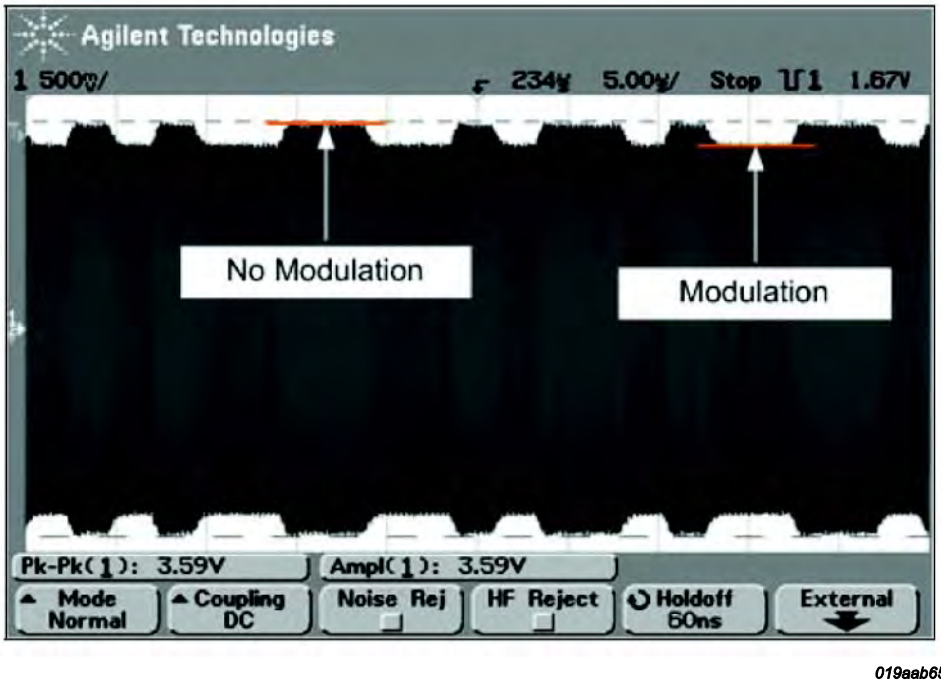


Fig 24. Modulation visualization

4.3 Timer Unit

A timer unit is implemented in the PN512. The external host controller may use this timer to manage timing relevant tasks. The timer unit may be used in one of the following configurations:

- Time-out counter

- Watch-dog counter
- Stop watch
- Programmable one-shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time.

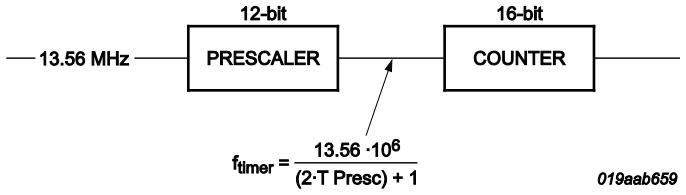


Fig 25. Timer Schematic

The timer has an input clock of 13.56 MHz (derived from the 27.12 MHz quartz). The timer consists of two stages: 1 prescaler and 1 counter as shown in Fig 25.

The prescaler is a 12-bit counter. The reload value for TPrescaler can be defined between 0 and 4095 in register TModeReg and TPrescalerReg.

The reload value for the counter is defined by 16 bits in a range of 0 to 65535 in the register TReloadReg.

More information on the timer unit can be found in the datasheet [2].

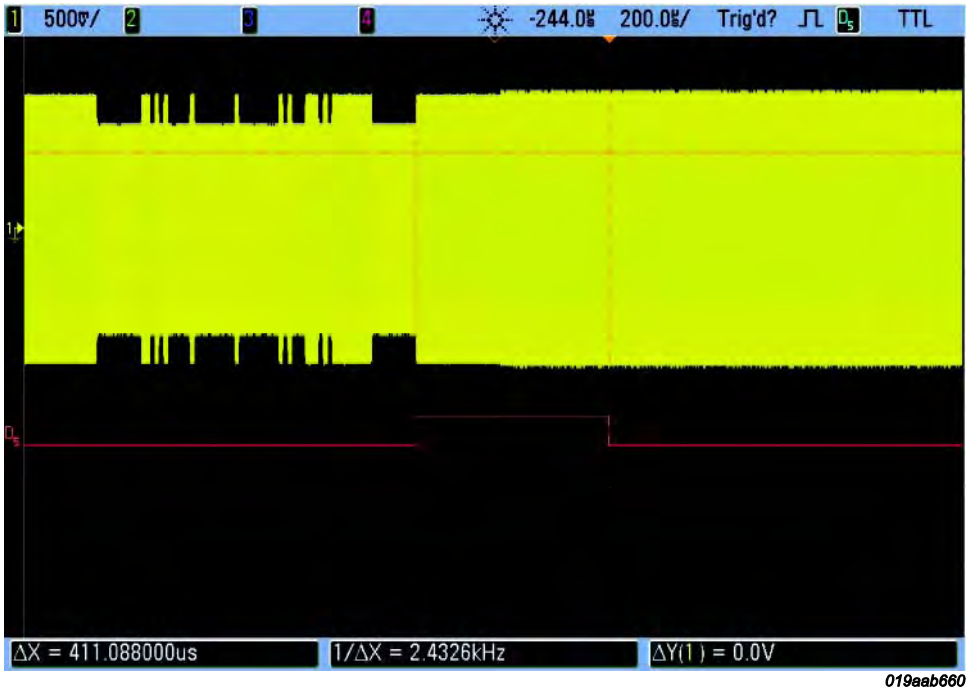
The time calculation using the timer can be summarized with the following equation:

$$t = \frac{(T\,\mathrm{Pr}\,escaler \cdot 2 + 1) \cdot T\,\mathrm{Re}\,load + 1}{13560000}$$

4.3.1 Timer Example 1 – Time Measurement between Events

The following example shows how to measure the time between two events. The timer is started automatically after the end of transmission and stops after the 5th bit (1 startbit, 4 stopbits) in this example. The example shows a REQB and the corresponding tag answer.

Fig 26 shows a visualization of this measurement. It can be seen that a REQB signal is sent by the reader. After end of transmission of REQB the timer is started automatically. This can be seen by the red signal at the bottom of the picture.



(2) The digital signal at the bottom shows the timer running

Fig 26. Time measurement example

Fig 27 shows a zoom of the tag response in Fig 23. Furthermore, the stop condition can be depicted starting from the phase shift after the preamble until the 5th bit (1 startbit, 4 databits).

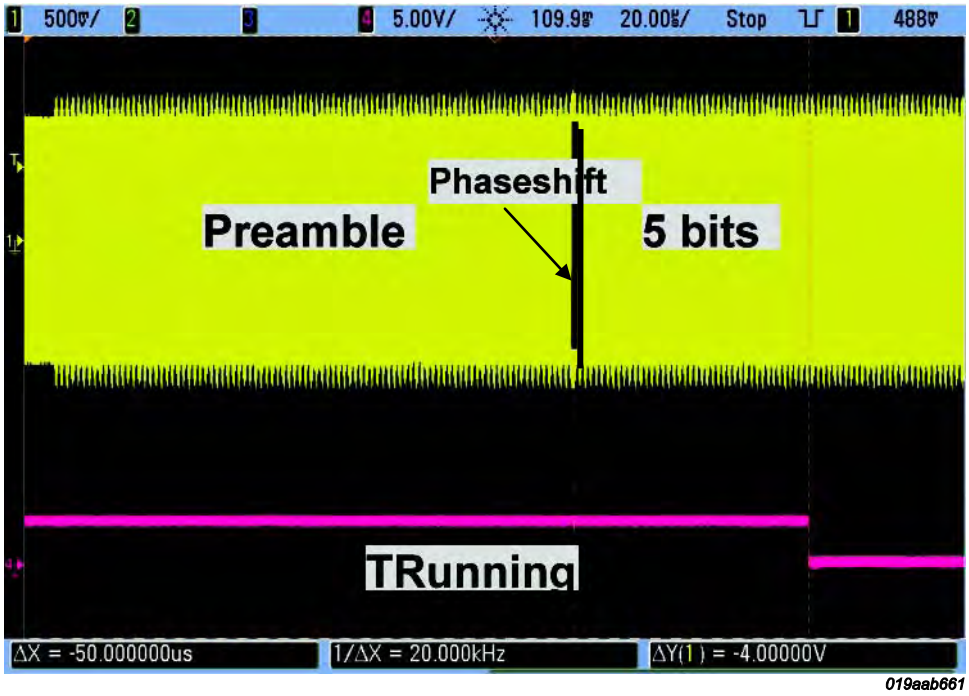


Fig 27. Tag response zoom

The total time of TRunning is measured at 411us with the oscilloscope (see Fig 26).

The total time calculated out of the software depends on the prescaler (TPrescaler), timer reload value (TReloadReg) and the counter value (TCounterValReg) at the end of the transmission.

For this example the prescaler was set to

Register	Value
2Ah	80h
2Bh	07h

The timer reload value was set to

Register	Value
2Ch	FFh
2Dh	F8h

The REQB command is started after this configuration.

After the timer has stopped, we read out the counter value in register TCounterValReg.

The counter value is read

Register	Value
2Eh	FEh
2Fh	85h

Now, the counter value is subtracted from the reload value.

Register	Value in Hex	Value in Dec
Reload Value	FF F8	65528
Counter Value	FE 85	65157
Results		**371**

Total Time:

$$T_{tot} = \frac{(T\,\mathrm{Pr}escaler \cdot 2 + 1) \cdot T\,\mathrm{Re}load + 1}{13560000}$$

The formula for calculating one clock cycle is

$$t_{clk} = \frac{2 \cdot \mathrm{Pr}escaler + 1}{13560000}$$

with Prescaler = 7

t_{clk}=1,10619 us

Total time (T_{tot}) when TimerIRQ is generated:

$$Ttot = tclk \cdot \frac{\mathrm{Re}loadValue + 1 - CounterValue}{13560000}$$

T_{tot}=411,57 us

4.3.2 Timer Example 2 – Timeout configuration

The following example shows the usage of the timer for a timeout. The Frame Waiting Times (FWT) for different Frame Waiting Time Integers (FWI) are taken as basis for the timeout calculation and configuration.

Baudrate	D	1 etu [s]
106kBit/s	1	9,43953E-06

FWI	FWT [s]	FWT [ms]	**Number of ETUs required for FWT**	TReload value to be set in DEC	TReload value to be set in HEX
0	0,000302065	0,302	32	4	0004
1	0,00060413	0,604	64	8	0008
2	0,00120826	1,208	128	16	0010
3	0,002416519	2,417	256	32	0020
4	0,004833038	4,833	512	64	0040
5	0,009666077	9,666	1024	128	0080
6	0,019332153	19,332	2048	256	0100
7	0,038664307	38,664	4096	512	0200
8	0,077328614	77,329	8192	1024	0400
9	0,154657227	154,657	16384	2048	0800
10	0,309314454	309,314	32768	4096	1000
11	0,618628909	618,629	65536	8192	2000
12	1,237257817	1237,258	131072	16384	4000
13	2,474515634	2474,516	262144	32768	8000
14	4,949031268	4949,031	524288	65536	FFFF

TPrescaler	512
TReload	1
Time unit	7,56637E-05

Number of ETUs for 1 TimeUnit	8,015648796 ~ 8 ETU

As an example the TReload is set to 0008 to indicate 0.604ms. Fig 28 shows the signal of TRunning.

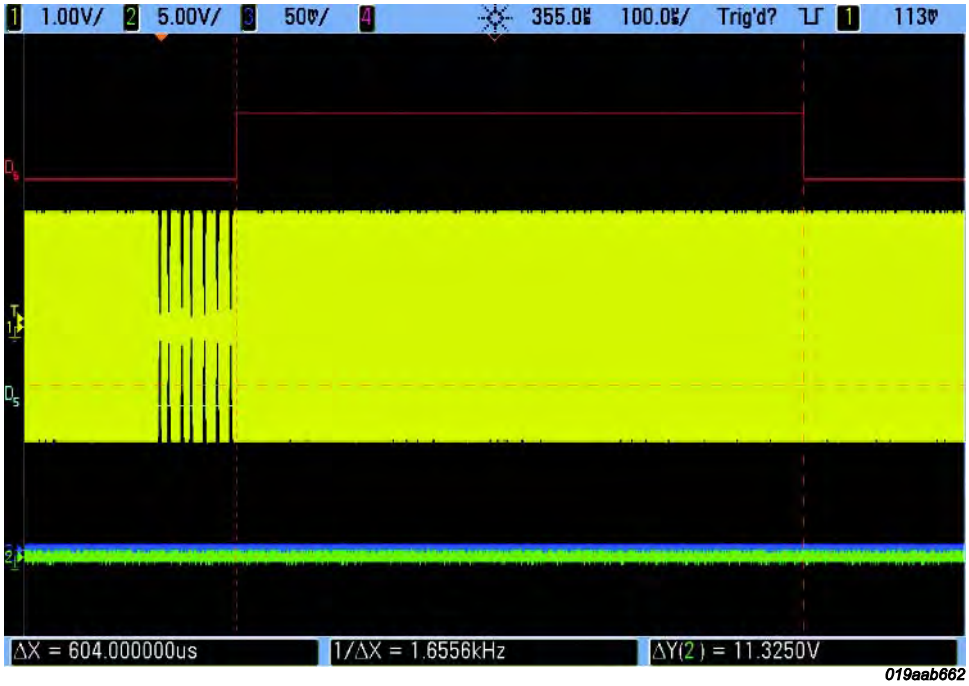
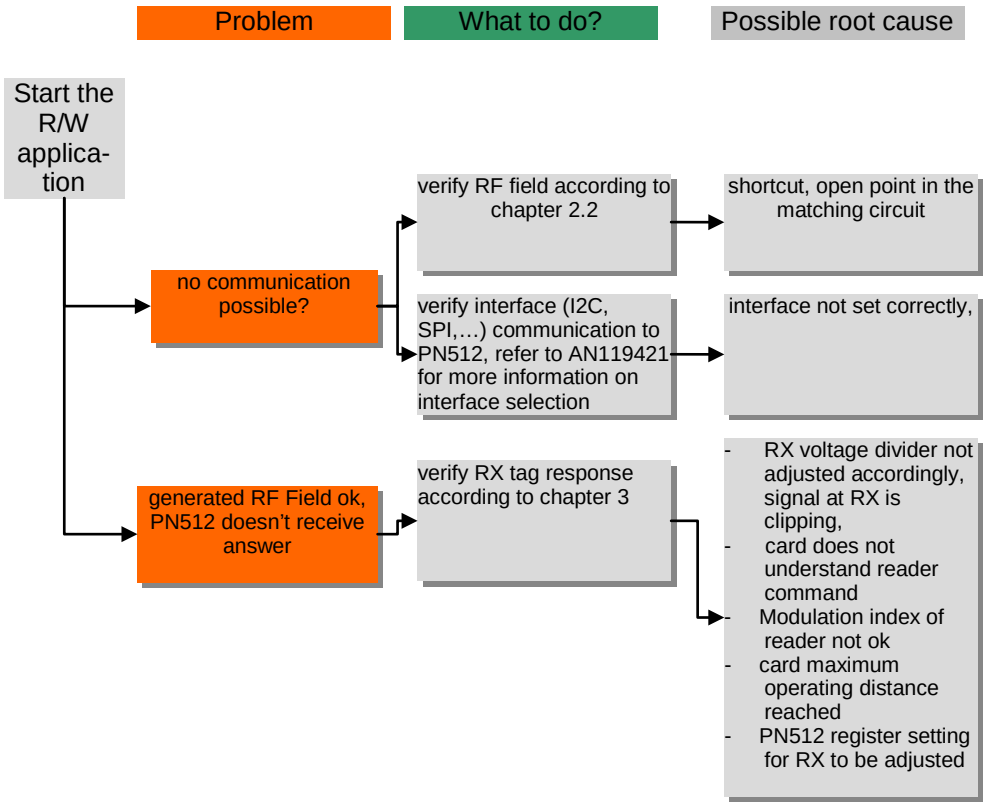


Fig 28. TRunning on the red signal

5. Troubleshooting Guide

This troubleshooting section should support you in finding the root cause of the problem. This list is not exhaustive since the source of problem is different in each application.



6. References

[1] AN1425xx – RF Amplifier for NXP Contactless Reader IC's

[2] 1113xx – PN512 Datasheet

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