AN11019

CLRC663, MFRC630, MFRC631, SLRC610 Antenna Design Guide

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Document information

Info	Content
Keywords	CLRC663, MFRC630, MFRC631, SLRC610, antenna design, antenna tuning, matching procedure
Abstract	This document describes the principles of antenna tuning for the contactless reader IC CLRC663, MFRC630, MFRC631, SLRC610. A practical example is given to tune an ID2±10 antenna for all baud rates according to ISO/IEC 14443 and ISO/IEC 15693.

Revision history

Rev	Date	Description
1.5	20180626	Editorial updates
1.4	20170305	Update for CLRC663 *plus*
1.3	20160510	Removed reference to crystal in Section 4 CLRC663 hardware design
1.2	20150907	Rework of the design guide
1.1	20150126	Debugging part added (chapter 7)
1.0	20150501	Initial Version

Contact information

For more information, please visit: http://www.nxp.com

1. Introduction

The antenna design for the CLRC663 is not much different than the antenna designs for most of the other NXP reader ICs in general. However, some CLRC663 specific details need to be considered to get an optimum performance.

This document describes the generic NFC and RFID antenna design rules in section 3 as simple as possible, considering the different requirements due to ISO/IEC 14443, NFC or EMVCo as introduced in section 2.

The section 4 describes the antenna design for the CLRC663 in detail.

In the Annex in section 5 some basics about the antenna impedance measurement and the related tools can be found.

2. NFC Reader antenna design

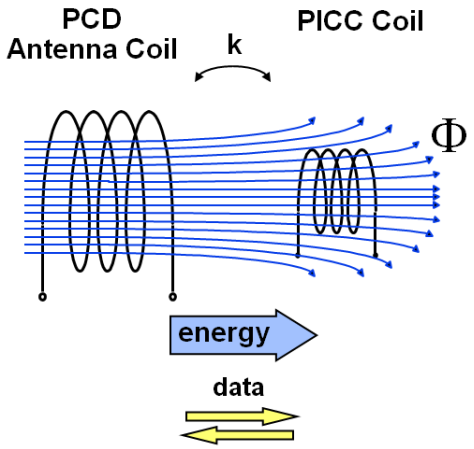
2.1 ISO/IEC 14443 specifics

The ISO/IEC 14443 (called “ISO” in the following, details see [2]) specifies the contactless interface as widely being used with contactless smartcards like e.g. MIFARE product-based cards.

The ISO/IEC 14443 defines the communication between a reader (“proximity coupling device” = PCD) and a contactless smartcard (“proximity chip card” = PICC). In four parts it describes the physical characteristics (i.e. the size of the PICC antennas), the analog parameters like e.g. modulation and coding schemes, the card activation sequences (“Anti-collision”) and the digital protocol. The ISO/IEC 10373-6 (see [3]) describes the test setup as well as all the related tests for cards and the reader.

The ISO/IEC 14443 reader antenna consists of an antenna coil, which is matched to the reader IC. This antenna coil, as shown in Fig 1,

1. generates the magnetic field to provide the power to operate a card (PICC),
2. transmits the data from the reader (PCD) to the card (PICC), and
3. receives the data from the card (PICC) to the reader (PCD).



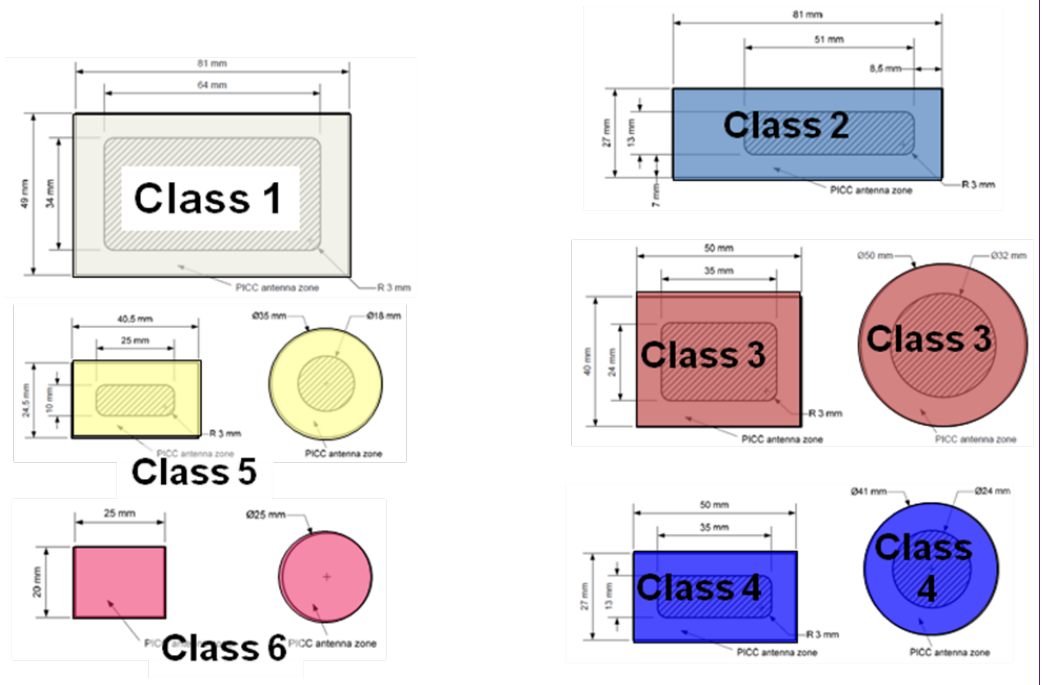
(1) k = coupling coefficient

(2) Φ = magnetic flux

Fig 1. Magnetic coupling between reader (PCD) and card (PICC)

According to ISO the PICC antenna coils can be categorized into the classes 1 to 6, as shown in Fig 2.

The PCD antenna is not defined as such, but the PCD must support the classes 1, 2, and 3. The support of the classes 4, 5, and 6 is optional.



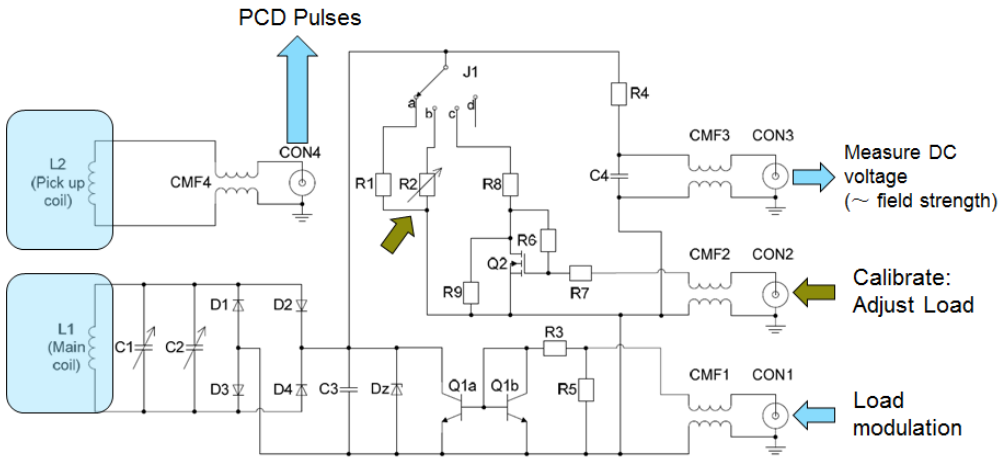
(1) A PCD must always support the classes 1, 2, and 3.

Fig 2. PICC classes according to ISO/IEC 14443

The PCD antenna coil sizes are not specified. So for ISO/IEC 14443 compliant readers all different sizes of antenna coils from a few 10 mm^2 up to 20 cm diameter can be found in various shapes.

ISO/IEC 14443 does not specify an operating volume. The reader manufacturer needs to guarantee that within the operating volume - that he himself defines - all related ISO/IEC 10373-6 tests can be passed.

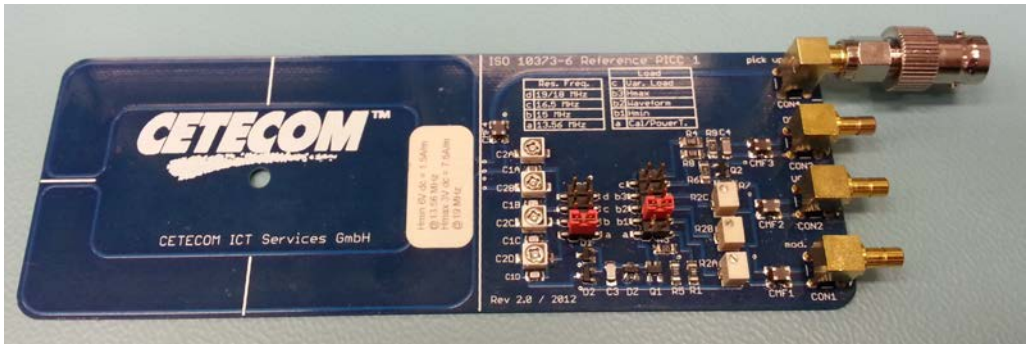
The compliance tests require calibrated reference PICCs, as defined in ISO/IEC10373-6. The schematic of such reference PICC is shown in Fig 3. For each PICC Class there is one reference PICC, which needs to be calibrated according to the required measurement. Practically it makes sense to use one calibrated reference PICC for each measurement case.



(1) Details see [3].

Fig 3. ISO/IEC 10373-6 reference PICC

Some reference PICCs, which are commercially available (e.g. Fig 4), are pre-calibrated and equipped with several jumper options to address the most relevant tests with a single reference PICC.



(1) The jumper settings allow different pre-calibrations.

Fig 4. ISO/IEC 10373-6 reference PICC Class 1

Still for each PICC Class a separated reference PICC is required.

The **most** relevant analog tests for PCDs are:

1. Field strength tests (min and max)
2. Wave shape tests (for all bit rates)
3. Load modulation amplitude tests

Note: This application note does not replace the detailed test description in ISO/IEC 10373-6.

There is no common certification process for ISO/IEC14443 compliance in place, even though many national bodies use ISO/IEC 14443 to operate the electronic passports and electronic ID cards. For these programs, some nations have established a certification process to guarantee interoperability. An example is given in [5].

2.1.1 Field strength tests

For the field strength tests, it is preferred to have the PCD send a continuous carrier, i.e. it performs no modulation.

The field strength tests simply require the calibrated reference PICC and a dc voltage measurement device (volt meter or oscilloscope). The field strength is equivalent to the calibrated (and required) voltage level. ISO/IEC 10373-6 defines minimum voltage levels, corresponding to the minimum required field strength, and maximum voltage levels, corresponding to the maximum allowed field strength. The measured voltage levels must stay in between these limits.

2.1.2 Wave shape tests

The PCD needs to send the related pulse(s): It may send an ISO/IEC 14443 REQA and / or REQB with the required bit rate, as e.g. specified in [5]. Any other command fits the purpose, too.

Note: For the test of higher bit rates it makes sense to implement some specific test commands, which send artificial commands, e.g. REQA and / or REQB, using the coding and modulation of the corresponding higher bit rates. The standard way of activating

higher bitrates cannot be applied, since the reference PICC for ISO/IEC 14443-2 tests does not allow the protocol layer, which is normally required to switch to higher bit rates.

The wave shape tests require:

1. a calibrated reference PICC, which is placed at the position of the calibrated field strength (corresponding to the dc voltage as measured in section 2.1.1),
2. a digital oscilloscope with a measurement bandwidth of 500 M samples or higher, and
3. a tool that filters and transforms the oscilloscope data into the envelope signal according to ISO/IEC 10373-6.

The tool normally returns the filtered and transformed envelop as well as the corresponding values of rise and fall times, residual carrier levels and over- and undershoots, which must be kept within the given limits.

2.1.3 Load modulation tests

The PCD needs to send a test command, which allows to check a response from the reference PICC.

The load modulation tests require:

1. a calibrated reference PICC, which is placed at the position of the calibrated field strength (corresponding to the dc voltage as measured in section 2.1.1) and
2. a signal generator with a pattern generator, that provides the load modulation signal as a response to the PCD test commands.

The response must be triggered by the PCD test command, i.e. the signal generator needs a delayed trigger input either from the field or from the PCD itself. The voltage level of the load modulation input signal for each test case must be (pre-) calibrated in the Test PCD set up.

The PCD must be able to receive all the responses with the given minimum load modulation signal level.

2.2 EMVCo specifics

EMVCo specifies a contactless interface for point of sales (POS) terminals (= PCD) and the corresponding contactless payment cards in [6]. This interface is very similar to the one defined ISO/IEC 14443, but it uses its own set of requirements and specification details. The EMVCo test equipment and way of testing is quite different from the test specification as defined in ISO/IEC 10373-6.

For the reader tests a calibrated EMVCo reference PICC is required. This reference PICC can be bought only from one of the accredited laboratories.

Some of the antenna design parameters also need to be adapted towards EMVCo requirements.

The most relevant analog tests for PCDs are:

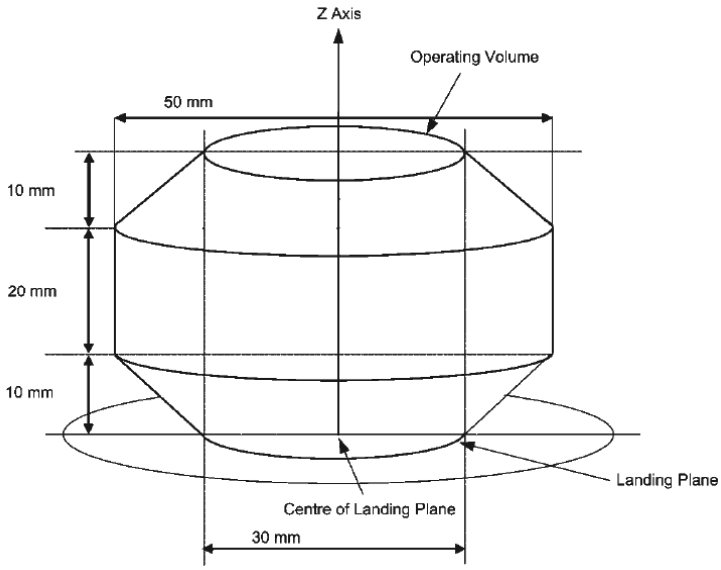
1. PCD power test (field strength),
2. Modulation PCD → PICC tests (wave shape tests) and
3. Load modulation tests.

EMVCo specifies and requires only the bit rate of 106kbit/s for both type A and B, but no higher bit rates.

Note: This application note does not replace the detailed test description in ISO/IEC 10373-6.

2.2.1 EMVCo Operating volume

One main difference for the tests is the definition of an operating volume, as shown in Fig 5. This volume is tested with the EMV-Test-PICC.



(1) Details see [6].

Fig 5. EMVCo POS operating volume requirement

Within this volume, the given parameters need to be fulfilled.

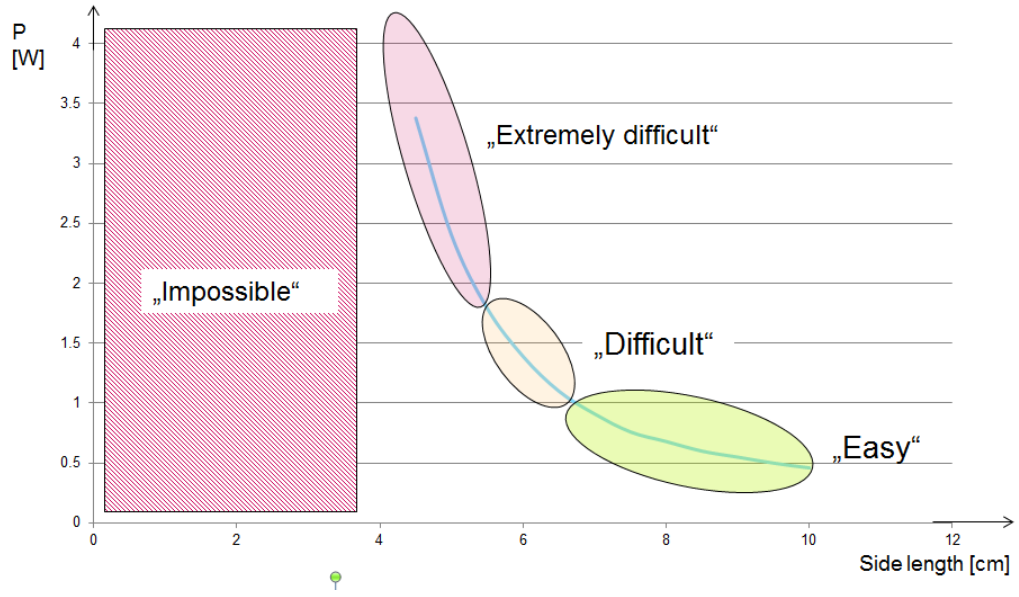
2.2.2 EMVCo Field strength

For the field strength test, it is preferred to have the PCD send a continuous carrier, i.e. it performs no modulation.

The voltage level, which can be measured in all of the given positions, needs to be between the minimum and maximum limit, as given in [6].

Due to the operating volume, it can become challenging to meet the EMVCo requirements with small antennas.

Fig 6 shows the required power versus antenna size. The curve is based on an antenna simulation, which uses a few simplifications, so it does not take the loading effect of the EMVCo reference PICC into account. On the other hand, the simulation was done under ideal environmental conditions, i.e. no metal environment influences the antenna. The simulation results can be taken as reference to estimate the design effort especially for small antennas compared to “normal” antenna sizes.



(1) Side length of a square antenna.

(2) These simulation results do neither take any specific environment nor loading effects into account.

Fig 6. EMVCo POS Reader antenna size

2.2.3 EMVCo Wave shapes

The PCD needs to send the related pulse(s): It may send an EMVCo REQA and / or REQB.

The wave shape tests require:

1. a calibrated EMVCo reference PICC, which is placed at each of the given position (see Fig 5),
2. a digital oscilloscope with a measurement bandwidth of 500Msamples or higher, and
3. a tool that filters and transforms the oscilloscope data into the envelope signal according to the EMVCo test requirement.

The tool normally returns the filtered and transformed envelop as well as the corresponding values of rise and fall times, residual carrier levels and over- and undershoots, which must be kept within the given limits.

2.2.4 EMVCo Load modulation

The PCD needs to send a test command, which allows to check a response from the reference PICC. Typically, the EMVCo loop back command sequence is used for this.

Note: Since these tests do not replace the certification tests as required by EMVCo, simple tests commands might be even more useful than the full EMVCo test sequence. Such a simple test command can be easily debugged and typically allows an easier triggering.

The load modulation tests require:

1. a calibrated reference PICC, which is placed at each of the given position (see Fig 5) and
2. a signal generator with a pattern generator, that provides the load modulation signal as a response to the PCD test commands.

The response must be triggered by the PCD test command, i.e. the signal generator needs a delayed trigger input either from the field or from the PCD itself. The voltage level of the load modulation input signal for each test case must be set according to [6].

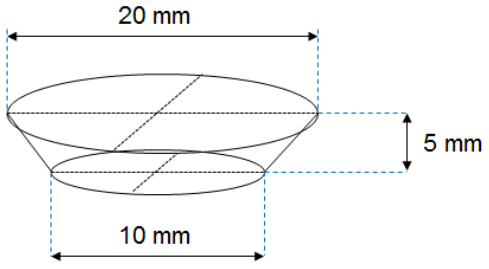
The PCD must be able to receive all the responses with the given minimum load modulation signal level.

2.3 NFC specifics

The standard NFC device needs to fulfill the reader mode (PCD), the passive target and the passive initiator. The passive target from an antenna point of view is very similar to the optional card mode (PICC).

2.3.1 NFC Operating volume

The NFC Forum specifies an operating volume as shown in Fig 7.



(1) Details see NFC Analog Technical Specification, [4]

Fig 7. NFC Forum operating volume

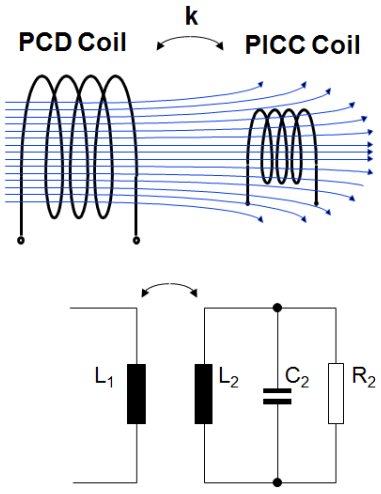
3. Generic PCD antenna design rules

Some of the design rules are very common for NXP NFC Reader designs, i.e. they do neither specifically depend on the used standard (ISO, NFC or EMVCo) nor depend on the NXP Reader IC but rather on physical or technical basics.

3.1 Optimum Antenna Coil

The optimum antenna coil size for a standard PCD can be derived from the Biot-Savart law. The major prerequisites are some simplifications like the assumption that the antenna system is optimized based on the parallel operation of smart cards on top of the PCD antenna. The optimization is derived for the operating distance, i.e. the target is to show the optimum PCD antenna size for a given required operating distance.

The principle and simplified electrical circuit is shown in Fig 8.



(1) Index 1: PCD
(2) Index 2: PICC

Fig 8. PCD Antenna coil

The index 2 indicates the parameters of the PICC. Here the PICC is taken as given, i.e. the parameters with the index 2 cannot be modified. This is another simplification, but also refers to the reality, where the reader antenna optimization does not allow to change card parameters.

The PCD antenna is taken as a circular antenna to allow a simple calculation. The impact of different form factors is discussed later.

Out of this law the coupling coefficient *k* between PCD and PICC antenna can be described as following:

$$k = \mu_0 \cdot \frac{r^2}{2(r^2 + x^2)^{3/2}} \cdot \frac{A_2}{\sqrt{L_{01} \cdot L_{02}}} \quad (1)$$

A_2 = Card antenna coil area, fixed

L_{02} = Card antenna coil single turn inductance, fixed

L_{01} = Reader coil single turn inductance

r = Reader Antenna coil radius

x = Operating distance in the center of the Reader antenna

μ_0 = relative permeability

The single turn inductance can be described like this:

$$L_{01} \approx \frac{2 \cdot 10^{-7}}{[m]} \cdot 2\pi \cdot r \cdot \ln\left(\frac{2\pi \cdot r}{d}\right) \quad (2)$$

d = coil wire diameter with *d* << *r*

Note: The formula to calculate the inductance of the antenna coil can only be taken as reference. In real life, many details influence the result, which are not considered in this simple formula. So, a measurement of the coil parameters as described below is required anyway.

3.1.1 Number of turns

Changing the number of turns does not change the coupling, since the inductance itself has no influence on the coupling. So, in principle antenna coils with a single turn can be used as well as antenna coils with many turns.

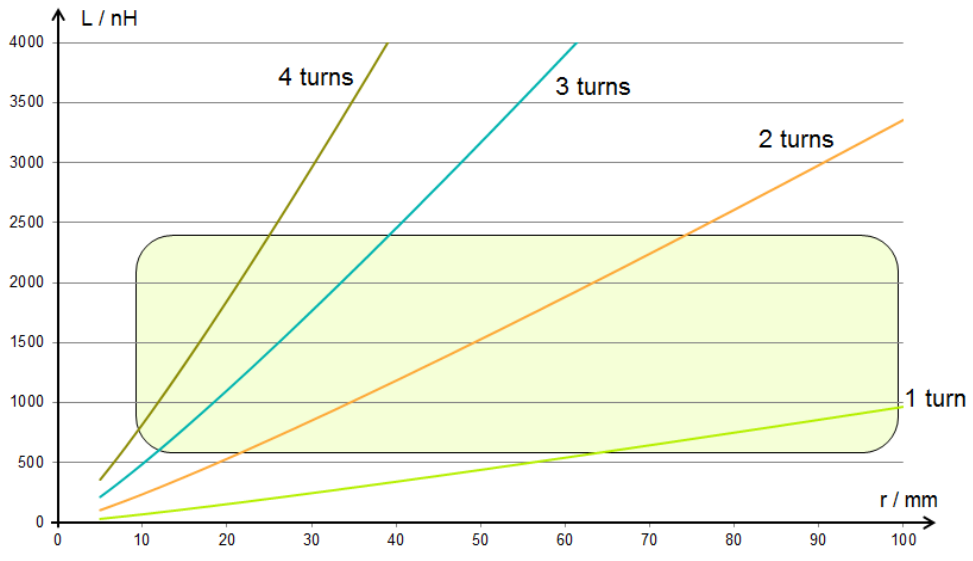
The only remaining parameter to optimize the coupling is the antenna radius r (i.e. the antenna size), and will be discussed in section 3.1.2.

However, the number of turns changes the inductance which on one hand changes the matching circuit.

Out of experience it turns out to be optimum to have an inductance around L ≈ 1 µH for a proper matching, but a wide range of L ≈ 300 nH up to L≈ 4 µH still can be matched properly, so typically 1 up to 4 turns in the normal range of antenna sizes are used.

The Fig 9 shows the typical inductance values versus the antenna coil radius for 1, 2, 3 and 4 turns. These values are just examples, since the environment, the track width or wire thickness and some other parameters may influence the inductance.

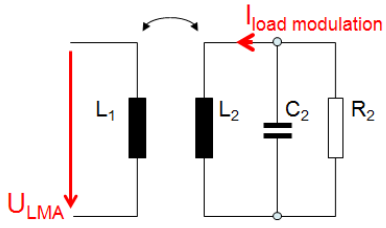
Furthermore, the typical PCD antenna coil does not use the circular shape, but rather a rectangular form factor. The given calculated values show the wide range that can be used, and shall be used as reference only. The antenna coil inductance must be measured anyway later to do the antenna matching.



(1) Green area: target area for standard antenna matching.

Fig 9. Inductance examples versus coil radius

On the other hand, the number of turns defines the relationship of voltage level versus current level. Especially for the load modulation (see Fig 10) it might be helpful to increase the number of turns on the PCD antenna coil.



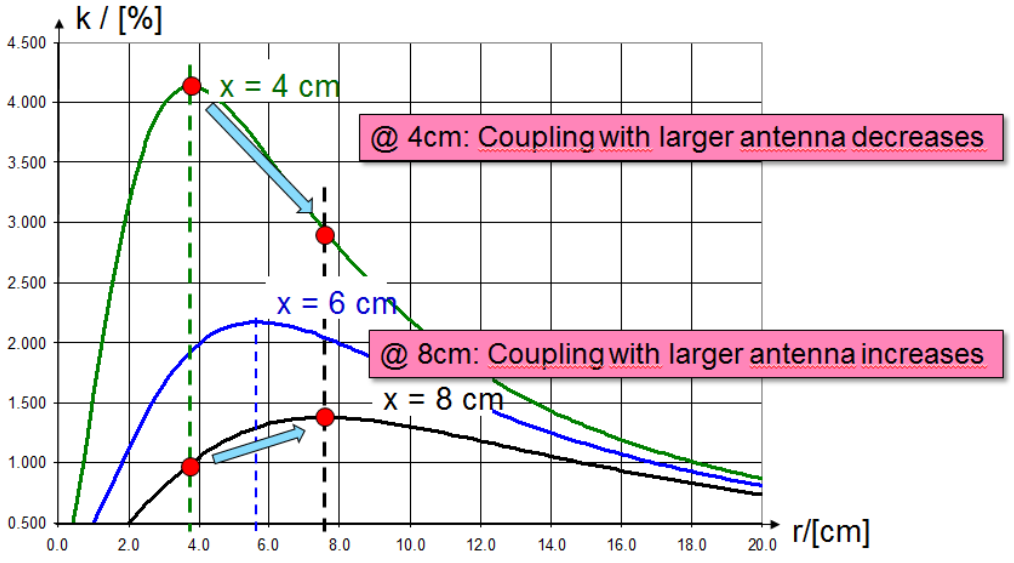
(1) Index1 = PCD

(2) Index 2 = PICC antenna coil

Fig 10. Load modulation

3.1.2 Optimum antenna coil size

Fig 11 shows the coupling coefficient versus antenna radius for three different operating distances. The scaling of the coupling coefficient does not necessarily show the correct absolute value, since some of the fixed parameters are estimated only for this graph. However, the relative value is important to indicate the optimum antenna size.



(1) Green: at a distance of x = 4 cm

(2) Blue: at a distance of x = 6 cm

(3) Black: at a distance of x = 8 cm

(4) The coupling coefficient scaling in this diagram is relative only. The absolute value might differ.

Fig 11. Coupling coefficient vs PCD antenna radius

The maximum coupling can be achieved, when

$$r = x \tag{3}$$

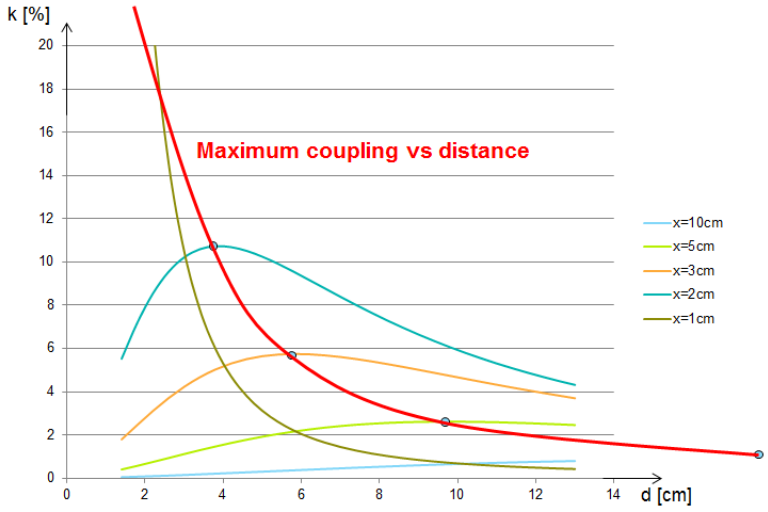
r = Reader Antenna coil radius

x = Operating distance in the center of the Reader antenna

The maximum coupling at an operating distance of 4 cm can be achieved with an antenna coil of approximately 4 cm radius (i.e. 8 cm diameter). Increasing the antenna radius from 4 cm to 8 cm decreases the coupling at 4 cm distance (green curve), but increases the coupling at 8 cm distance (black curve).

However, the optimum antenna size as such does not guarantee that the coupling is strong enough.

The maximum coupling coefficient versus the operating distance can be estimated as shown in Fig 12. This maximum coupling is related to the optimum antenna size.



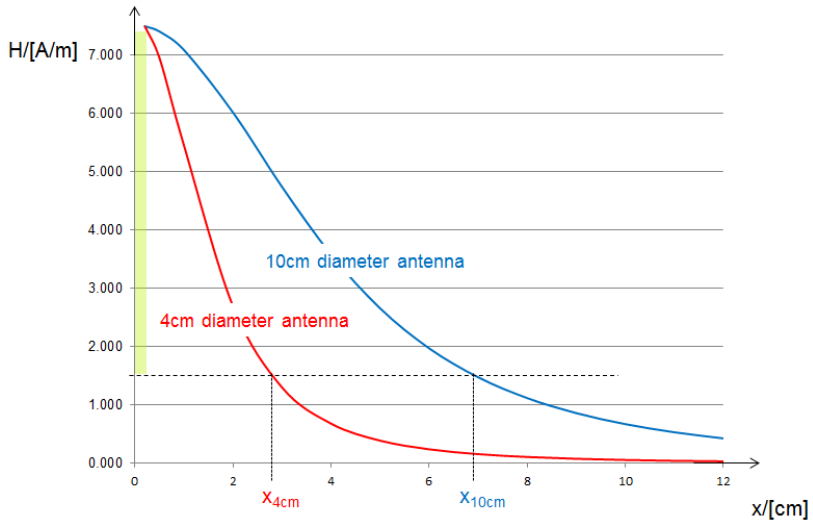
(1) The absolute scale of k might not be correct due to simplifications.

Fig 12. Maximum coupling vs antenna size

Theoretical example:

The Fig 13 shows the field strength versus operating distance of two different antenna sizes. For both antennas, the antenna current is tuned to deliver the maximum allowed field strength of 7.5 A/m at the minimum operating distance of 2 mm.

The small antenna with 4 cm diameter achieves an operating distance of almost 3 cm, the large antenna with 10 cm diameter achieves an operating distance of almost 7 cm.



(1) Minimum required field strength Hmin = 1.5 A/m

(2) Both antennas scaled to deliver Hmax = 7.5 A/m at maximum

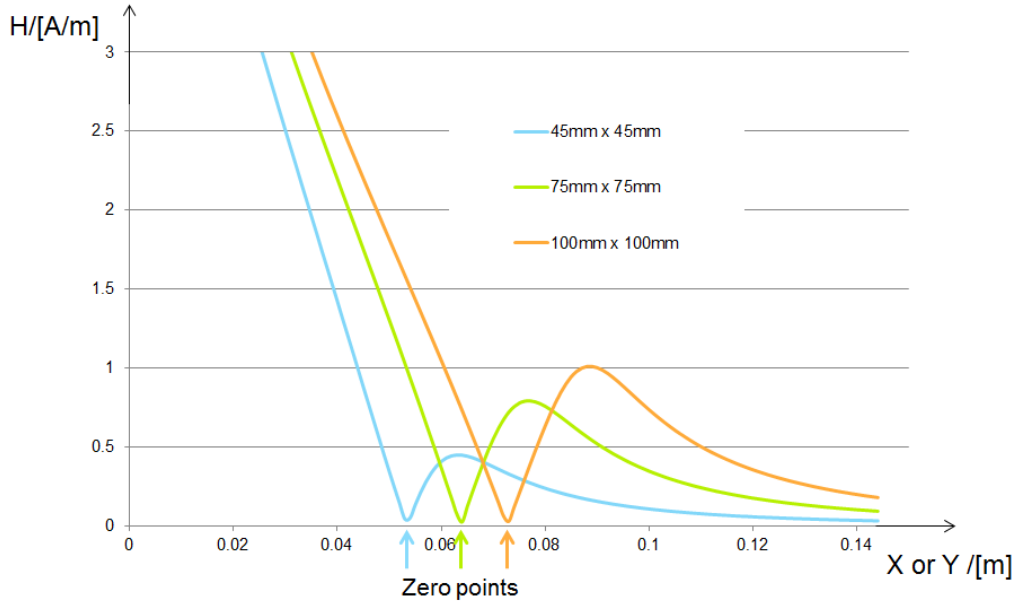
Fig 13. Operating distance x versus antenna size

Note: The large antenna is driven with a current $I_{largeantenna} \approx 4 \times I_{smallantenna}$.

Note: This graph does not include the detuning and loading effect of the reader antenna.

The Fig 14 shows the simulation result of three different square antennas. The magnitude of the field strength is shown versus the distance from the center of the antenna area in either X or Y direction. The curves indicate the zero points, which are areas around the antenna slightly outside the antenna area, where no field can be measured (i.e. where the coupling is zero).

At a zero point no tag device can be operated, even if the required field strength is very low. This needs to be considered, if there is a requirement to read tags within a certain given operating volume, which might touch the zero points, especially if the antenna is too small.



(1) Operating distance = 1cm, X and Y = horizontal distance from antenna center.

(2) These simulation results do neither take any specific environment nor loading effects into account

Fig 14. Magnitude of field strength in 1 cm distance

Note: The field strength is not the same for all three antennas, but has been adjusted individually to achieve the maximum allowed field strength for each antenna.

3.2 Layout recommendations

The connection between the Tx output pins (Tx1 and Tx2) and the EMC low pass filter has to be as short as possible. The GND connection especially between TVSS and the C0 (see Fig 17) capacitors must be as short as possible. The demo board layout is using the middle layer as GND plane, so TVSS and the C0 capacitors are shortly connected to GND. In case of a two-layer design the GND plane should be done properly.

The connection between the block capacitors and the VDD pins need to be as short as possible. This holds especially for the TVDD and its block capacitor.

The CLRC663 evaluation board and its related description can be taken as a reference.

The Fig 15 and Fig 16 show a part of the top and bottom as well as the middle layer structure around the CLRC663 as reference. The GND layer is one of the middle layers to have a proper GND plane.

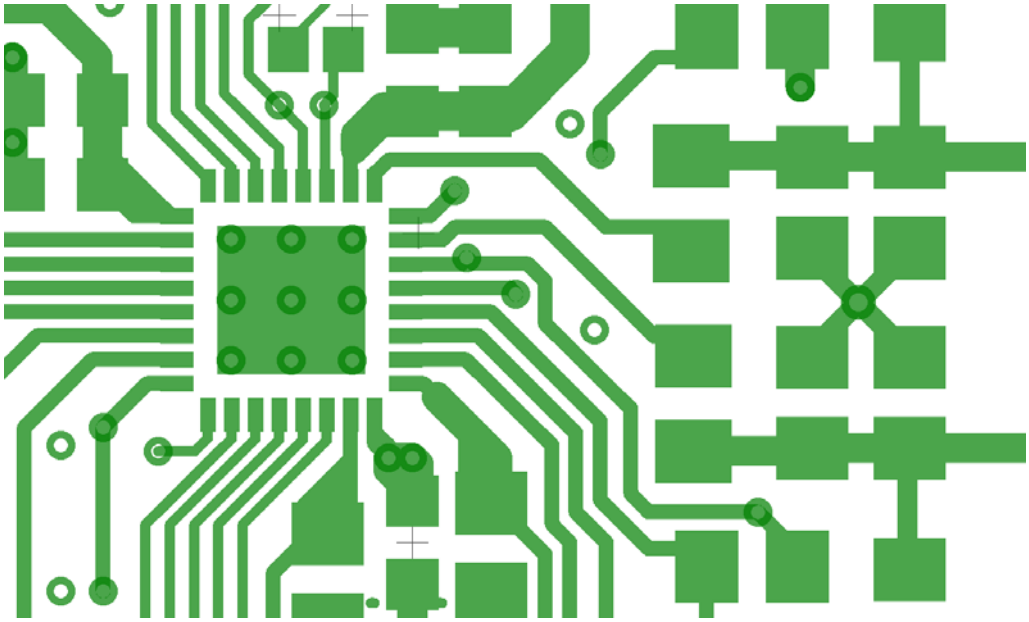
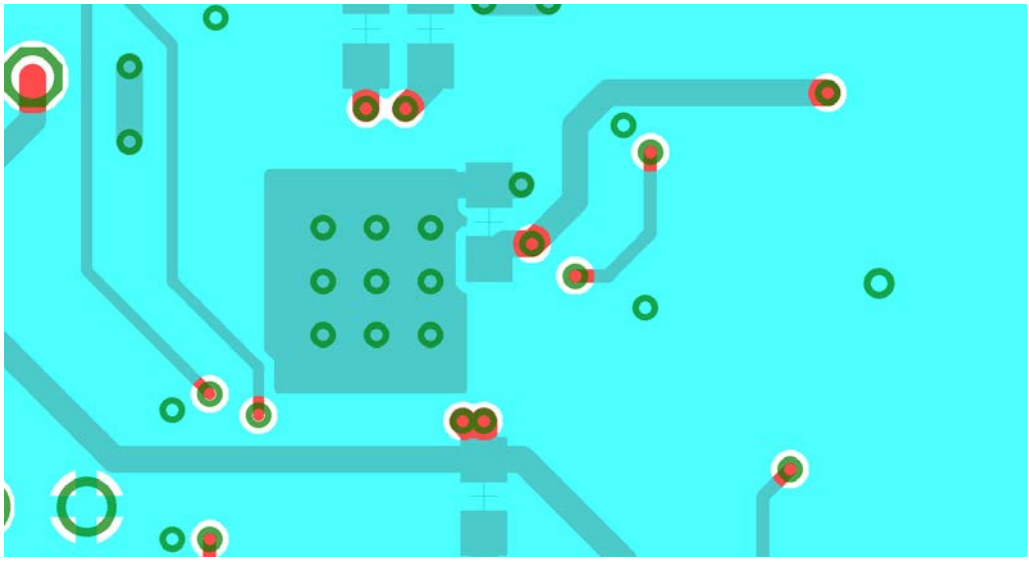


Fig 15. CLRC663 Layout Demo board Top layer



(blue: middle layer GND)

Fig 16. CLRC663 Layout Demo board Bottom and Middle layer

4. CLRC663 hardware design

The CLRC663 is optimized to support the NFC, ISO and EMVCo with a minimum of additional components. The CLRC663 simply requires the antenna matching circuitry, some block capacitors and the crystal.

However, the calculation and tuning of the matching components need to be done carefully to provide the full performance as well as to meet CE and FCC regulations.

The Fig 17 shows a typical analog circuitry using the CLRC663.

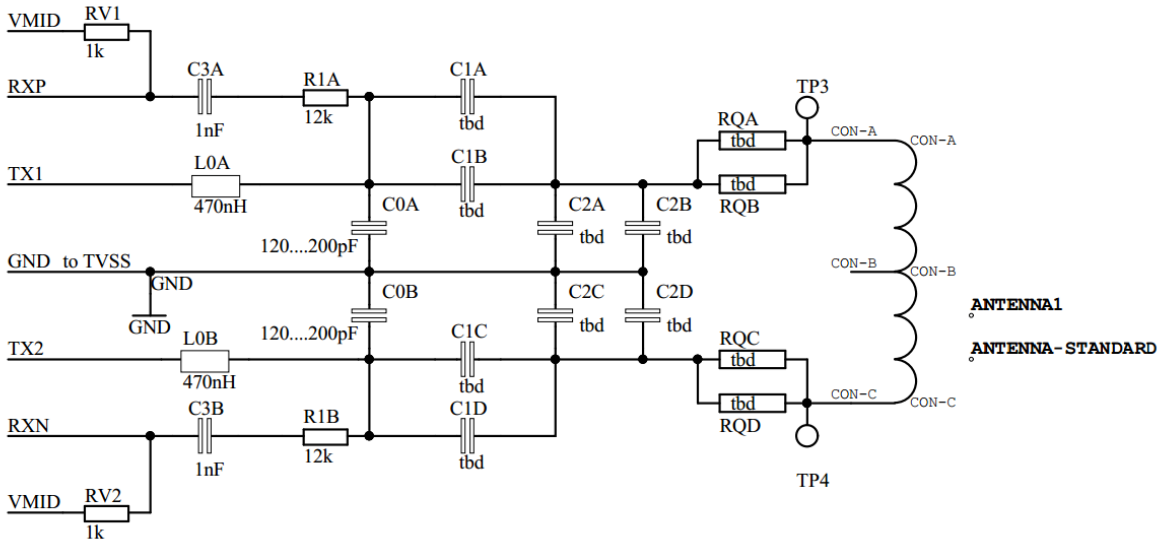


Fig 17. Typical CLRC663 analog circuit

The antenna is typically a part of the PCB design (see section 3.2). All capacitors are typical ceramic capacitors (e.g. X7R). The capacitors used in the matching circuitry are NP0.

The inductor L0x must be capable of driving the required power: In case the maximum output power is needed, the L0x must be able to drive the 300 mA without going into saturation.

Note: Be aware of tolerances! The most critical tolerance in the antenna circuits appears at the antenna coil itself, but even for the matching circuitry tolerances of < ±1% are recommended.

4.1 CLRC663 requirements

The CLRC663 is optimized to support the EMVCo operating volume. Therefore, the Tx output can drive up to I_{TVDD} = 250 mA, the CLRC663 Plus even can drive up to I_{TVDD} = 350mA. Based on a power supply voltage of TVDD = 5 V a power consumption for the total antenna circuit of up to P_{tot} > 1.5 W is possible.

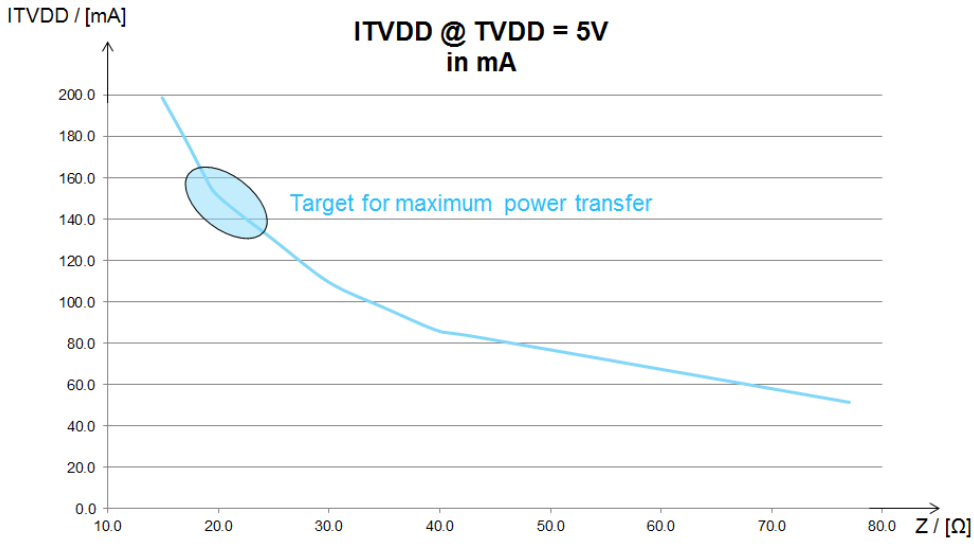
The power supply must be designed properly to be able to deliver a clean supply voltage.

Note: Every noise level on top of the supply voltage can disturb the performance of the CLRC663. Therefore, sometimes higher values of the block capacitors in the range of up to 10 µF might help to improve the performance and also stabilizes the power supply. For that reason, the blocking capacitors for TVDD should be as close as possible to the IC.

4.1.1 Target impedance

The CLRC663 provides an NMOS/NMOS Push-Pull output stage to drive the antenna circuit. The output impedance of each Tx output is approximately 1-3 Ohm, so basically the antenna impedance itself controls the I_{TVDD}, and therefor the field strength.

Fig 18 shows the driver current I_{TVDD} versus the antenna impedance. The target impedance to get a maximum field strength and power transfer should be close to 20 Ω.



(1) Antenna impedance tuned and measured between TX1 and TX2

Fig 18. I_{TVDD} versus antenna impedance

Note: The CLRC663 plus allows an impedance of < 20Ω with the limit of I_{TVDD} = 350 mA.

4.2 Antenna for card reader

The CLRC663 supports only pure reader mode. That means for NFC, only P2P passive initiator is supported.

4.2.1 Antenna matching

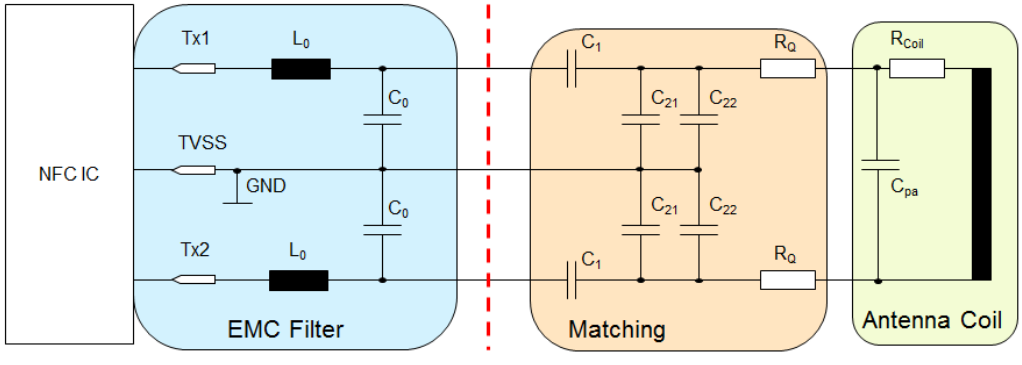
For proper antenna design the antenna impedance must be measured using an impedance analyzer or VNA (vector network analyzer). Such a VNA can be a high end tool from Agilent or Rohde & Schwarz (like the R&S ZVL (see [7], [10]), as normally used in this document), but might be a cheap alternative with less accuracy like e.g. the miniVNA Pro (see[8], [11], [12]). In any case the analyzer needs to be able to measure the impedance in magnitude and phase (vector).

Such VNA can be used to measure the antenna coil as well as the antenna impedance including the matching circuit.

The antenna matching is done with the following steps:

1. Measure the antenna coil
2. Define target impedance and Q-factor
3. Define the EMC filter
4. Calculate the matching components
5. Simulate the matching
6. Assembly and measurement
7. Adaptation of simulation
8. Correction and assembly

The details of those steps are described with an example of the CLRC663 demo board. The blocks and components are used as shown in Fig 19.



(1) This circuit only covers the Tx part.

Fig 19. CLRC663 Reader only antenna matching circuit

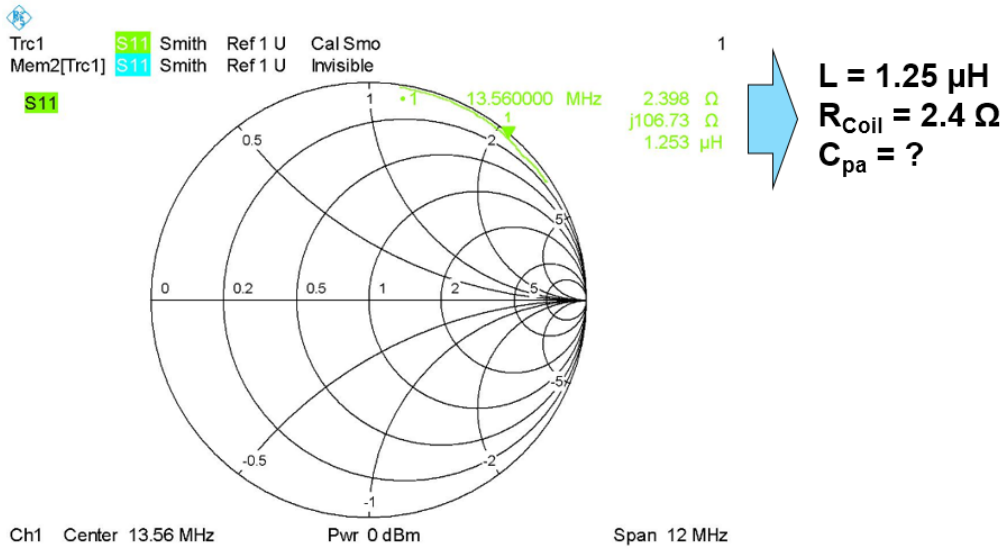
4.2.1.1 Measure the antenna coil

The antenna coil must be designed as described in section 3 and be measured. The measurement is required to derive the inductance L, the resistance R_{Coil} and the capacitance C_{pa} as accurate as possible.

The easiest even though not most accurate way is to use the VNA to measure the impedance $\underline{Z}$ of the antenna coil at 13.56 MHz and to calculate L and R out of it:

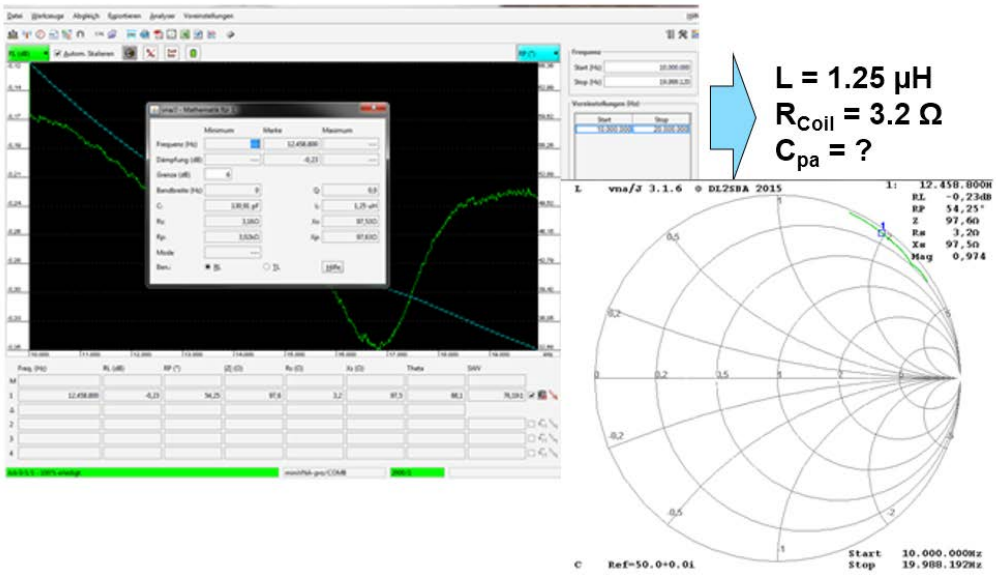
$$\underline{Z} = R + j\omega L_{Coil} \quad (4)$$

Typically, the VNA can directly show the L and R, as shown in Fig 20 and Fig 21.



(1) Measurement with R&S ZVL

Fig 20. Measurement 1: Antenna coil of CLRC663 demo board



(1) Measurement with miniVNA Pro and VNA/J

Fig 21. Measurement 2: Antenna coil of CLRC663 demo board

In this example the antenna coil is measured with these values:

L = 1.25 µH

R_{Coil} = 2.4 - 3.2 Ω

C_{pa} = not measured, can be estimated

The inductance can be measured quite accurate, but the resistance is not very accurate due to the relationship between R and jωL. And the capacitance is not measured at all with this simple measurement.

There are several ways to improve the accuracy and even further derive the capacitance, but these simple results are enough to start the tuning procedure. This tuning procedure needs to be done anyway, so there is no real need to spend more effort in measuring the antenna coil parameters more accurate.

4.2.1.2 Define target impedance and Q-factor

The target impedance must be defined. For the maximum power transfer, it should be 20 Ω (as indicated in section 4.1.1). In such case the driver current I_{TVDD} gets close to the maximum allowed limit of $I_{TVDDmax}$ = 250 mA.

For the CLRC663 Plus the target impedance might go down to 15Ω to increase the driver current. In such case the driver current I_{TVDD} gets close to the maximum allowed limit of $I_{TVDDmax}$ = 350 mA under loading conditions.

The impedance target might be different for different applications. An impedance target of R_{match} = 50…80 Ω might be better in battery powered devices, where the current consumption must be minimum, while at the same time the required maximum operating distance can be lower.

Note: The following examples show the design for a maximum power transfer, e.g. for an EMVCo POS design.

The quality factor Q depends on the overall system requirements and frame conditions. The overall system requires the Q to be in a range, which allows us to meet the timing and pulse shape requirements of the corresponding standard (ISO, NFC or EMV). These requirements are mainly the same, but with some differences:

While ISO allows data rates of up 848 kbit/s, NFC allows the data rates of up to 424 kbit/s. EMV systems are limited to 106 kbit/s. So typically, the Q of EMV reader systems can be higher than the Q of ISO or NFC reader systems.

The Q is an indirect value, since the measurement of the Q in the overall antenna system, which includes the antenna driver as well as the contactless card, is complex – and not required. The wave shape and timing measurements, as required according to the standards, are the relevant measurements, and the corresponding Q value is not of any importance.

Here in a first step the Q is chosen for the passive and linear antenna circuit only. So, it can be seen as start value to calculate the damping resistors R_Q.

Good starting values as entry for the calculation of the matching calculation are shown in Table 1.

Table 1. Q-factor

Values for the passive linear antenna circuit only.

Q	Condition
10	Start value for the matching calculation for NFC Reader design, supporting higher bit rates (212, 424, 848 kbit/s).
15	Start value for the matching calculation for NFC Reader design, supporting higher bit rates (212, 424 kbit/s).
20	Start value for the matching calculation for typical NFC Reader design.
25	Start value for the matching calculation for typical NFC Reader design, limited to 106 kbit/s.
30	Nominal value for MIFARE Classic communication.

Note: The lower the Q, the better the stability and robustness of the antenna is. Antennas with lower Q show less detuning. The higher the Q, the higher the field strength is.

Note: The final Q must be tuned with the pulse shape measurements, if the antenna shall be fully optimized.

Note: It might be helpful to slightly adapt the Q in the given Excel sheet calculation [13] in such a way that the resulting damping resistor R_Q is calculated to be within an E-series of values (i.e. 2.7 Ω or 3.3 Ω, but not 2.845 Ω). In such case the following calculation is more accurate, i.e. the calculation result gets closer to the measured result.

4.2.1.3 Define the EMC filter

The EMC filter can be a second order low pass filter as shown in Fig 17, and contains an inductor (L0) and a capacitor (C0). The cut off frequency defines the overall detuning behavior as well as the transfer function of the antenna circuit.

The inductor L0 needs to be capable to drive the full power into the antenna without going into saturation. The Q-factor of this inductor should be as high as possible.

Typically, the inductance is in range of:

L0 = 330 nH … 560 nH

The cut off frequency typically should be far above the carrier frequency but far below the second harmonic:

F_{Cutoff} = 14.5 MHz … 22 MHz

Based on this the following EMC filter values are chosen:

L0 = L0A = L0B = 470 nH

C0 = C0A = C0B = 56 pF + 68 pF[1]

F_{Cutoff} = 20.9 MHz

Note: The chosen values of the inductance, the cut off frequency and the corresponding capacitance have shown to be a reasonable trade-off between the transfer function for the transmit signal as well as for the receive signal on one hand and the filter function to suppress the higher harmonics on the other hand.

4.2.1.4 Calculate the matching components

The next step is to calculate the values of the matching circuit. The input for the Excel sheet as shown in Fig 22 needs to be:

“Measured” values:

La = L = 1253 nH (measured antenna coil inductance)

Ca = C_{pa} = 0.1 pF (estimated parallel capacitance of the antenna coil)

Ra = R_{Coil} = 2.7Ω (measured antenna coil resistance)

Preset values:

Q = 10 (defined Q-factor, see section 4.2.1.2)

Rmatch = 25 Ω (defined target impedance, see section 4.2.1.2)

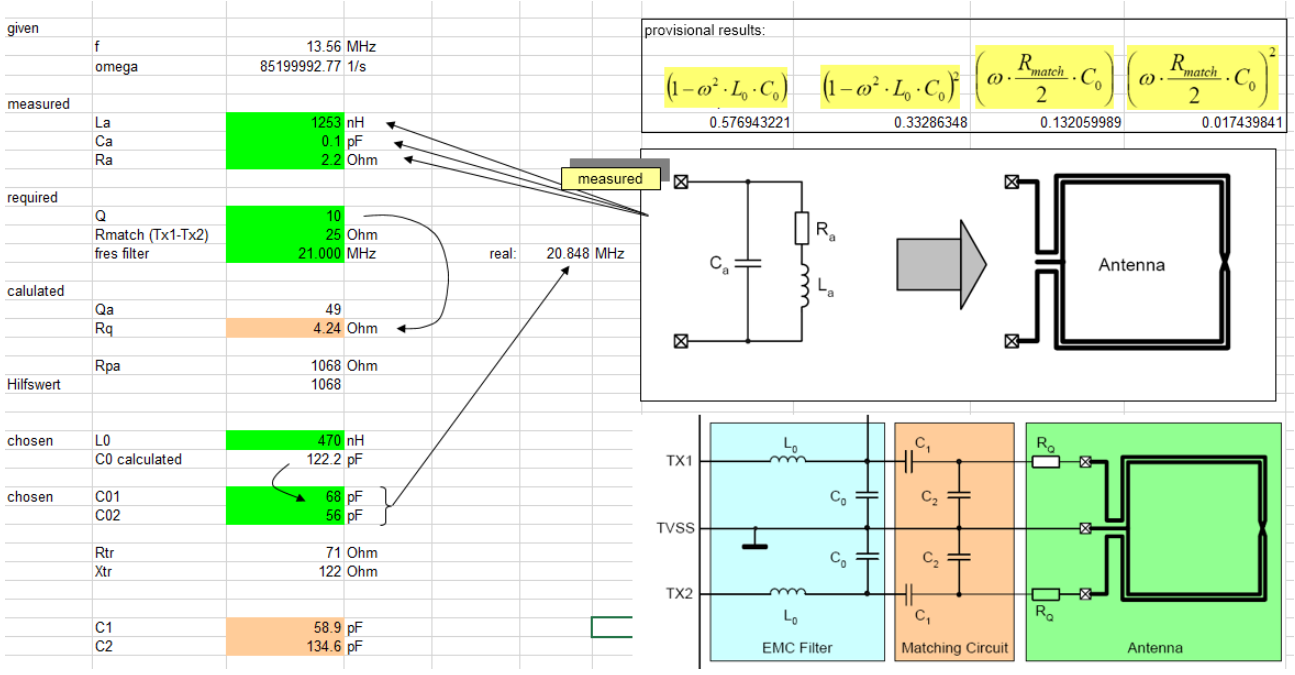
L0 = L0A = L0B = 470 nH (EMC filter inductance, see section 4.2.1.3)

C0 = C0A = C0B = 56 pF + 68 pF (EMC filter capacitance, see section 4.2.1.3)

Calculated Values (see Fig 22):

Rq = R_Q = 4.24 Ω

1. [1] Two capacitors are chosen, because they are already assembled on the evaluation board. A single capacitor of 120 pF can be taken alternatively. The matching calculation should be done with the real value.



(1) Excel sheet, see [13]

Fig 22. Antenna matching calculation

The matching capacitors are calculated:

C1 = (C1A + C1B) = (C1C + C1D) = 58.9 pF → 47 pF + 12 pF (0.1 pF more)

C2 = (C2A + C2B) = (C2C + C2D) = 134.6 pF → 100 pF + 33 pF + 1.5 pF (0.1 pF less)

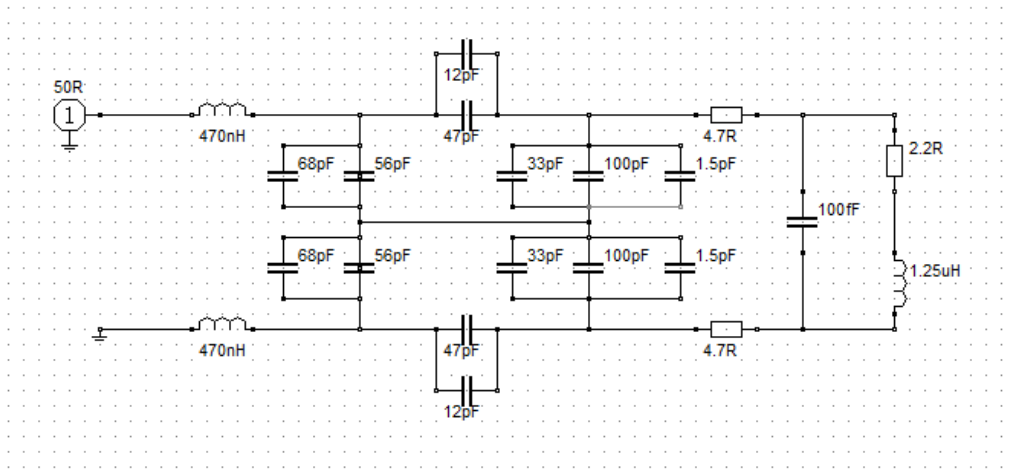
4.2.1.5 Simulate the matching

The measurement of the antenna coil itself typically is not very accurate. Therefore a (fine) tuning of the antenna normally is required, which might become easier in combination together with a simulation.

A simple matching simulation tool like e.g. RFSIM99 (refer to [8]) can be used to support the antenna tuning. This is just an example; other simulation tools can be used as well. The simulation input and the result based on the above given start values for the antenna matching is shown in Fig 23 and Fig 24.

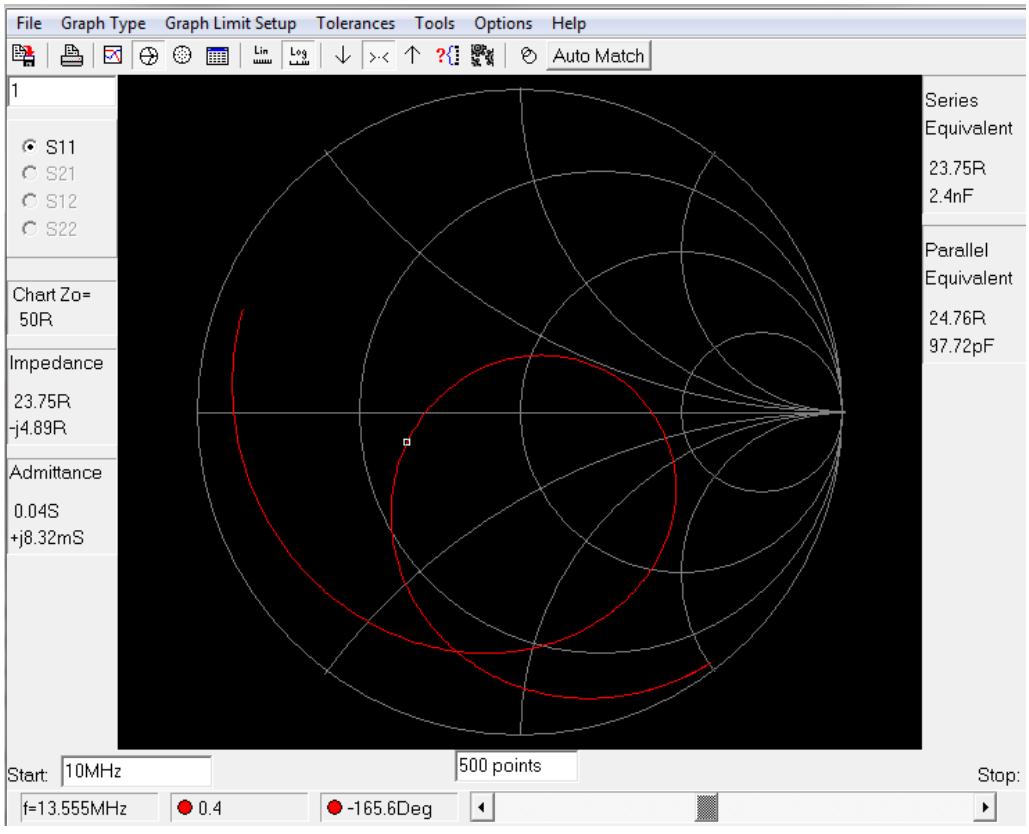
With these values the assembly can be done, even though the result is not yet optimum, as shown in Fig 24. The overall impedance is slightly below 25 Ω and capacitive (-j4 Ω).

Note: The result is not as calculated, since not the exact calculated values of the capacitors are taken for assembly.



(1) The “measurement GND” is not the CLRC663 and evaluation board GND!

Fig 23. RFSIM99 Schematic

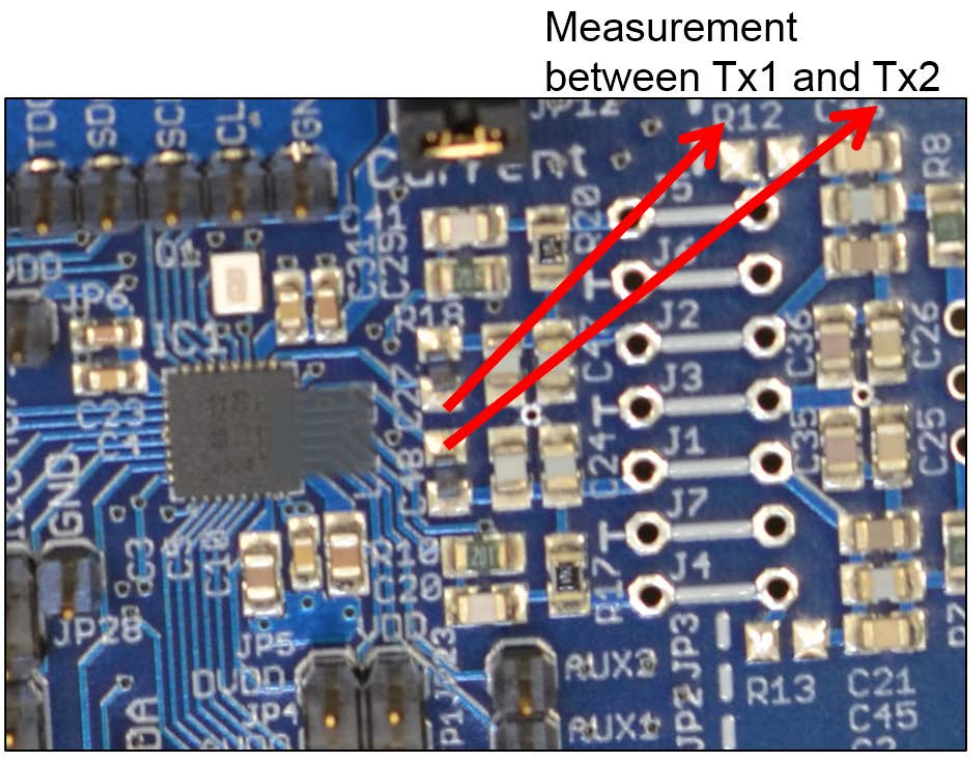


(1) Simulation based on the first calculated start values.

Fig 24. RFSIM99 Simulation result

4.2.1.6 Assembly and measurement

After the first assembly, the impedance measurement must be done, as shown in an example in Fig 25.

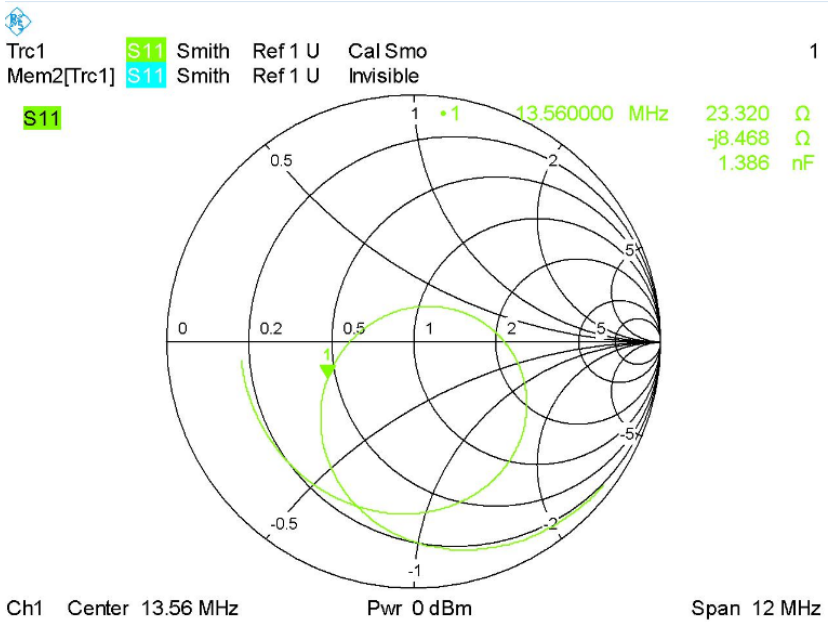


(1) A simple connector is soldered between TX1 and TX2 to simplify the impedance measurement.

Fig 25. Impedance measurement example

The measurement result is shown in Fig 26. The circuit does not meet the requirements, i.e. it needs to be re-tuned.

The measurement result is typically slightly different than the simulation result, since the accuracy of the original antenna coil measurement is limited.



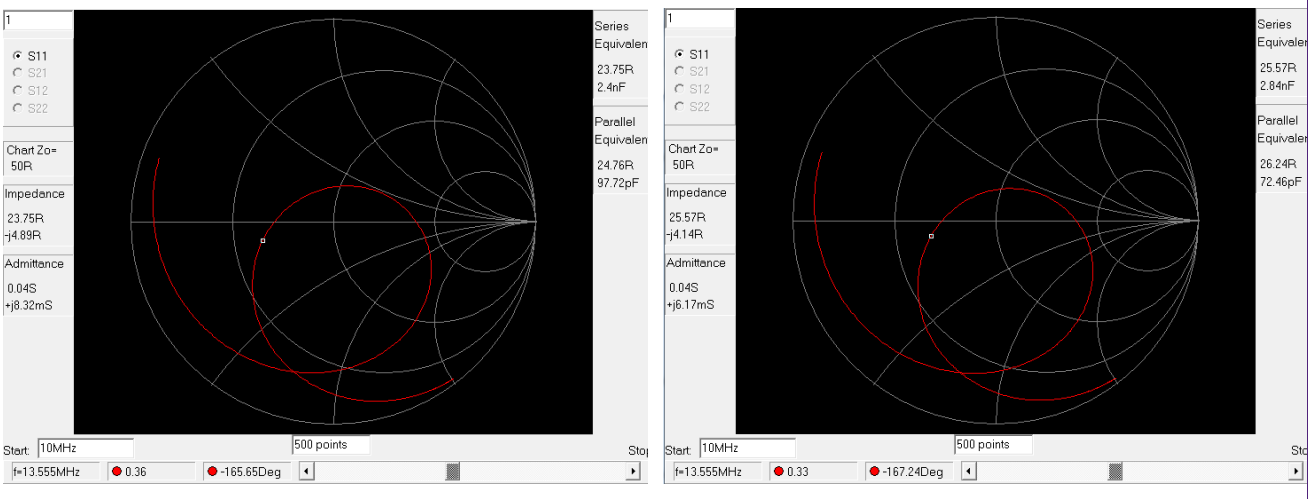
(1) This matching does not meet the requirements. It must be corrected and retuned.

Fig 26. Measurement result of first assembly

4.2.1.7 Impedance adaptation in simulation

The easiest and fastest way to (fine) tune the antenna is to first of all adapt the simulation in such a way that it shows the same result as the reality. The parameters of the antenna coil are the parameters to be changed, since these parameters are not measured (or estimated) correctly.

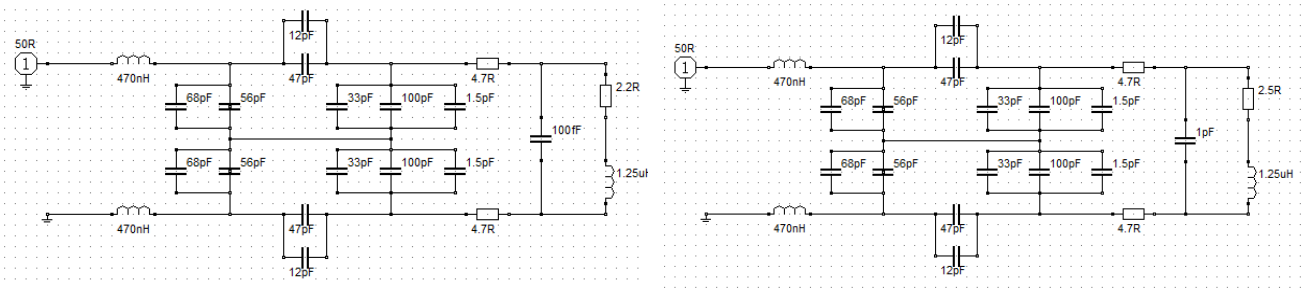
So with the values of L, C_{pa}, and R_{Coil} the simulation is tuned from Fig 27a to Fig 27b. The changed values can be seen in Fig 28b.



a. Impedance first step

b. Impedance after adaptation

Fig 27. Impedance adaptation in the simulation (result)



a. Circuit first step

b. Circuit after adaptation

Fig 28. Impedance adaptation in the simulation (circuit)

With these adapted values of the antenna coil the last step of the final tuning can be done:

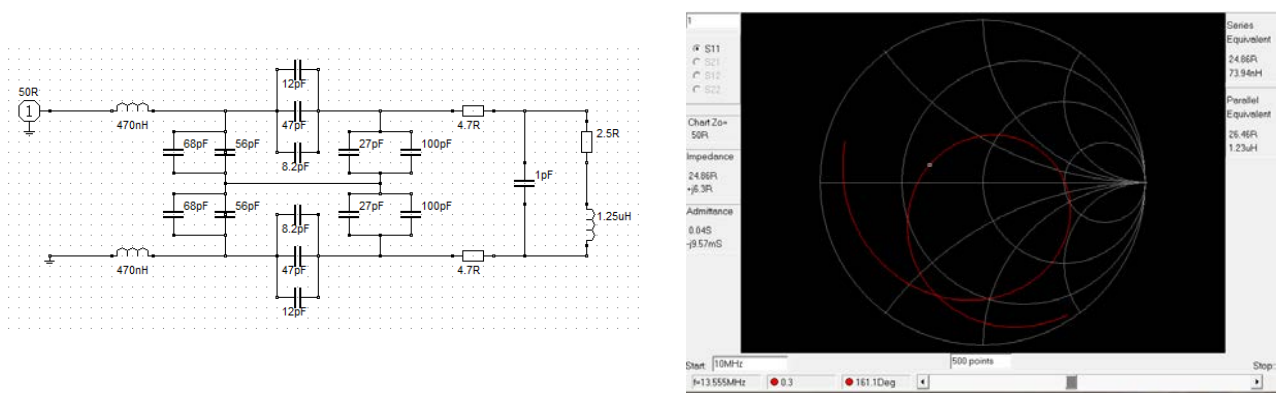
La = L = 1253 nH

Ca = C_{pa} = 1 pF

Ra = R_{Coil} = 2.5 Ω

4.2.1.8 Impedance correction and assembly

The tuning of the impedance is now corrected with the values of C1 and C2, as shown in Fig 29.

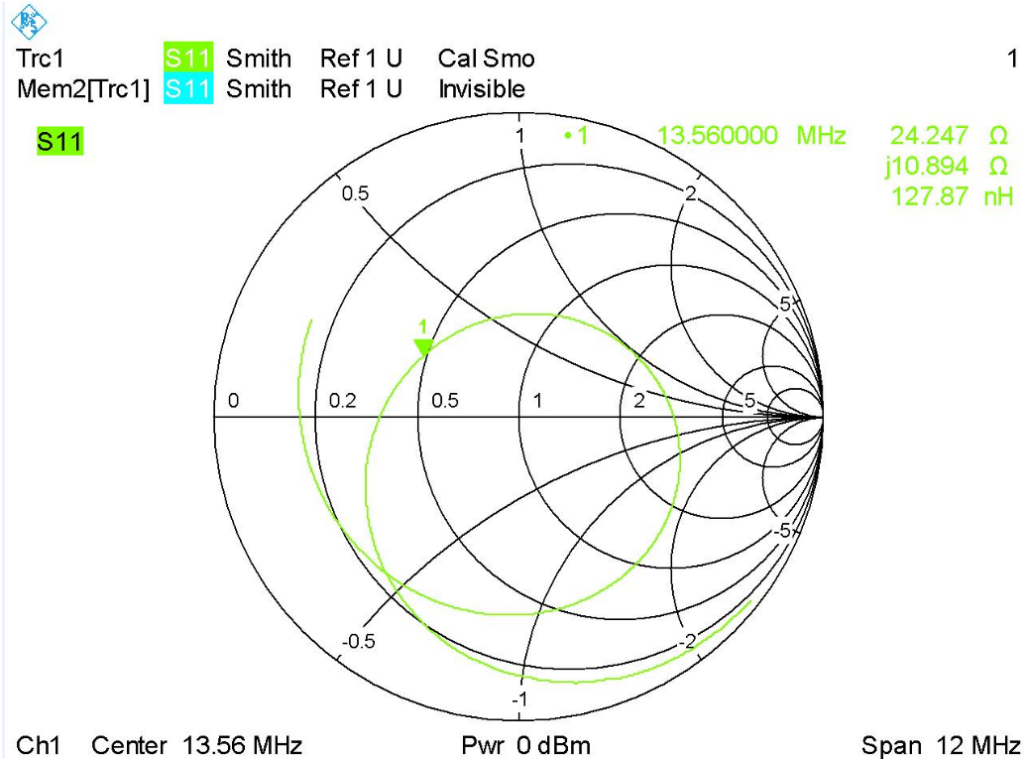


a. Final simulation circuit

b. Final Simulation result

Fig 29. Final tuning simulation

These values are assembled, and the impedance is measured. The result is shown in Fig 30.



(1) This impedance is measured unloaded.

Fig 30. Final tuning measurement result

4.2.2 Loading effect

The target impedance of the antenna design defines the I_{TVDD} (driver current of the CLRC663) and the output power (i.e. operating distance for a given antenna coil) as shown in section 3.

The lower the impedance gets, the higher the I_{TVDD} becomes. Especially for high power reader design, where the impedance is quite low to achieve a maximum of field strength (as e.g. shown in Fig 6), the I_{TVDD} might get close to its limit. In worst case loading conditions, the I_{TVDD} might even exceed the specification limits and therefor reduce the life time of the CLRC663.

So, in any case it is strongly recommended to check the loading and detuning of the antenna.

The first step is to check two typical and extreme use cases:

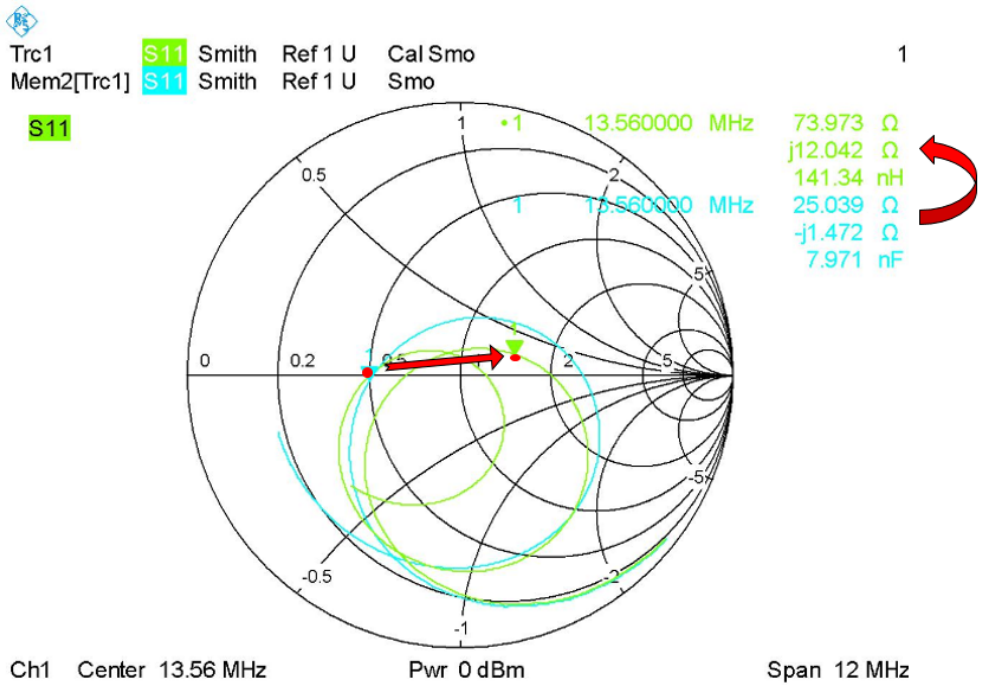
1. Loading with reference PICCs
2. Loading with a metal plate

Both cases must be tested under real operating conditions to ensure the I_{TVDD} limit (“active” loading, see 4.2.2.3), but it is very helpful to check the “passive” loading and understand its behavior.

4.2.2.1 “Passive” loading with reference PICCs

The loading with reference PICCs being calibrated for the Hmin test show a kind of worst case loading with typical PICCs, since this is the purpose of calibrated reference PICCs.

Fig 31 shows the unloaded impedance curve (blue) as well as the loaded curve (green), when the antenna is loaded with a reference PICC. In this case the reference PICC is placed closely to the antenna to achieve the maximum possible coupling between PCD and PICC.



(1) $I_{TVDDloaded} < I_{TVDDunloaded}$

Fig 31. Antenna impedance example with reference PICC loading

The change of the impedance curve indicates a lower I_{TVDD} under loading conditions. That implies that with the above shown antenna matching the loading with reference PICCs (or typical smart cards) does even decrease the field strength and I_{TVDD}. This even sometimes helps to meet the maximum EMVCo limits for power transfer, especially with small antennas.

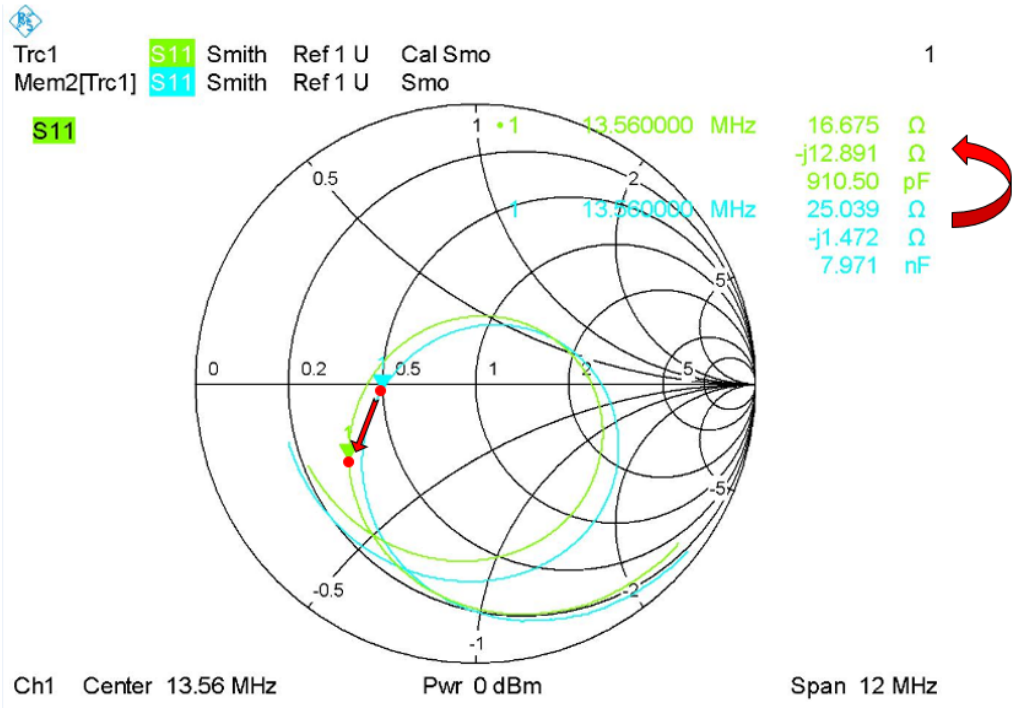
This loading must be cross checked under normal operating conditions (see 4.2.2.3).

Note: The loading with the reference PICC typically turns the impedance circle in the smith chart clockwise. At the same time the overall Q-factor drops, so the circle gets smaller. Due to the tuning of the antenna, the impedance almost stays resistive, but moves towards a higher impedance. A new resonance (small loop) at a frequency above 13.56 MHz can be seen: this is related to the resonance frequency of the reference PICC itself.

4.2.2.2 “Passive” loading with metal

The other most critical case typically is the loading with some large metal plate. Such metal plate e.g. might even be an NFC tablet or a large NFC phone.

Fig 32 shows the unloaded impedance curve (blue) as well as the impedance curve, when a large smart phone loads the antenna (green), where the battery acts as a magnetic short cut. In this example, the worst-case loading effect occurs in almost 2 cm distance.



(1) $I_{TVDDloaded} > I_{TVDDunloaded}$

Fig 32. Antenna impedance example with smart phone loading

As can be seen, in this case of metal loading the I_{TVDD} must increase, since the overall impedance gets lower:

$$Z_{unloaded} = \left|\underline{Z}\right| \approx 25\Omega$$

$$Z_{loaded} = \left|\underline{Z}\right| \approx \sqrt{16.7^2 + 12.9^2} = 21.1\Omega$$

This behavior needs to be checked carefully, directly measuring the I_{TVDD}.

4.2.2.3 “Active” loading

The impedance measurement as shown above is always done with limited power (typically 0 dBm), so especially the reference PICC shows a slightly different behavior than in the real test case. Therefore the “passive” loading measurement can only show the trend of loading and detuning, but does not allow a 1:1 calculation of the related I_{TVDD} out of the impedance.

So finally, the loading must be tested under real operating conditions, i.e. the CLRC663 must be powered and the carrier must be enabled. Then the I_{TVDD} must be measured under the different loading conditions (see above). In no case the I_{TVDD} is allowed to exceed the specification limit.

4.3 Optimizing the transmitting

In a typical PCD design the output stage of the CLRC663 is used with the maximum available output power, and the overall power consumption (and field distribution) is limited with the antenna impedance.

The standard modulation of the Tx signal is either a 100% AM for type A or a 10% AM for type B. The modulation index for type B must be adjusted due to the antenna tuning with the set_residual_carrier in the TxAmp register.

On top it might be helpful to adapt the rise and fall times of the Tx envelop signal to match the pulse shapes to the timing requirements of the according standard (NFC, ISO or EMVCo).

The optimum register settings might be different from the default values stored in the EEPROM. So, for the optimization and testing typically the registers can be tuned and changed directly. As soon as the optimum settings are derived, the new settings might be changed and stored in the user area of the EEPROM. For writing data in the EEPROM either the WriteE2 command (08h) or WriteE2Page command (09h) can be used.

For storing the register values in to the EEPROM, page 3 to 95 (address 00C0h to 17FFh) are free for customer use.

For loading a set of registers the LoadReg command (0Ch) can be used. In the final application simply the standard LoadReg command can be used with the optimized settings.

Example: (using PCSerial with the commands WriteE2Page and LoadReg)

```
//> Terminate any running command. Flush_FiFo
  SR 00 00
  SR 02 b0
//> Flush Fifo. Read Error Reg
  SR 02 B0
  GR 0A
// -------------------- WriteE2Page command -------------------------
SR 05 03            // write page number into FIFO
//> 64 bytes to 0 to 63
SR 05 57            // example values for Register Values to be stored ibn EEPROM
SR 05 71            // example values for Register Values to be stored ibn EEPROM
SR 05 51
```

```
SR 05 00
SR 05 00
...
SR 05 00            // 64 bytes are written into EEPROM

//> Terminate any running command. Flush_FiFo
SR 00 00
SR 02 B0
//>------- Load Register (loading 3 registers)
SR 05 00            // EEPROM addressL
SR 05 C0            // EEPROM addressH
SR 05 29            // Address of the Register to star with loading
SR 05 03            // Number of registers that should be loaded
SR 00 0C            // LoadReg command
// ---------------END-----------------------
```

In this example a whole EEPROM page is written so in the final application all needed registers settings can be stored on the chip and can be loaded by using LoadReg. In the example the LoadReg is setting the Register 29h, 2Ah and 2Bh. So, in total 3 registers are loaded, that can be extended up to the whole register area.

The default settings in the EEPROM are optimized for the CLRC663 based on the evaluation board antenna. Some of these settings might be adjusted and optimized for other antenna designs.

The major parameters for the Tx are:

1. Modulation pulse width (normally not required to be changed)
2. Modulation index (for type B)
3. TxClkMode (for type A, if needed)
4. Tx Shaping (rise and fall time, if needed)

4.3.1 Modulation pulse width type A

The modulation pulse width is adjusted with the TxDataModWidth register (address 2Fh) (DModWidth). Typical values are:

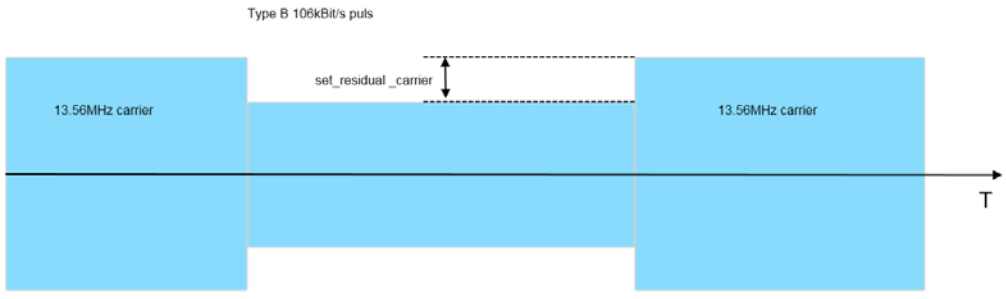
- 106 kBit/s: 27h
- 212 kBit/s: 10h
- 424 kBit/s: 8h
- 848 kBit/s: 2h

Normally no optimization is needed.

4.3.2 Type B Modulation index

For type B the modulation index needs to be checked and maybe adjusted, since the final optimum setting depends on the antenna design. The LoadProtocol provides the correct settings, which are required for type B, but the modulation index must be set with set_residual_carrier (TxAmp register (address 29h)), as described in detail in [1].

The modulation index for type B modulation can be set as shown in Fig 33. With set_residual_carrier the modulation index is set in such a way that with increasing the value the modulation index also increases.

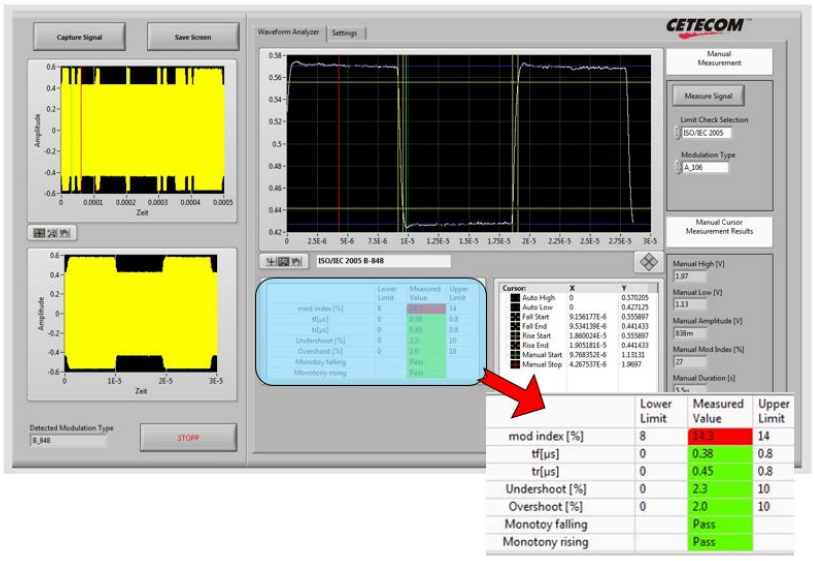


(1) set_residual_carrier

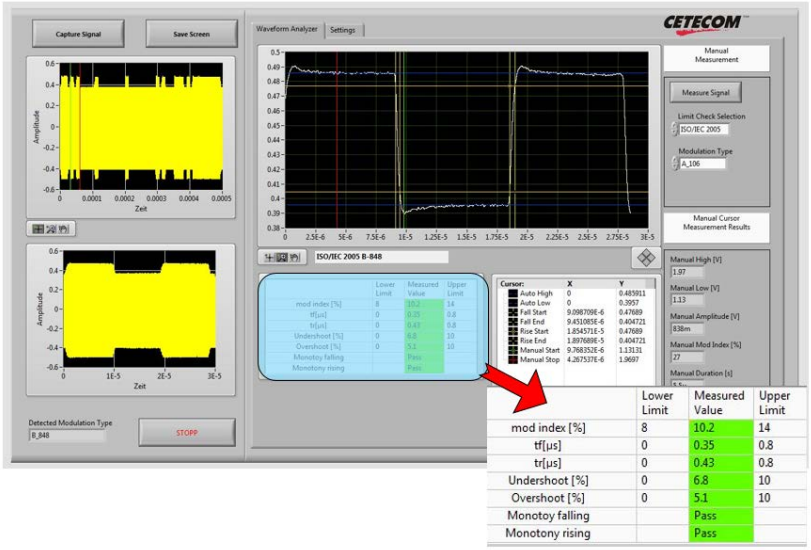
Fig 33. Type B modulation index

Fig 34 shows an example that starts with a value F3h for set_residual_carrier and 0Ah for tx_set_iLoad. The corresponding modulation index is 14.3. This value exceeds the ISO limit of 14 for the modulation index. That means the index must be reduced by decreasing the set_residual_carrier value step by step until the targeted modulation index is reached. In this example target is an index of around 10 so the value for set_residual_carrier is decreased until a value of CDh. In this case tx_set_iload is fixed to 0Ah. With the Value CDh the modulation index decreased to 10.2 so close to the target value.

After adjusting the modulation index the variation of the index needs to be checked. This is done under load conditions, which means a reference PICC should be placed in maximum distance (maximum distance is set by the minimum field strength according the chosen standard). The modulation index is typical adjusted in this position, so to check if the value is correct for all position the distance between reader and PICC needs to be reduced step by step. The most critical positions are maximum distance and minimum distance. If all positions are within the limits the index is adjusted and can be used.



(1)



(2)

(1) set_residual_carrier = F3h , tx_set_iLoad = 0Ah

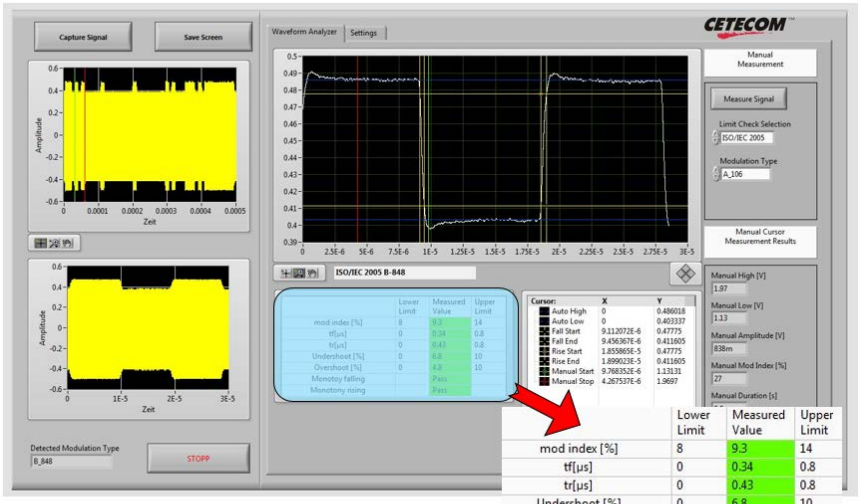
(2) set_residual_carrier = CDh , tx_set_iLoad = 0Ah

Fig 34. set_residual_carrier example

In the case there is no value that fits for all positions, it is possible to fine tune the modulation index by using the tx_set_iLoad. By increasing this value, the modulation index will decrease. In Fig 35 an example is given to the effect of changing the tx_set_iLoad. By changing the value from 0Ah to 0Fh the modulation index decreases from 10.2 to 9.3. This change is dependent to the matching that is used. So, the difference in the modulation index between the values of tx_set_iLoad will vary with different matching's.

	Lower Limit	Measured Value	Upper Limit
mod index [%]	8	10.2	14
tf[µs]	0	0.35	0.8
tr[µs]	0	0.43	0.8
Undershoot [%]	0	6.8	10
Overshoot [%]	0	5.1	10
Monotoy falling		Pass	
Monotony rising		Pass	

(1)



	Lower Limit	Measured Value	Upper Limit
mod index [%]	8	9.3	14
tf[µs]	0	0.34	0.8
tr[µs]	0	0.43	0.8
Undershoot [%]	0	6.8	10
Overshoot [%]	0	4.8	10
Monotoy falling		Pass	
Monotony rising		Pass	

(2)

(1) set_residual_carrier = CDh , tx_set_iLoad = 0Ah

(2) set_residual_carrier = CDh , tx_set_iLoad = 0Fh

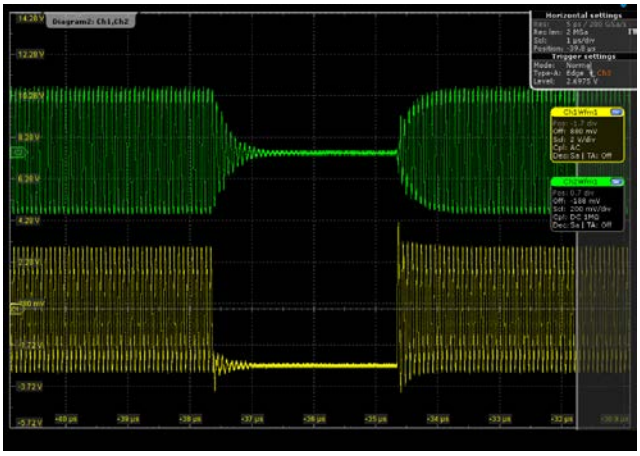
Fig 35. Tx_set_iLoad

4.3.3 Tx envelope shape

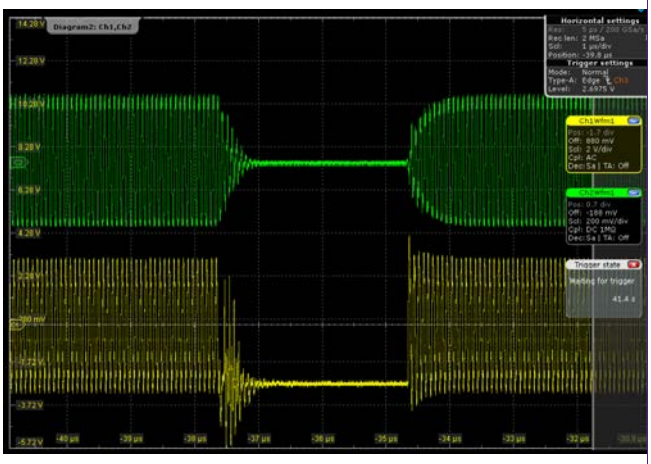
The CLRC663 provides some registers to adjust the wave shapes. The following description is based on the default settings from the LoadProtocol of the corresponding protocol (type A or type B).

4.3.3.1 TxClkMode

For type A the 100% ASK is enabled, so basically no residual carrier needs to be adjusted. However, the DrvMode register (address 28h) Bit 0-2 (TxClkMode) allows to change the Tx output stage behavior during the modulation pulses. The Fig 35 shows an example with the default setting (001b output pulled to 0 in any case) as well as the setting, where the Tx output stages are open drain (101b), and only the low side MOS (pull) are actively driven. The green signal shows the field, picked up with the reference PICC in a few cm distances. The yellow signal shows the Tx output using a standard probe with a standard GND cable. These signals just indicate the difference between different register settings in principle.



a. TxClkMode = 001bin (Default)



b. TxClkMode = 101bin (low side pull)

Fig 36. TxClkMode

4.3.3.2 Tx overshoot protection

The CLRC663 provides an overshoot protection for 100% ASK to avoid overshoots during a PCD communication. Therefore, two timers, overshootT1 and overshootT2, can be used.

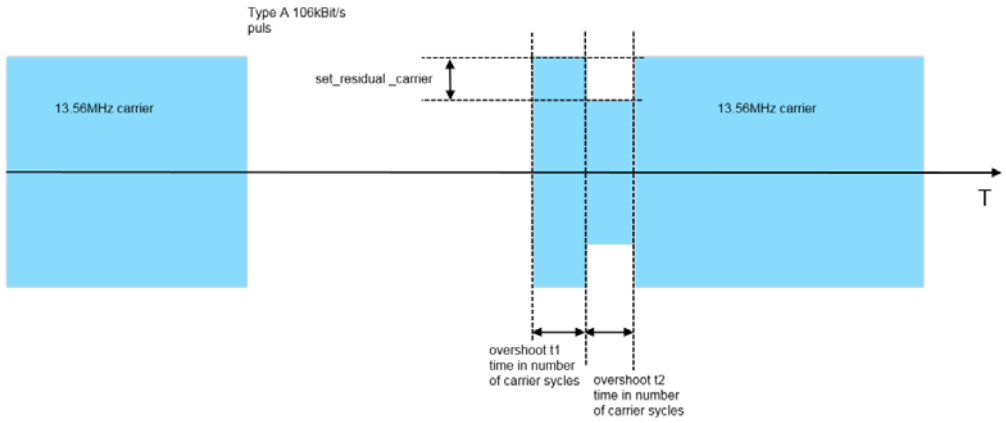
During the timer overshootT1 runs, the main amplitude defined by set_cw_amplitude is provided to the output driver. Followed by an amplitude denoted by set_residual_carrier with the duration of overshootT2.

Note: If CwMax in TxCon register (address 2Ah) is set to 1 set_cw_amplitude is overwritten and the Tx output is pulled to maximum voltage.

In Fig 37 the parameter and influence on the pulse is shown. For using the overshoot protection there are 3 values that need to be adopted. These values are

1. OvershootT1 in Txl register (address 2Bh)
2. OvershootT2 in TxCon register (address 2Ah)
3. set_residual_carrier in TxAmp register (address 29h)

Note: The tx_set_iLoad (Txl register) is setting the value range for the set_residual_carrier and it should always be >1. This value influences the amplitude for the time of overshootT2 and the maximum Amplitude difference between 1h and Fh is around 8% of the carrier amplitude. That means if only tx_set_iLoad is changed from 1h to Fh the remaining carrier for T2 time is rising by 8% (around 210 mV). So, the default Value (6h) can typically be used and does not need to be further adopted.



(1) Type A 106kBit/s pulse showing the parameters of the overshoot protection

Fig 37. Principle and parameter overview of the overshoot protection

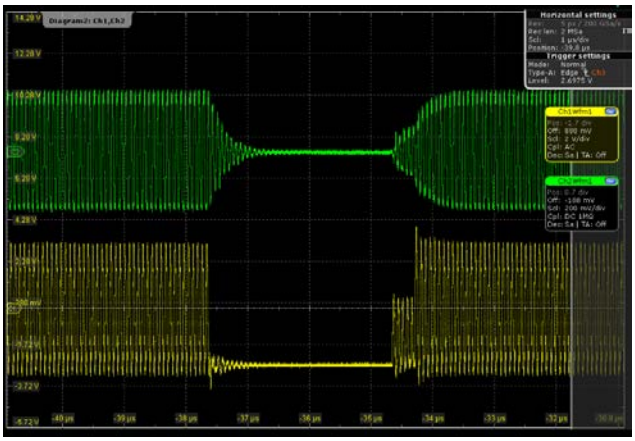
For optimizing the rising edge, in case of overshoots, of a type A 106 kBit/s:

First step: Start with only OvershootT2 (T2). That means define a length in carrier cycles (typical 5) and decrease the amplitude by increasing the set_residual_carrier (see Fig 38 first picture). If this does not improve the shaping then increase or decrease the T2 time and repeat the first step.

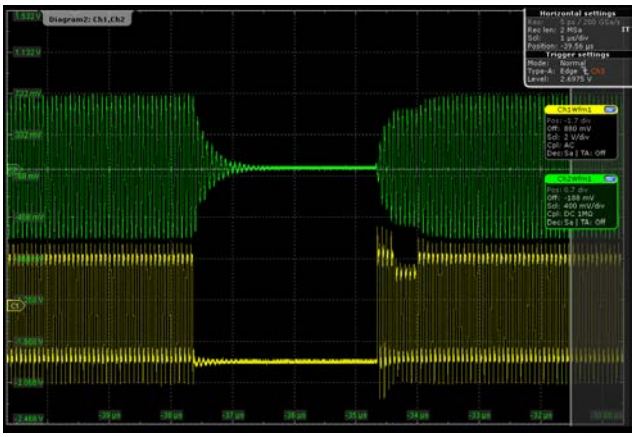
Second step: In case there is no value combination that improves significantly the pulse shape, OvershootT1 (T1) needs to be set. In this case increase T1 time for the optimized setting (outcome of the first step). In Fig 38, second picture, 4 clock cycles for T1 have been added so the pulse shaping becomes smoother on the rising edge.

Depending on the overshoot the values need to be adopted for the target hardware and in worst case position of the ref. PICC, where the overshoot is maximum.

The length and the amplitude that typically improves the rising edge in case there is no combination of OvershootT2 and set_residual_carrier.



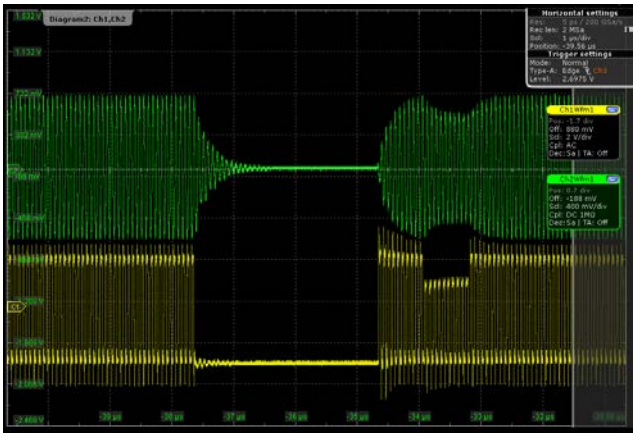
a. OvershootT2 = 5h, set_residual_carrier = 1Ah, OvershootT1 = 0h
b. Green: Field probe
c. Yellow: Tx1 signal



a. OvershootT2 = 5h, set_residual_carrier = 07h, OvershootT1 = 4h
b. Green: Field probe
c. Yellow: Tx1 signal

Fig 38. Example of Tx overshoot protection (100% ASK envelope)

Note: Check the final register settings and consider that a wrong setting can worsen the pulse shape (see Fig 39).



a. OvershootT2 = Ah, set_residual_carrier = Fh, OvershootT1 = Ah
b. Green: Field probe
c. Yellow: Tx1 signal

Fig 39. Bad settings for Tx Overshoot protection

4.4 Optimizing the receiving

Fig 40 shows the high-level principle of the Rx blocks for one Rx path. The major register for the Rx are:

1. Rcv (the registers related to the receiver setting),
2. RxAna (sets gain and the high pass corner frequency (HPCF)), and
3. RxThreshold (MinLevel and MinLevelP).

The rcv_gain adjusts the analog gain of the demodulated subcarrier in the I and Q channel. The HPCF limits the bandwidth of the (modulated) sub carrier signal.

For the optimization of the Rx circuit it is recommended to use the debug and test signals as described in chapter 4.4.2.

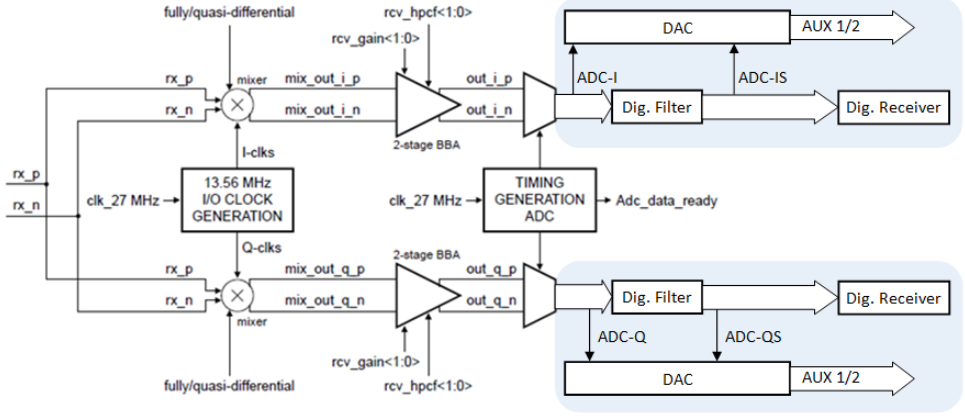


Fig 40. CLRC663 Rx block diagram

The optimum register settings might be different from the default values stored in the EEPROM. So, for the optimization and testing typically the registers can be tuned and changed directly. As soon as the optimum settings are derived, the new settings might be changed. Then the optimized values must be set in the final application.

The default settings in the EEPROM are optimized for the CLRC663 based on the evaluation board antenna. Some of these settings might be adjusted and optimized for other antenna designs.

4.4.1 External Rx components

The RxP and RxN are connected to the antenna circuit. Typically, there is a standard coupling capacitor used to connect the Rx circuit to the EMC filter (see Fig 17). External filtering is normally not required.

The voltage level at the RxN and RxP must be high enough to achieve a good sensitivity, but must not exceed the given limit (see [1]).

Typically, the serial resistor R2A and R2B is in the range of 7…15 kΩ. The exact value can be chosen by measuring the Rx voltage. The measurement can be done in following steps:

1. Choose R2A and R2B (e.g. start with 11 kΩ).

2. Measure the Voltage (measure with active probe) at RxN and RxP. The U_{max} and $U_{peak\ to\ peak} \leq 1.7$ V and above 1.2 V (Typical 1,5 V)
   a. Measure with active and passive loading (Ref PICC and card in the field) and check the Voltage at RxN and RxP.
3. Adopt the R2A and R2B value
   a. If the voltage at RxN and RxP is > 1.7 V than increase the resistor value. The resistor must be increased until the voltage is in the limit.
   b. If the voltage at RxN and RxP is < 1.2 V than decrease the resistor value. The resistor must be decreased until the voltage is within the limit.

Note: The voltage measurement at the RxP and RxN pins must be done with low capacitance probe (active probe) with an input capacitance of < 3 pF.

Note: The relevant value is the peak value, which shall be as large as possible without exceeding the specified limit (refer to [1]). Typically, a value of V_{Rxpeak} = 1.5 V is optimum.

Note: Consider antenna loading and detuning effects!

4.4.2 Debugging

In reader design, it is often required to optimize the hardware in terms of performance and noise. For critical designs, it is necessary to check the receiver path for noise, which could cause problems in the communication with the card. To do this kind of debugging or to optimize the reader towards best performance, the CLRC663 has two Pins AUX1 and AUX2 which can be used to measure analog debug signals.

The following part is an overview of how to use these pins for debugging purposes.

4.4.2.1 Unlock RC663

To use the analog debug pins Aux 1 and Aux 2 3 relevant registers must be configured. These registers are locked and set to read only as default. To use the registers, they need to be unlocked. The following unlock procedure shows how to unlock these registers the RC 663. It is important that you only use the registers as described.

Note: If you configure the registers in a different way than the described one or you set other undescribed registers, the RC663 can be destroyed.

The unlock procedure must be in this order. It is necessary to exactly follow the order with every write and read register.
TestMode is Register 0x66. After a power-down or reset the CLRC 663 goes back into default and locked state.

Following example is using the CLRC663PcSerial.3.6 to unlock the Chip:

(SR = sets the Register (first Value) with the second Value, GR= reads the Register)

```
SR 66 80
GR 66
SR 66 C0
SR 66 E0
GR 66
SR 66 D0
GR 66
SR 66 C3
GR 66
```

Now you can configure register 0x6C, 0x6D and 0x65 as described in chapter 4.4.2.3.

4.4.2.2 Lock the unlocked RC663

There are two ways to lock the RC663 after unlocking it. First of all, with every reset or power on reset (POR) the RC663 is locked again. But the IC can also be locked without reset or POR by writing 0x00 into the TestMode Register (Register 0x66). When register 0x66 is set to 0 the configured values remain in the latest condition and the 663 is locked. The values are stored in the registers until a reset or POR occurs, which sets the registers again set to the default values.

Note: Do not use other settings or other undescribed registers in the unlocked state of the CLRC 663! The IC can be destroyed.

4.4.2.3 Setting for Aux usage and test signal description

The register 6Ch and 6Dh are set to 09h that allows the use of the DacCon (Digital-analog converter). The DacCon is a test bus that can be used to set different debug signals to the analog debug pins (Aux1 and AUX2).

Table 2. Presetting for Aux1/2 usage

Register	Value	Description
0x06C	09h	Set AnaTbSel1 to 9 for using DacCon register to configure the Aux pins
0x6D	09h	Set AnaTbSel2 to 9 for using DacCon register to configure the Aux pins

Table 3. Aux1/2 settings (Register 0x65)

Register	Value	Aux1 signal	Aux2 Signal	Description
0x65	0x11	ADC - Q	ADC - Q	Upper half byte for **Aux1** signal setting and Lower half byte for **Aux2**. The test Signals can be combined as shown exemplary in this table.
	0x22	ADC _ I	ADC _ I	
	0x33	ADC - QS	ADC - QS	
	0x44	ADC - IS	ADC - IS	
	0x12	ADC - Q	ADC - I	
	0x13	ADC – Q	ADC - QS	
	0x14	ADC - Q	ADC - IS	
	0x99	bpsk_sum	bpsk_sum	
	0xAA	dpresent_sum	dpresent_sum	

The Q and I signal are from the Analog Part before the filter stage. QS and IS are picked up after the filter (Fig 40).

bpsk_sum

This test signal shows the sum of the bpsk phase jumps. Each peak of this signal indicates a detected phase jump of the activated receiver.

dpresent_sum

This signal shows the correlation of the sampled ADC signal with the subcarrier, so a high value is shown if the subcarrier is detected.

4.4.2.4 How to debug with analog test signals examples

The following test examples are done with the RC663 evaluation board V3.0 and a MIFARE product 1k card. The reader sends an ISO/IEC 14443 REQA command and the card is answering. This answer (ATQA) is measured at the AUX1 pin.

All different signal types are measured with the same setup.

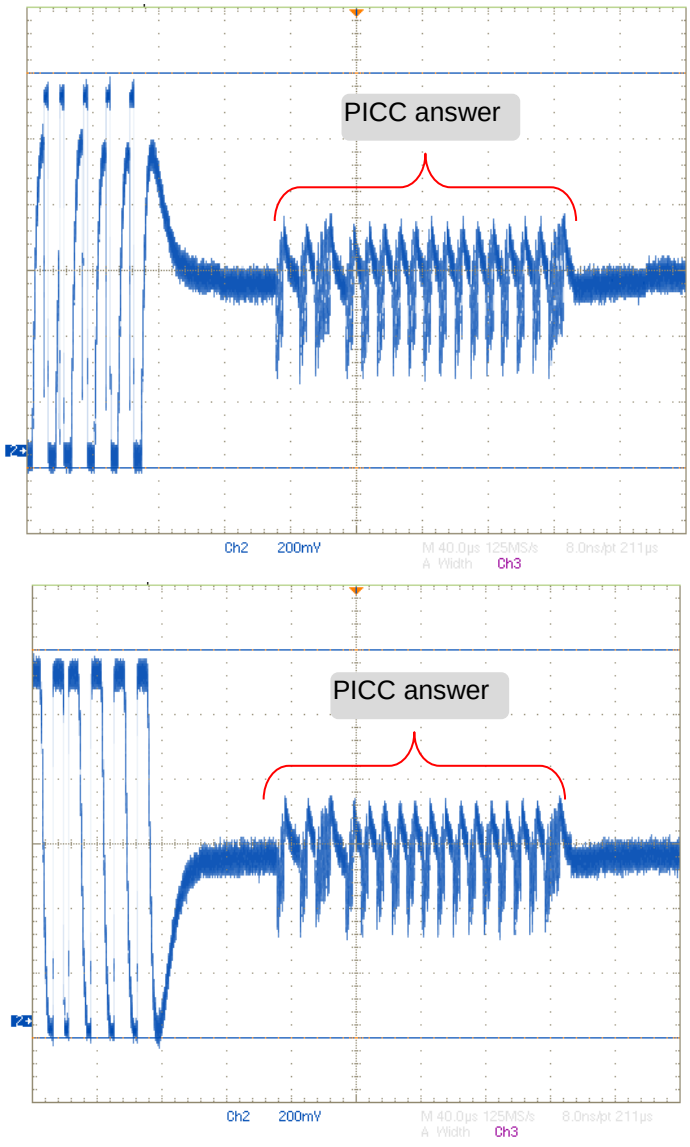
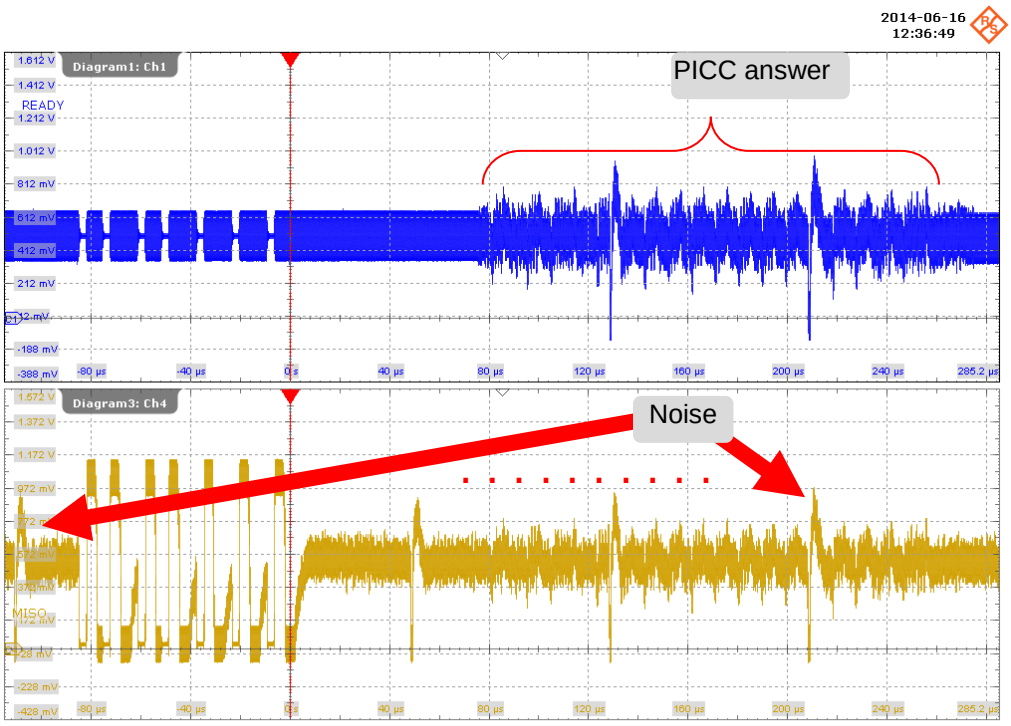


Fig 41. AUX1 with ADC-I signal AUX2 with ADC-Q signal

In Fig 41 you see a clear card answer directly after the REQA of the reader. After the answer the “normal” noise level is seen without any disturbance or huge noise spikes on the receiver path. That means these signals show that there is no additional noise on the receiver path that requires further investigation.

The next figure (Fig 42) shows the ADC Q signal at the Aux1 pin. At the beginning of the screenshot the Request A of the reader is shown, shortly behind the card answer. In addition to that, a harmonic noise signal with nearly the same amplitude as the card answer is visible. This noise is disturbing our receiver path that means we cannot get always a correct answer of the card, even if the response is quite clear and strong. This noise reduces the receiver performance of the reader.



(1) blue : ADC QS

(2) yellow: ADC Q

Fig 42. AUX1 with ADC-Q signal with PICC answer with noise

In this case the hardware needs to be analyzed, to find the source of this noise signal and reduce the noise level.

With the ADC I and Q signal the unfiltered receiver signal is given to the Aux pins. In addition to that the filtered I and Q channel can also be shown at these pins (Fig 43 example of ADC IS/QS). With the filtered signals, it is possible to see if the full answer is detected by the digital path of the CLRC663 receiver. The sampled I and Q signal are stopped as soon as the card answer is received properly, or if there is an error in the communication detected.

In comparison to this the un-filtered signals always show the full receiver signal.

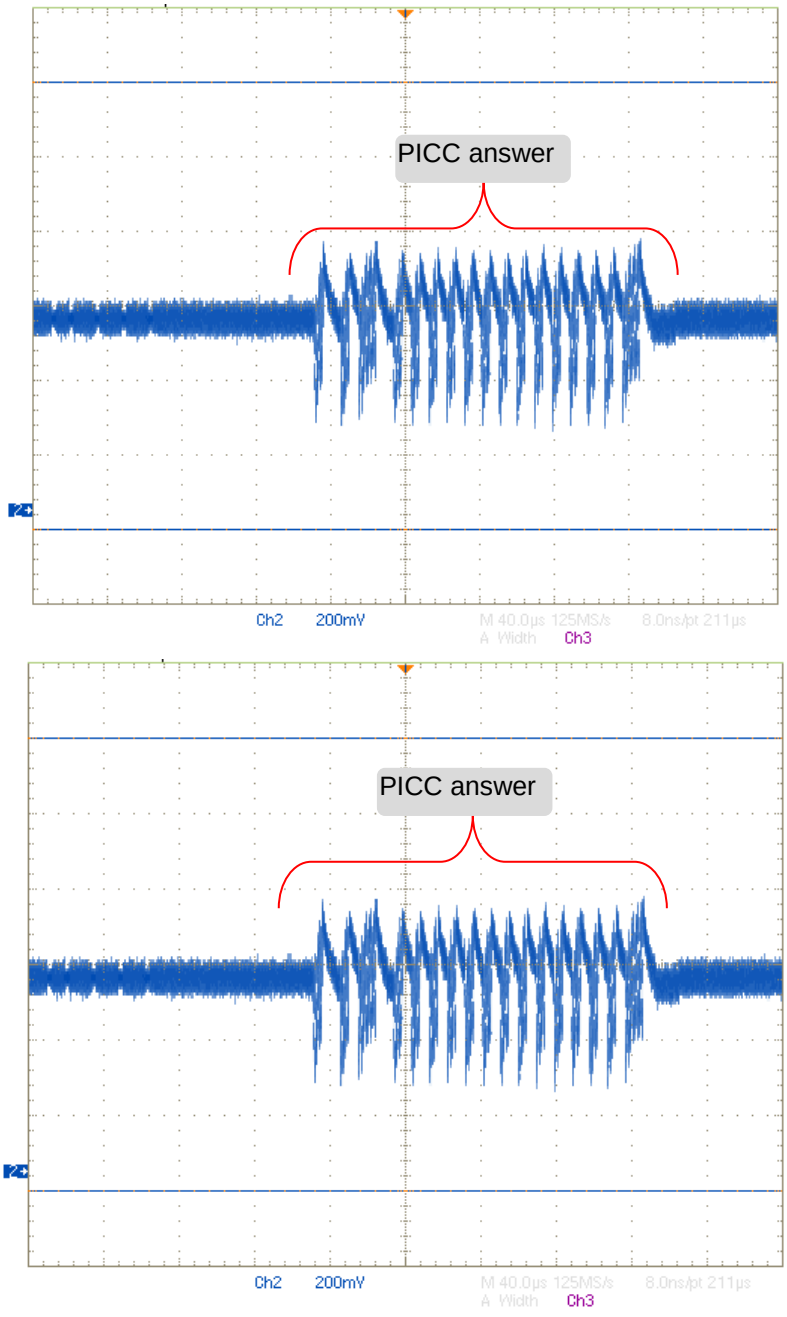
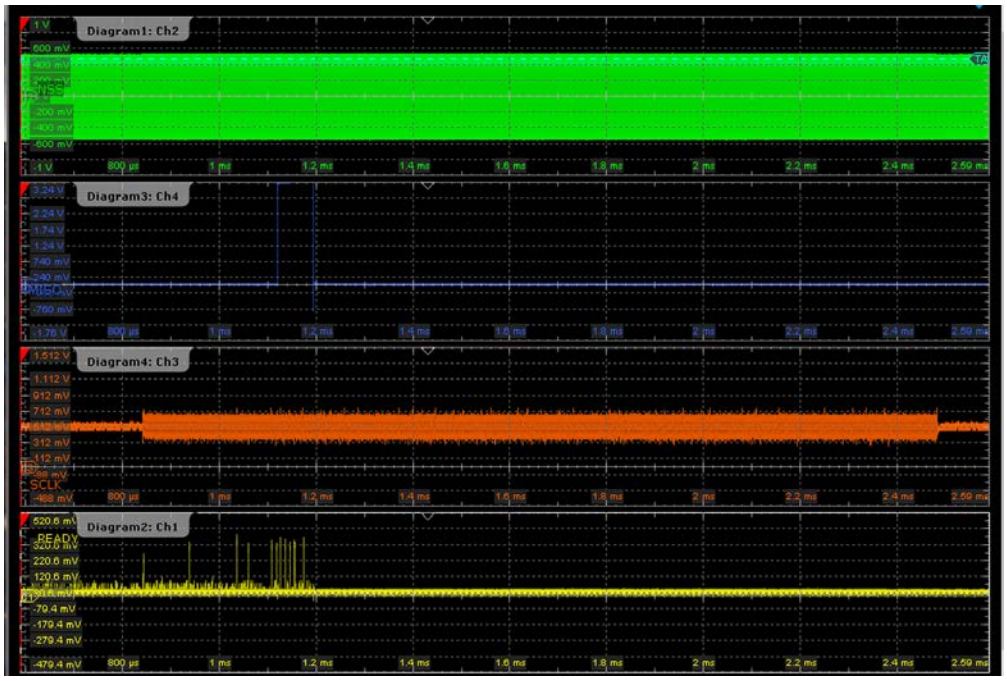


Fig 43. AUX1 with ADC-QS and IS signal

The same procedure can also be used for ISO/IEC 14443 type B or other standards. The target is to see if there is noise on the receiver and to check if the card answer is strong enough to be seen by the receiver. These test signals can be used to optimize the register settings.

Fig 44 shows an ISO/IEC 14443 type B answer which is not received fully, even though the signal is quite clear and also the phase jumps of the BPSK are much higher than the background noise level. In this case the failure could have two main reasons. First there

is a real short and high noise peak that is not visible in this timescale. The other reason for the failure might be a wrong register setting.



(1) green : field from the pickup coil
(2) blue : dpresent_sum
(3) orange: ADC Q
(4) yellow : bpsk:sum

Fig 44. Type B failed reception

4.4.3 Optimization

The following chapter is describing a way to optimize the CLRC663, MFRC630 / 631 and SLRC610 towards optimum receiver performance. If the transmitter path of the reader is done as shown before in this document and the expected target for field strength and pulse shapes as well as the receiver voltage is reached, the last step is to find the optimum register setting for the receiver. The first point that needs to be done is to check with some sample tags (for each standard that should be supported also for different tag sizes, if needed), if the card response is seen as soon as the card is answering or if there is an answer but the reader is not able to see this answer. If the answer is always seen, the reader is optimized.

Recommendation:

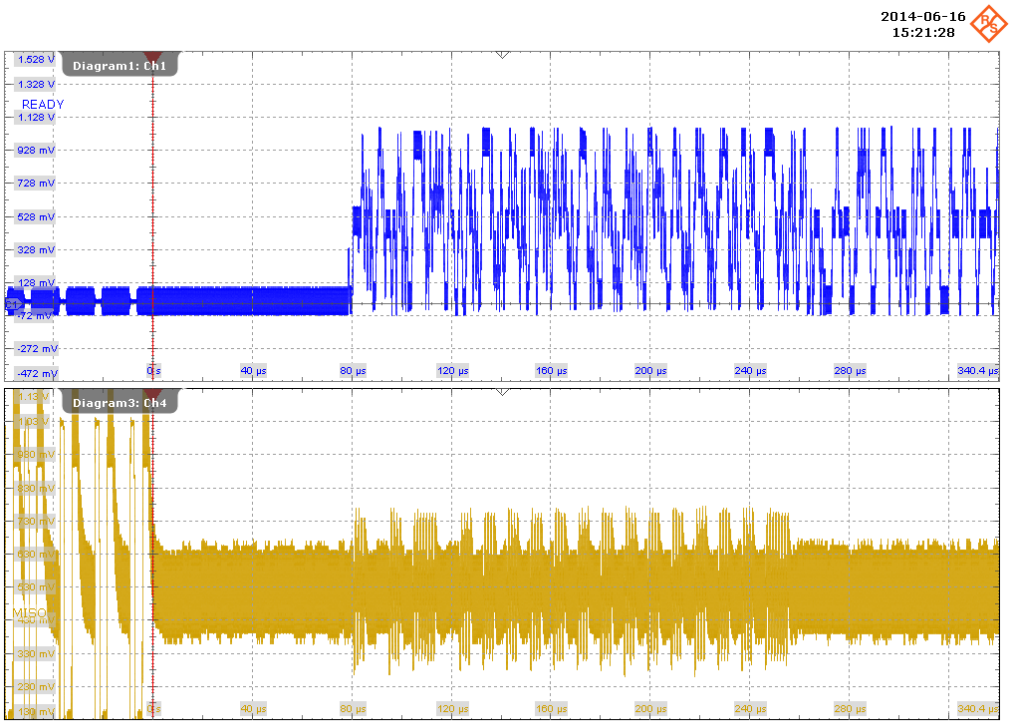
1) Do not use RectFilter in Register 5Dh (RxMod) for ISO/IEC 14443 type A and B, NFC and FeliCa communication. This feature is only relevant for ISO/IEC 15693 and will otherwise dramatically reduce the sensitivity and stability of the receiver path.

2) Turn of the PreFilter in register 5Dh for the optimization procedure itself. Turn it on only after optimization, to check if it increases the performance.

4.4.3.1 Type A optimization

For type A optimization the most usable signals are the **dpresent_sum** as well as the **ADC I/Q** signal. The optimization is always needed. In Fig 45 a fail signal is shown. The receiver starts decoding the ISO/IEC 14443 type A answer, but due to a low Rx threshold setting the CLRC663 does not detect the end of the frame, so it does not stop (Chanel 1, blue Signal) after the card answer is finished (Chanel 2, yellow).

To optimize the settings, it is recommended to disable all optional features (like PreFilter in Register 5Dh, etc.).



(1) blue : dpresent_sum

(2) yellow: ADC Q

Fig 45. Type A fail to decode the card answer

Following is a short example of one way for optimizing the settings for the CLRC663.

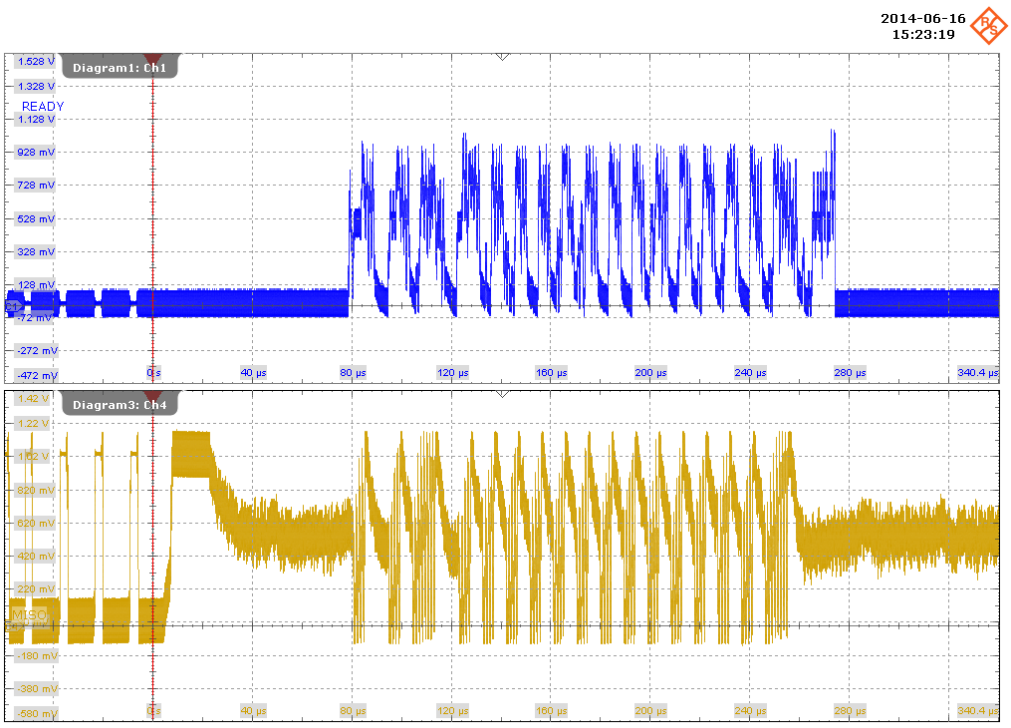
Steps:

- Unlock CLRC663 (as described in chapter 4.4.2.1)
  - Route the test signals to the Aux pins
  - Connect the probe to the Aux pins with a ground connection that is a close as possible (ground wounded around the probe), to avoid noise coupling into the test signal.
- Use the sigout as trigger signal (typically: Tx active, falling edge)
- Place a card in the field and decrease the distance to the point where the card starts to be seen by the reader
- Check the ADC I/Q signal (chose the stronger one)

- Increase the distance if an answer is stronger than the noise on the ADC signal.
- Now change the following registers to see if the reader can be configured to get the card answer (changing only one value at the time do see the impact)
  - xAna (add.: 39h) rcv_hpcf and rcv_gain (always start with max gain and min hpcf)
  - RxThreshold (add.: 37h); Adjust Minlevel without a card in the field, starting with 0h and increase up to the value where no ghost card (reader shows errors and random data without a card in the field) is seen any more
- RxMod (add: 5Dh) PreFilter and RectFilter (Bit 4 and 5) **always disable RectFilter!** After optimization enable PreFilter and check if this increases the performance, if not it can also stay disabled.

After the optimization, the reader should see the full answer as soon as the card starts responding (Fig 46).

Note: In case the anti-collision is implemented the setting of the collision level also needs to be optimized after the single card operation is optimized. For this optimization, the CollLevel in register 38h (RCV) needs to be adopted.



(1) Ch1(blue) : dpressent_sum

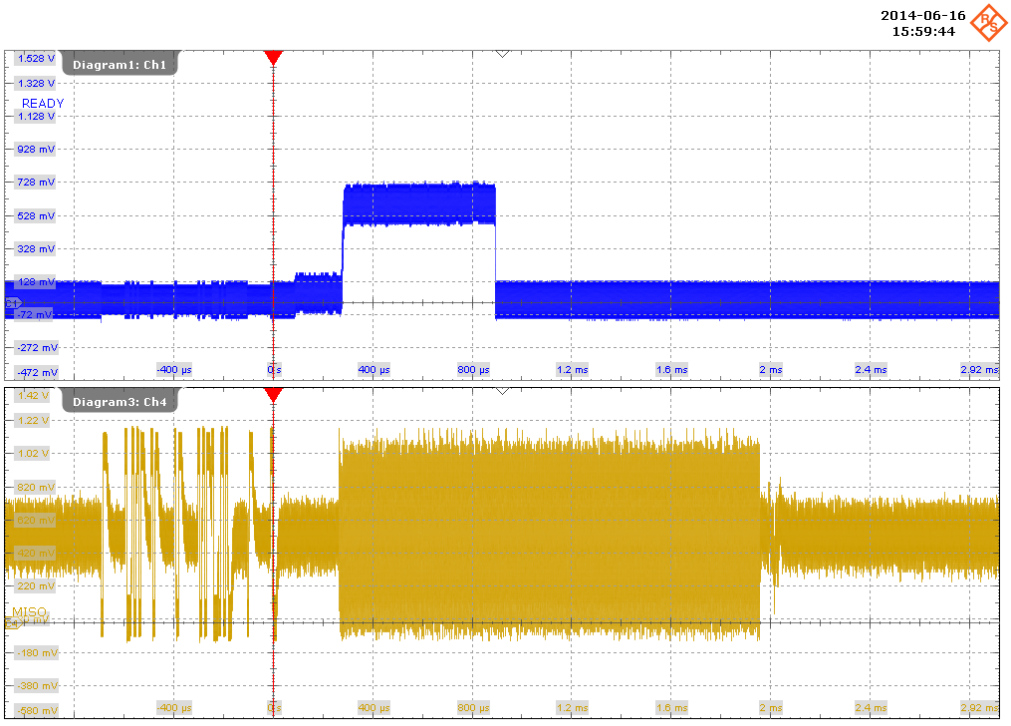
(2) Ch4 (yellow) : ADC Q

Fig 46. Valid Type A answer

4.4.3.2 Type B optimization

For type B the most usable signals are the **dpresent_sum, bpsk_sum** and **ADC I/Q.** To optimize the settings, it is recommended to disable all optional features (like PreFilter in Register 5Dh, etc.).

The optimization is always required to achieve the best settings for the own hardware to get the best performance. Fig 47 shows an example of a clear type B answer that is not fully detected by the reader. The receiver stopped in the middle of the card answer due to a wrong setting of RectFilter (enabled). The full length of the card answer is shown by the ADC Q signal on Chanel 4 (yellow), while the Channel 1 (blue) shows the dpresent_sum signal, indicating the receiver stopping too early.



(1) blue : dpresent_sum

(2) yellow : ADC Q

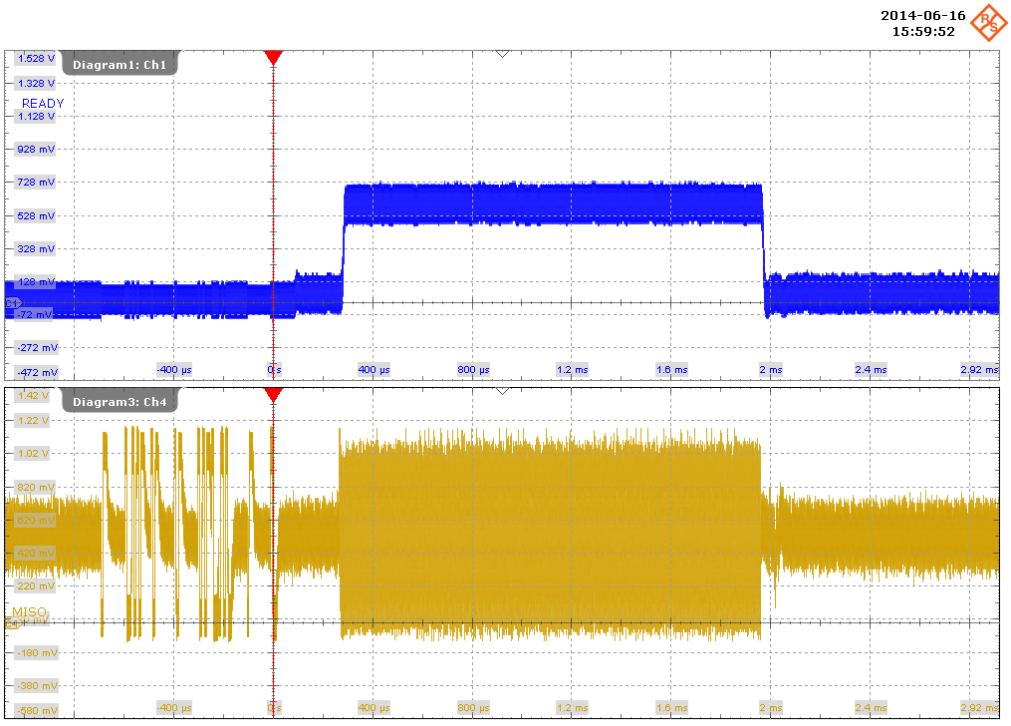
Fig 47. Type B failed reception

To optimize the performance the following steps are a short example of one way for optimizing the settings for the CLRC663.

Steps:

- Unlock CLRC663 (as described in chapter 4.4.2.1).
  - Rout the test signals to the AUX pins.
  - Connect the probe to the AUX pins with a ground connection, which is as short as possible (ground wounded around the probe) to avoid noise coupling into the test signal.
- Use the SIGOUT as trigger signal (typically: Tx active, falling edge).
- Adjust RxThreshold (add.: 37h), step 1:
  - Adjust Minlevel without a card in the field, starting with 0h and increase up to the value where no ghost card (reader shows errors and random data without a card in the field) is seen any more.
- Place a card in the field and decrease the distance to the point where the receiver starts to detect the card.
- Check the ADC I/Q signal (chose the stronger one) and also check the bpsk_sum signal to ensure that the phase jumps are higher than the noise.
- Increase the distance if an answer is stronger than the noise on the ADC signal.
- Now change the following registers to see if the reader can be configured to get the card answer (changing only one value at the time do see the impact):
  - RxAna (add.: 39h) rcv_hpcf and rcv_gain
    (always start with max gain and min hpcf)
  - RxThreshold (add.: 37h), step 2: Adjust MinlevelP: to optimize this value a card needs to be placed in the field at the maximum reading distance where the card is starting to answer (it needs to be the border to see if the register change increases or decreases the reading distance). E.g. increase the value beginning from 0h and see if it is possible to get a value where which increase the reading distance (assuming the card is answering always, which can be cross checked on the ADC I/Q signal).
  - RxMod (add: 5Dh) PreFilter and RectFilter (Bit 4 and 5)
    always disable RectFilter!
    After optimization enable PreFilter and check if this increases the performance (if not it can also stay disabled).

After the optimization, the reader should see the full answer as soon as the card starts responding (see Fig 48 a type B answer is shown that is fully detected by the CLRC663).



(1) Ch1, blue : dpresent_sum

(2) Ch4, yellow : ADC Q

Fig 48. AUX1 with ADC-Q signal with PICC answer

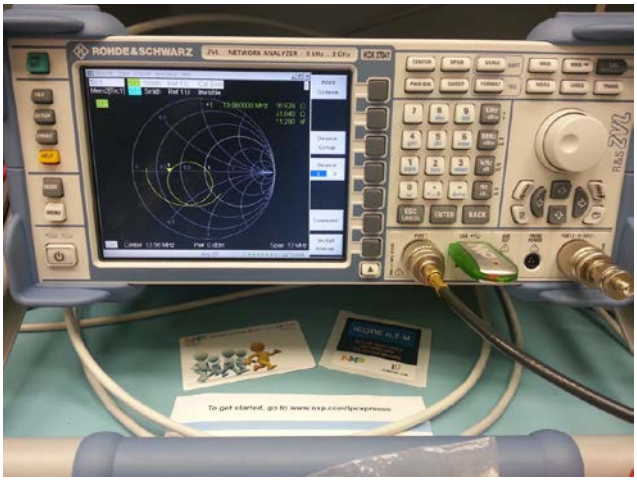
5. Annex

5.1 VNA and calibration

This annex describes some basics about impedance measurement and the related measurement tools.

5.1.1 Vector Network Analyzer

The impedance measurement must be done with a vector network analyzer, e.g. as shown in Fig 49.

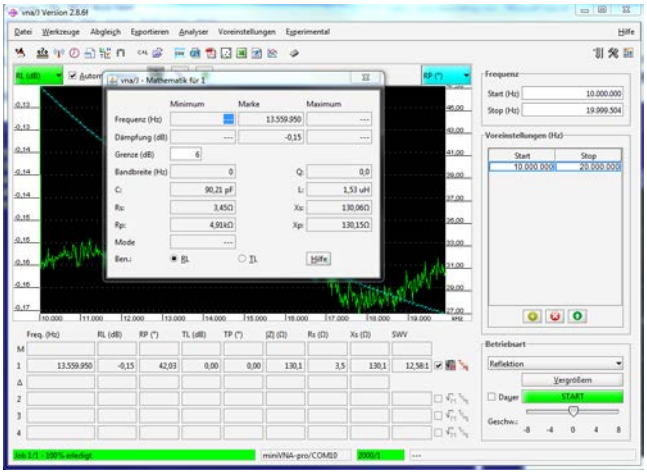


d. Rohde & Schwarz ZVL (refer to [10])

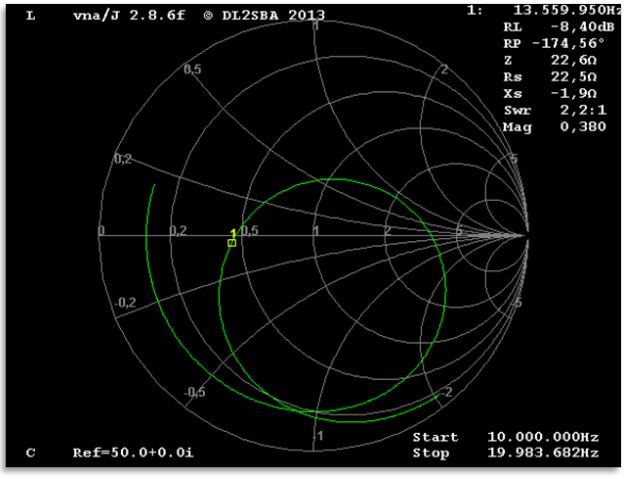
e. MiniVNA Pro (refer to [11])

Fig 49. Examples of Vector Network Analyzers

For the miniVNA Pro the recommendation is to use the VNA/J SW tool (refer to [12]), as shown in Fig 50.



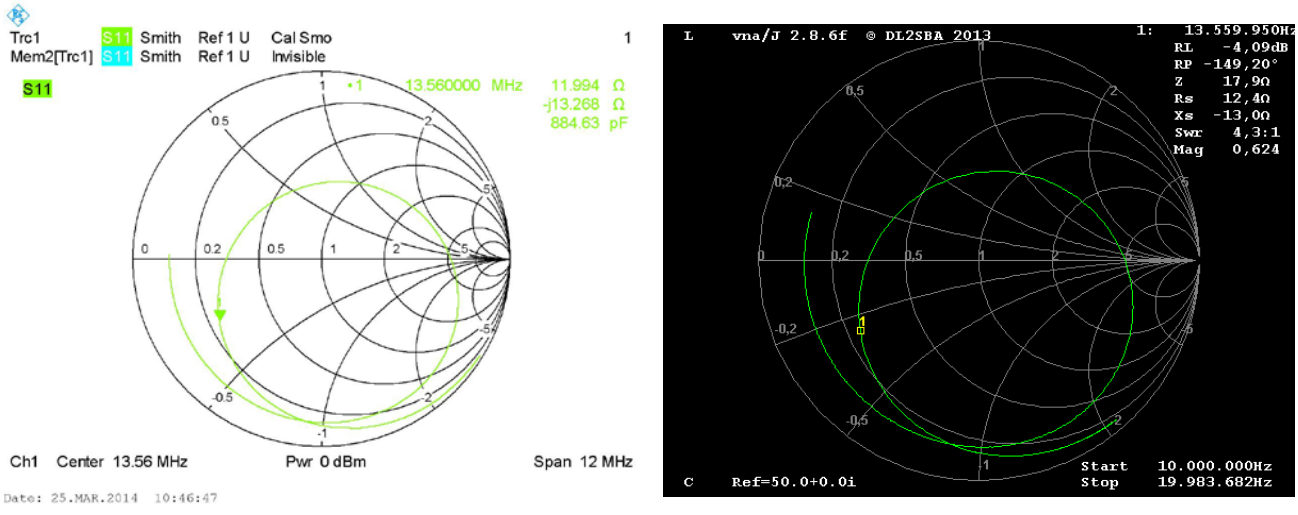
a. VNA/J with antenna coil measurement



b. VNA/J Smith chart example

Fig 50. VNA/J from DL2SBA (refer to [12])

In Fig 51 the result of the same measurement is shown for the R&S ZVL as well as for the VNA/J using the miniVNA Pro. The accuracy of the ZVL is much higher than the one of the miniVNA Pro. However, for the antenna matching and tuning procedure as described in this document, both devices can be used.



a. From R&S ZVL

b. From miniVNA Pro

Fig 51. Impedance Measurement result example (Smith chart)

5.1.2 Impedance measurement

The impedance measurement, which is needed to tune the antenna circuit correctly, is a S11 measurement, showing the normalized resistance and reactance of the antenna circuit impedance in a smith chart:

$$\underline{Z} = |Z| \cdot e^{j\theta} = R + jX \quad (5)$$

$\underline{Z}$ = complex impedance

Θ = phase between voltage and current

R = real part, resistance

X = imaginary part, reactance

The smith chart shows the normalized impedance, typically normalized to 50 Ω. Some measurement and simulation tools allow a normalization to values different than 50 Ω. However, in this document the normalization is not changed.

The return loss (reflection coefficient), which can be directly derived from the S11 measurement (i.e. from the smith chart), is of no interest for the NFC Reader antenna tuning, since no 50 Ω system is used. This return loss could only be used, if the chosen target impedance is 50 Ω. Anyhow the return loss does not show the phase or whether the circuit is capacitive or inductive.

Typically, a frequency sweep from 10 MHz to 20 MHz is enough to do the antenna tuning.

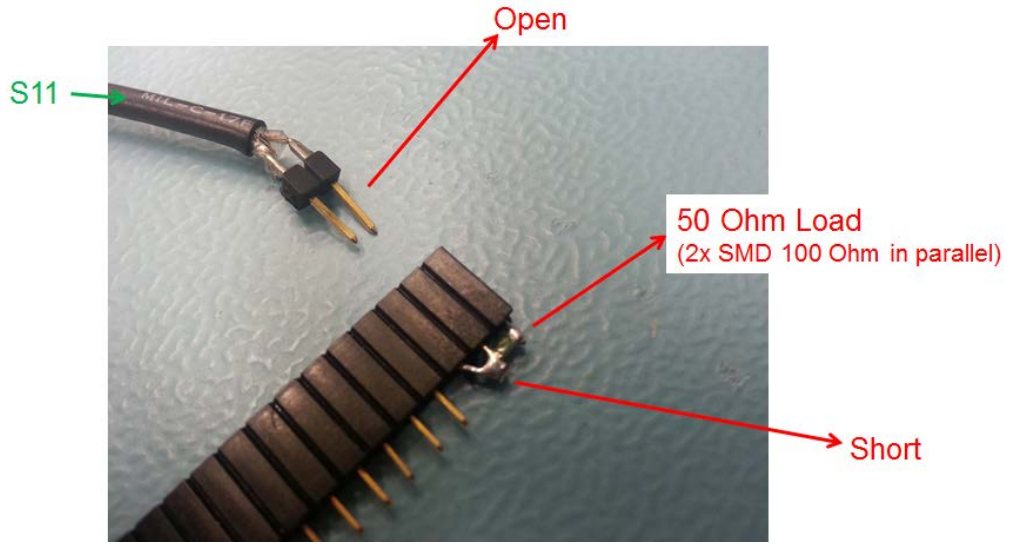
The standard VNA provides an unbalanced 50 Ω measurement port, which is used here to measure a balanced impedance. The mismatch due to this setup error can be neglected.

The power level must be low enough (e.g. 0 dBm or less), and the CLRC663 must be unpowered. Then the CLRC663 can remain in the circuit, while measuring the S11 between Tx1 and Tx2.

5.1.3 Calibration

The major part before the measurement itself is the calibration of the measurement tool (VNA) and measurement setup (cable and probe). A high end 50 Ω calibration kit for the used connector types (N-connector or SMA) does not help much, since the measurement itself needs to be done at the Tx pins of the used NFC Reader IC as possible. Therefore, the calibration must be done as close at these points as possible.

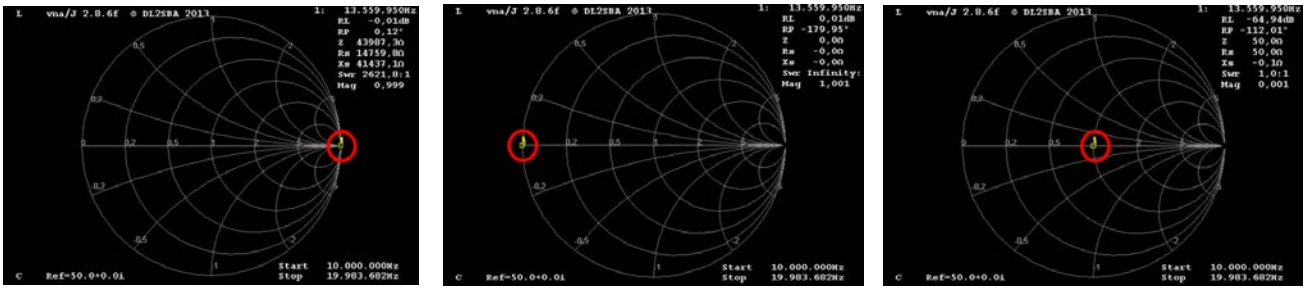
So, the better solution is to create a simple connection, i.e. using a standard 2.54 mm pin row connector (male and female) to connect the VNA. This can be used to measure the antenna impedance at the correct points, but also to calibrate the VNA. A very simple but highly efficient homemade connector and tool is shown in Fig 52.



(1) The mismatch due to the unbalanced measurement of a balanced impedance can be ignored.

Fig 52. Measurement connector and calibration kit

After the calibration, the measurement setup should be checked and should show the results as shown in Fig 53.



a. Open b. Short c. Load

Fig 53. Calibration result

6. References

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[11] MiniVNA Pro, http://miniradiosolutions.com/minivna-pro/

[12] VNA/J from Dietmar Krause, DL2SBA, www.dl2sba.com

[13] AN11246_239810 - Antenna matching calculation, http://www.nxp.com

7. Abbreviations

Abbr.	Meaning
A/m	Ampere per meter (magnetic field strength measurement unit)
AN	Application Note
EMC	ElectroMagnetic Compatibility
Hmin / Hmax	Minimal and Maximum magnetic field strength
IC	Integrated Circuit
ISO/IEC	International Standard Organization / International Electrotechnical Community
LMA	Load modulation amplitude
mA	milliampere
MHz	Mega Hertz
NFC	Near Field Communication
PCB	Printed Circuit Board
PCD	Proximity Coupling Device (Contactless reader)
PICC	Proximity Integrated Circuit Card (Contactless card)
Q / Q-factor	Quality Factor
RF	Radiofrequency
TBD	To Be Defined
V	Voltage

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