AN10419

Single card I²C bus buffers

Rev. 1 — 10 November 2010 Application note

Document information

Info	Content
Keywords	PCA9515A, PCA9516A, PCA9518A
Abstract	NXP Semiconductors family of level shifting bus buffers are detailed in this application note that discusses device operation, maximum cable length and frequency calculations and typical applications.

Revision history

Rev	Date	Description
1	20101110	application note; initial version

Contact information

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1. Introduction

1.1 Description

PCA9515A/16A/18A series of single card I²C-bus and SMBus bus buffers are used where I/O card insertion into a live backplane is not required such as telephones, personal computers and laptop computers. These applications do not require long bus length when masters and slave are located on the same PC boards or enclosed in a same small cabinet.

The PCA9515A/16A/18A are designed to work with I²C clock frequencies up to 400 kHz and are suitable for utilization in a multi-master I²C-bus or SMBus environment. The devices support bus arbitration and contention with bus masters located on any segment. They are bidirectional and require no direction control.

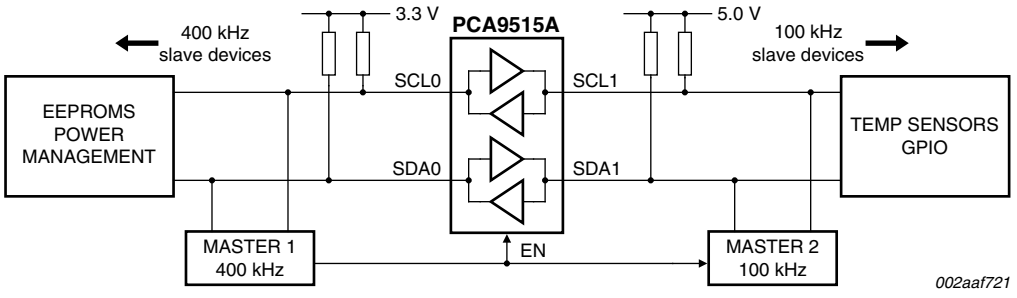
The PCA9515A/16A/18A also support logic level translations since either side voltage can be at different levels. While retaining all the operating modes and features of the I²C-bus system during the level shifts, it also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enables the system designer to isolate two halves of a bus for both voltage and capacitance.

The PCA9515A/16A/18A are static offset buffers. All sides have static offset and can operate only with slaves and masters with I²C-bus compliant (normal) I/Os.

There are no external hardware address pins since these devices do not have an I²C address. The bus buffer devices merely buffer the I²C-bus signals from segment to segment and do not respond to any I²C commands.

1.2 Applications

The typical application of PCA9515A/16A/18A bus buffers is as shown in Figure 1.



Master 1 works at 400 kHz only and cannot access 100 kHz only slaves.

Master 2 works at 100 kHz only and can access 100 kHz/400 kHz slaves.

PCA9515A is disabled when Master 1 sends commands.

PCA9516A is a 1-to-4 channel buffer and PCA9518A is expandable 1-to-4 channel buffer.

Fig 1. Typical single card bus buffer application

- They allow extension of the I²C-bus or SMBus on systems requiring capacitance loads larger than the 400 pF (max.) specified by the I²C-bus protocol. Designers can extend the use of the I²C-bus or SMBus in systems with more devices and/or longer bus lengths with only one repeater delay between any devices. The devices are multi-master capable and support arbitration and bus contention on any segment.
- The PCA9515A/16A/18A allow mixed operation of 100 kHz and 400 kHz devices on a combined bus by isolating the segment with 100 kHz devices from the rest of the 400 kHz system so that the 400 kHz devices can operate at their maximum speed.
- The PCA9515A/16A/18A have an individual repeater channel with an enable/disable feature that can be used to electrically isolate that segment of the I²C-bus or SMBus for using the same address slave device on a different segment.
- The PCA9515A/16A/18A release their I/O pins should their supply voltage fail. Sensing multiple power supplies on different bus segments and providing automatic isolation of failed segments or segments suffering ‘brown-out’ of their power supplies.
- The PCA9515A/16A/18A also support logic level translations since either side voltage can be at different levels.

1.3 Device features and characteristics

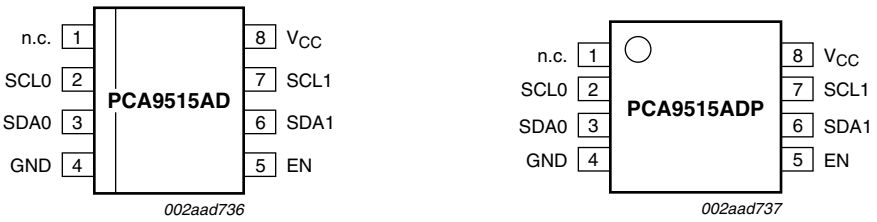
- Bidirectional buffer for the SDA and SCL lines designed to prevent I²C-bus corruption during live board insertion and removal from the backplane using enable feature
- Compatible with I²C-bus Standard-mode, I²C-bus Fast-mode, and SMBus standards; multi-master capable
- Low I_{CC} chip enable/disable: < 1 mA
- Wide operating voltage range with 5.5 V tolerant I²C and enable (EN) pins
- Supports arbitration and clock stretching across the repeater
- Active HIGH repeater enable input
- Powered-off high-impedance I²C-bus pins
- Open-drain input/outputs
- Lock-up free operation
- All I/Os are 5.5 V tolerant
- Operating temperature range is −40 °C to +85 °C
- Accommodate 100 kHz and 400 kHz devices and multiple masters
- ESD protection exceeds:
  - 2000 V HBM per JESD22-A114
  - 200 V MM per JESD22-A115
  - 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- PCA9515A is offered in SO8 (D) and TSSOP8 (MSOP) (DP) packages; PCA9516A is offered in SO16 and TSSOP16 packages; PCA9518A is available in SO20 and TSSOP20 packages

Table 1. Device selection summary

Feature	PCA9515A	PCA9516A	PCA9518A
V_{CC} range	2.3 V to 3.6 V	2.3 V to 3.6 V	2.3 V to 3.6 V
Number of channels	1	5	5
Input/output characteristics	$V_{IL} < 0.3V_{CC} \rightarrow V_{OL} = 0.52$ V at 6 mA $V_{IH} > 0.7V_{CC} \rightarrow V_O$ to V_{bus}	$V_{IL} < 0.3V_{CC} \rightarrow V_{OL} = 0.52$ V at 6 mA $V_{IH} > 0.7V_{CC} \rightarrow V_O$ to V_{bus}	$V_{IL} < 0.25V_{DD} \rightarrow V_{OL} = 0.52$ V at 6 mA $V_{IH} > 0.7V_{DD} \rightarrow V_O$ to V_{bus}

1.4 Package and pin description

1.4.1 PCA9515A



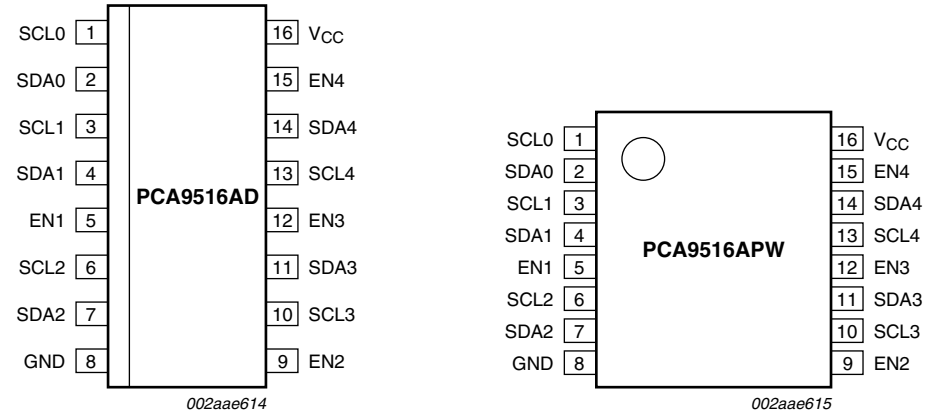
a. SO8 b. TSSOP8

Fig 2. Device pinning for PCA9515A

Table 2. Pin description for PCA9515A

Symbol	Pin	Description
n.c.	1	not connected
SCL0	2	serial clock bus 0; open-drain 5 V tolerant
SDA0	3	serial data bus 0; open-drain 5 V tolerant
GND	4	supply ground (0 V); connect this pin to a ground plane for best results
EN	5	active HIGH repeater enable input (internal pull-up with 100 kΩ)
SDA1	6	serial data bus 1; open-drain 5 V tolerant I/O
SCL1	7	serial clock bus 1; open-drain 5 V tolerant I/O
V_{CC}	8	supply voltage (2.3 V to 3.6 V)

1.4.2 PCA9516A



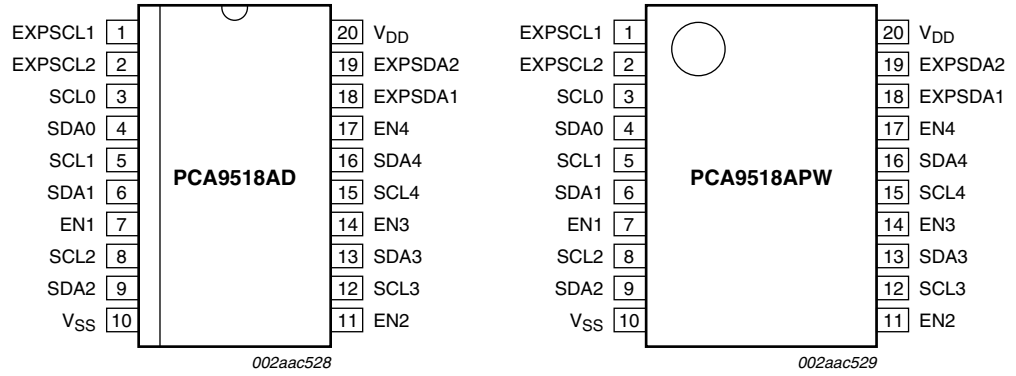
a. SO16 b. TSSOP16

Fig 3. Device pinning for PCA9516A

Table 3. Pin description for PCA9516A

Symbol	Pin	Description
SCL0	1	serial clock bus 0; open-drain, 5 V tolerant
SDA0	2	serial data bus 0; open-drain, 5 V tolerant
SCL1	3	serial clock bus 1; open-drain, 5 V tolerant
SDA1	4	serial data bus 1; open-drain, 5 V tolerant
EN1	5	active HIGH bus 1 enable input
SCL2	6	serial clock bus 2; open-drain, 5 V tolerant
SDA2	7	serial data bus 2; open-drain, 5 V tolerant
GND	8	supply ground (0 V); connect this pin to a ground plane for best results
EN2	9	active HIGH bus 2 enable input
SCL3	10	serial clock bus 3; open-drain, 5 V tolerant
SDA3	11	serial data bus 3; open-drain, 5 V tolerant
EN3	12	active HIGH bus 3 enable input
SCL4	13	serial clock bus 4; open-drain, 5 V tolerant
SDA4	14	serial data bus 4; open-drain, 5 V tolerant
EN4	15	active HIGH bus 4 enable input
V_{CC}	16	supply voltage (2.3 V to 3.6 V)

1.4.3 PCA9518A



a. SO20 b. TSSOP20

Fig 4. Device pinning for PCA9518A

Table 4. Pin description

Symbol	Pin	Description
EXPSCL1	1	expandable serial clock pin 1
EXPSCL2	2	expandable serial clock pin 2
SCL0	3	serial clock bus 0; open-drain, 5 V tolerant
SDA0	4	serial data bus 0; open-drain, 5 V tolerant
SCL1	5	serial clock bus 1; open-drain, 5 V tolerant
SDA1	6	serial data bus 1; open-drain, 5 V tolerant
EN1	7	active HIGH bus 1 enable input
SCL2	8	serial clock bus 2; open-drain, 5 V tolerant
SDA2	9	serial data bus 2; open-drain, 5 V tolerant
V_{SS}	10	supply ground (0 V); connect this pin to a ground plane for best results
EN2	11	active HIGH bus 2 enable input
SCL3	12	serial clock bus 3; open-drain, 5 V tolerant
SDA3	13	serial data bus 3; open-drain, 5 V tolerant
EN3	14	active HIGH bus 3 enable input
SCL4	15	serial clock bus 4; open-drain, 5 V tolerant
SDA4	16	serial data bus 4; open-drain, 5 V tolerant
EN4	17	active HIGH bus 4 enable input
EXPSDA1	18	expandable serial data pin 1
EXPSDA2	19	expandable serial data pin 2
V_{DD}	20	supply voltage (2.3 V to 3.6 V)

1.5 Ordering information

Table 5. Ordering information

Package	Container	PCA9515A	PCA9516A	PCA9518A
SO8	tube	PCA9515AD,112	-	-
SO8	tape and reel	PCA9515AD,118	-	-
TSSOP8	tape and reel	PCA9515ADP,118	-	-
SO16	tube	-	PCA9516AD,112	-
SO16	tape and reel	-	PCA9516AD,118	-
TSSOP16	tape and reel	-	PCA9516ADP,118	-
SO20	tube	-	-	PCA9518AD,112
SO20	tape and reel	-	-	PCA9518AD,118
TSSOP20	tape and reel	-	-	PCA9518ADP,118

Additional information on packages including outline dimensions, Moisture Sensitivity Level (MSL) ratings, $R_{th(j-a)}$ can be obtained at www.nxp.com/thermaldata/.

1.6 Data sheets and IBIS/SPICE models

Data sheets and IBIS models can be downloaded from www.nxp.com/edafiles/.

SPICE models require a device-specific Non-Disclosure Agreement (NDA), which can be requested at www.nxp.com/spice_circuit_models/.

2. Technical information

2.1 Functional description and block diagrams

2.1.1 PCA9515A

The PCA9515A integrated circuit contains two identical buffer circuits which enable I²C-bus and similar bus systems to be extended without degradation of system performance. The PCA9515A contains two bidirectional, open-drain buffers specifically designed to support the standard LOW-level contention arbitration of the I²C-bus. Except during arbitration or clock stretching, the PCA9515A acts like a pair of non-inverting, open-drain buffers, one for SDA and one for SCL.

The block diagram for the PCA9515A is shown in Figure 5.

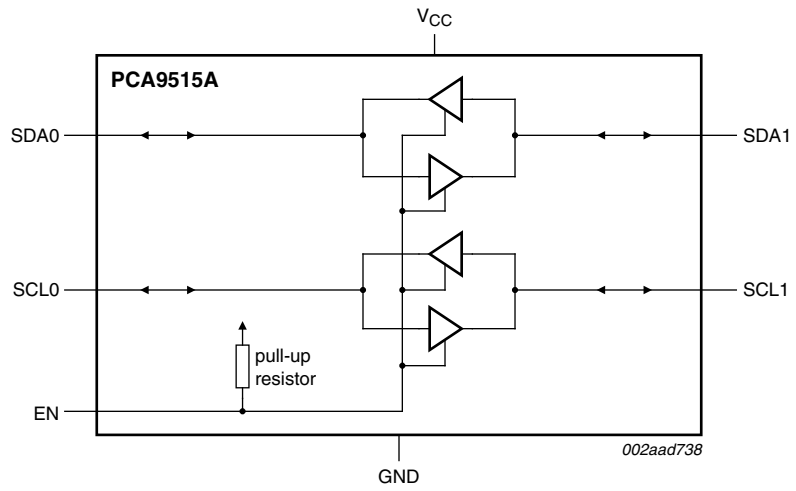


Fig 5. PCA9515A block diagram

2.1.2 PCA9516A

The PCA9516A is a five-way hub repeater, which enables I²C-bus and similar bus systems to be expanded with only one repeater delay and no functional degradation of system performance.

The PCA9516A contains five bidirectional, open-drain buffers specifically designed to support the standard low-level-contention arbitration of the I²C-bus. Except during arbitration or clock stretching, the PCA9516A acts like five pairs of non-inverting, open-drain buffers, one for SDA and one for SCL.

The block diagram for the PCA9516A is shown in Figure 6.

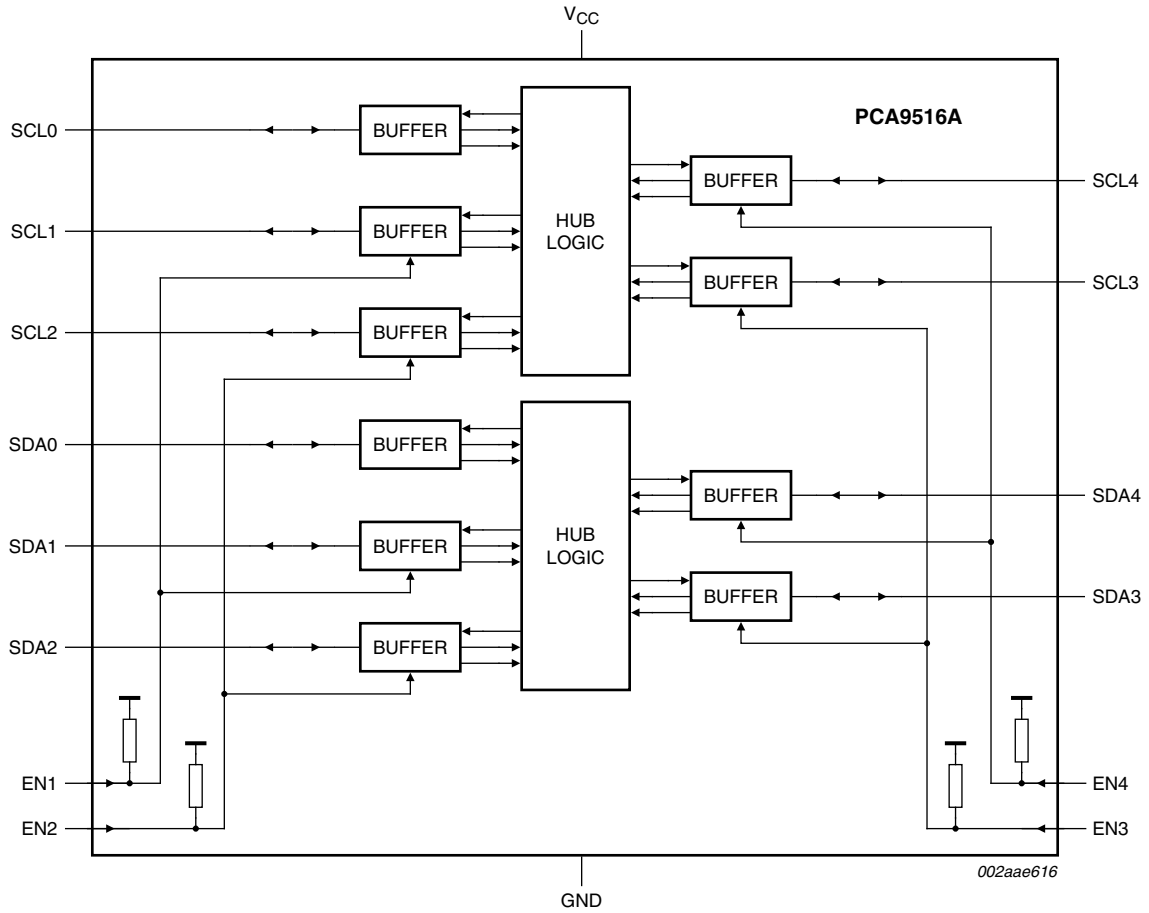


Fig 6. PCA9516A block diagram

2.1.3 PCA9518A

The PCA9518A CMOS integrated circuit is a five-way hub repeater, which enables I²C-bus and similar bus systems to be expanded in increments of five with only one repeater delay and no functional degradation of system performance. The PCA9518A CMOS integrated circuit contains five multi-directional, open-drain buffers specifically designed to support the standard low-level contention arbitration of the I²C-bus. Except during arbitration or clock stretching, the PCA9518A acts like a pair of non-inverting, open-drain buffers, one for SDA and one for SCL.

The block diagram for the PCA9518A is shown in Figure 7.

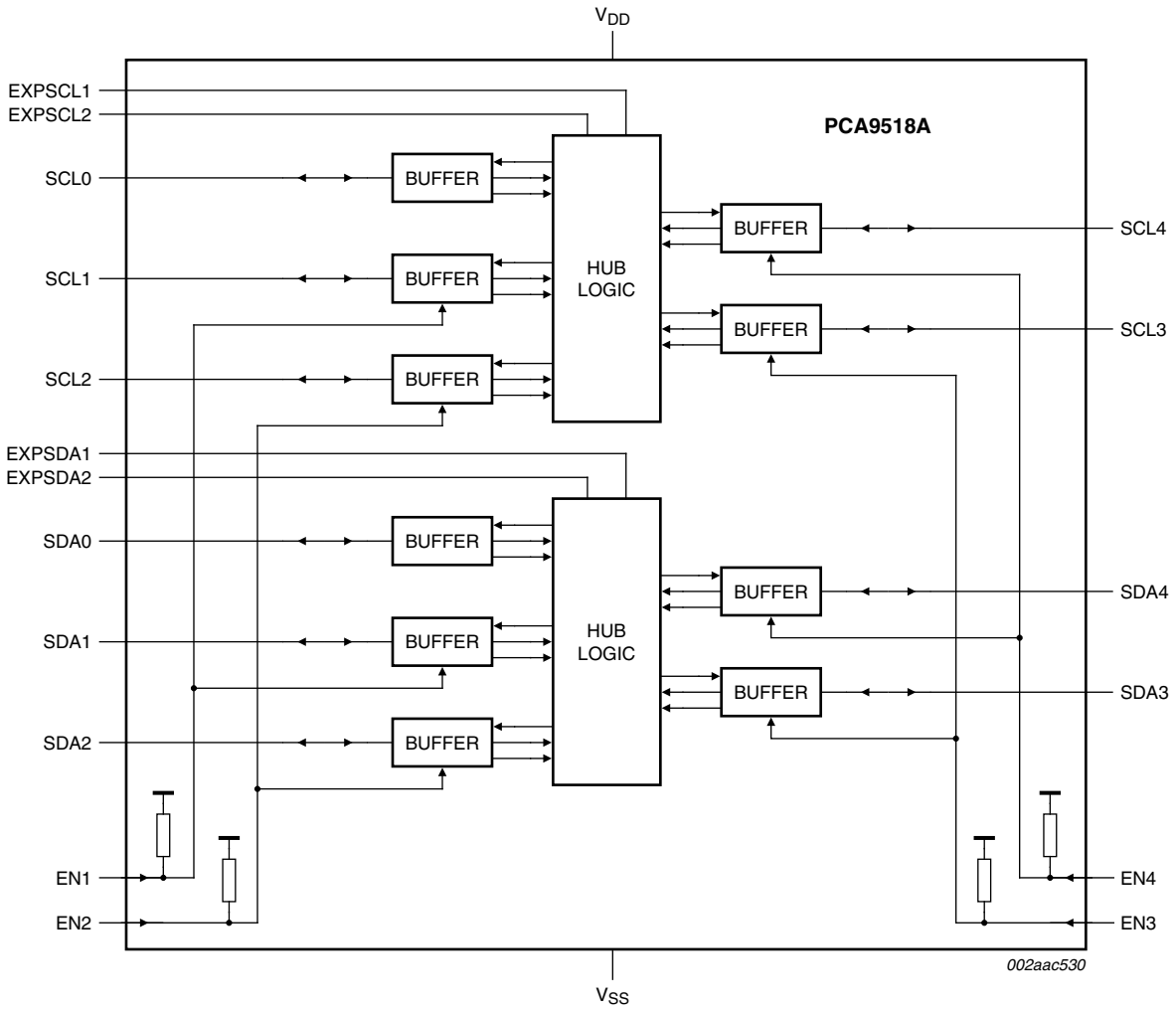


Fig 7. PCA9518A block diagram

3. Applications

3.1 Typical application for PCA9515A

A typical application for PCA9515A is shown in Figure 8. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 5 V bus. Both buses run at 100 kHz unless the slave bus is isolated and then the master bus can run at 400 kHz. Master devices can be placed on either bus.

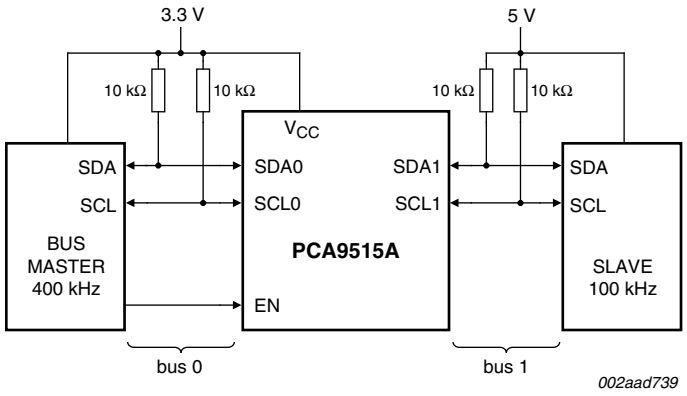


Fig 8. Typical application for PCA9515A

The PCA9515A is 5.5 V tolerant, so it does not require any additional circuitry to translate between the different bus voltages. When one side of the PCA9515A is pulled LOW by a device on the I²C-bus, a CMOS hysteresis type input detects the falling edge and causes the internal driver on the other side to turn on, thus causing the other side to also go LOW. The side driven LOW by the PCA9515A will typically be at V_{OL} = 0.52 V at pull-down current of 6 mA.

3.2 Typical application for PCA9516A

A typical application is shown in Figure 9. In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 5 V bus. All buses run at 100 kHz unless slave 3 is isolated, and then the master bus and slave 1 and slave 2 can run at 400 kHz.

Any segment of the hub can talk to any other segment of the hub. Bus masters and slaves can be located on all five segments with 400 pF load allowed on each segment.

Unused ports should be isolated by holding the enable pin (ENn) to GND and/or pulling SDAn/SCLn pins to V_{CC} through appropriately sized resistors. The primary bus master is normally connected to SDA0/SCL0. If the SDA0/SCL0 port is not used, the pins need to be pulled to V_{CC} through appropriately sized resistors.

The PCA9516A is 5.5 V tolerant so it does not require any additional circuitry to translate between the different bus voltages.

When one side of the PCA9516A is pulled LOW by a device on the I²C-bus, a CMOS hysteresis type input detects the falling edge and causes an internal driver on the other side to turn on, thus causing the other side to also go LOW. The side driven LOW by the PCA9516A will typically be at V_{OL} = 0.52 V at pull-down current of 6 mA.

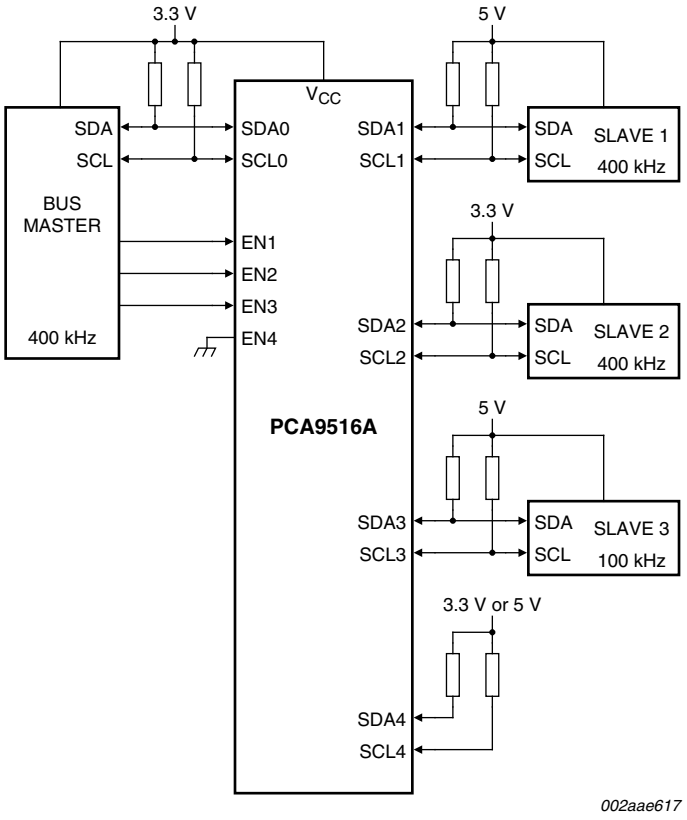


Fig 9. Typical application for PCA9516A

3.3 Typical application for PCA9518A

A typical application is shown in Figure 10 below. In this example, the system master is running on a 3.3 V I²C-bus while the slaves are connected to a 3.3 V or 5 V bus. All buses run at 100 kHz unless slave 3, slave 4 and slave 5 are isolated from the bus. Then the master bus and slave 1, slave 2 and slave 6 can run at 400 kHz. Any segment of the hub can talk to any other segment of the hub. Bus masters and slaves can be located on any segment with 400 pF load allowed on each segment.

The PCA9518A is 5.5 V tolerant, so it does not require any additional circuitry to translate between the different bus voltages.

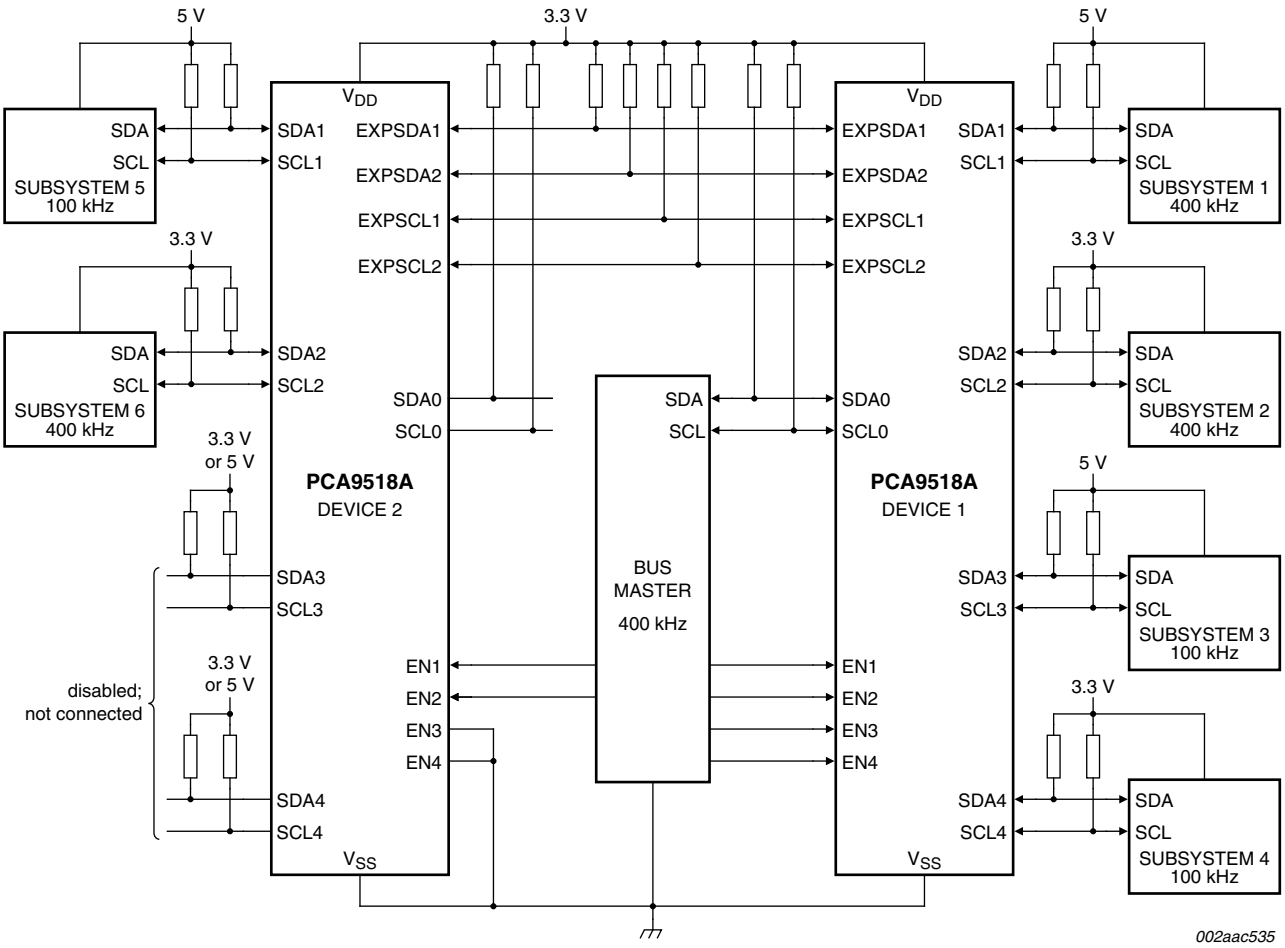
When one side of the PCA9518A is pulled LOW by a device on the I²C-bus, a CMOS hysteresis type input detects the falling edge and causes an internal driver on the other side to turn on, thus causing the other side to also go LOW. The side driven LOW by the PCA9518A will typically be at V_{OL} = 0.52 V at pull-down current of 6 mA.

The PCA9518A includes four open-drain I/O pins used for expansion. Two expansion pins, EXPSDA1 and EXPSDA2 are used to communicate the internal state of the serial data within each hub to the other hubs. The EXPSDA1 pins of all hubs are connected together to form an open-drain bus. Similarly, all EXPSDA2 pins, EXPSCL1 pins, and all EXPSCL2 pins are connected together forming a 4-wire bus between hubs.

Pull-up resistors are required on the EXPxxxn's[1] pins even if only one PCA9518A is used.

EXPSDA1 is the expansion bus that is driven LOW whenever any SDA pin falls below $0.3V_{DD}$. EXPSDA2 is the expansion bus that is driven LOW whenever any SDA pin is ≤0.4 V. EXPSCL1 is the expansion bus that is driven LOW whenever any SCL pin falls below $0.3V_{DD}$. EXPSCL2 is the expansion bus that is driven LOW whenever any SCL pin is ≤0.4 V. The EXPSDA2 returns HIGH after the SDA pin that was the last one being held below 0.4 V by an external driver starts to rise. The last SDA to rise above 0.4 V is held down by the PCA9518A to ~0.5 V until after the delay of the circuit which determines that it was the last to rise, then it is allowed to rise above the ~0.5 V level driven by the PCA9518A. Considering the bus 0 SDA to be the last one to go above 0.4 V, then the EXPSDA1 returns to HIGH after the EXPSDA2 is HIGH and either the bus 0 SDA rise time is 1 μs or, when the bus 0 SDA reaches $0.7V_{DD}$, whichever occurs first. After both EXPSDA2 and EXPSDA1 are HIGH the rest of the SDA lines are allowed to rise. The same description applies for the EXPSCL1, EXPSCL2, and SCL pins.

1. 'xxxn' is SDA1, SDA2, SCL1 or SCL2.



Only two of the five channels on the PCA9518A Device 2 are being used. EN3 and EN4 are connected to V_{SS} to disable channels 3 and 4 and/or SDA3/SCL3 and SDA4/SCL4 are pulled up to V_{DD}. SDA0 and SCL0 can be used as a normal I²C-bus port, but is unused then it must be pulled up to V_{DD} since there is no enable pin.

The pull-ups shown on Device 2 channels 3 and 4 are not required if their enable pins (ENn) are permanently held LOW.

Fig 10. Typical application: multiple expandable 5-channel I²C-bus hubs

4. Additional information

The latest data sheets and IBIS models for the I²C-bus Level shifting family of products and other I²C-bus and SMBus products can be found at the NXP Semiconductors web site www.nxp.com/ics/support/tools.

Software tools for most of NXP Semiconductors I²C-bus products can be found at: www.nxp.com/redirect/demoboard.com.

Additional technical support for the I²C-bus and SMBus Repeater/Hub/Expander family of products and other I²C-bus and SMBus products can be requested by e-mailing the question to: **I2C.Support@NXP.com**.

5. Abbreviations

Table 6. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
MM	Machine Model
MSL	Moisture Sensitivity Level
NDA	Non-Disclosure Agreement
SMBus	System Management Bus

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