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PCB design guidelines for automotive Ethernet

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Document information

Information	Content
Keywords	Automotive Ethernet, EMC, PCB design guidelines
Abstract	Ths document describes best practices and design guidelines for building printed circuit boards incorporating automotive Ethernet devices such as Ethernet PHYs and Ethernet switches.

Revision history

Rev	Date	Description
v.1	20230822	Initial version

1 Introduction

This document describes best practices and design guidelines for creating printed circuit boards (PCBs) incorporating automotive Ethernet products. It discusses a number of issues that need to be addressed in order to satisfy EMC and signal integrity requirements for high-speed communication systems.

The NXP Ethernet switch and PHY product families are optimized for use in the harsh environments of automotive applications. The physical layer used for automotive Ethernet provides transmit and receive capability over a single unshielded twisted pair cable at 100 Mbit/s and 1000 Mbit/s. The so-called PHYs are connected through the MDI interface to the vehicle cable harness, and through a variant of an MII interface to Ethernet switches or microcontrollers/processors. Electronic control unit (ECU) cable harnesses and connectors have a significant impact on the performance of wired communication systems, especially on EMC performance. The design and particularly the layout of a PCB is frequently the root cause of failed ECU-level EMC tests.

Intensive layout planning is mandatory for a successful PCB design. Component placement must be optimized to keep signal traces short and simplify routing. Ground and power planes should be designed first to ensure good power integrity.

Critical signals such as MDI, xMII and clock traces should be routed before other signals. This document describes the steps that need to be followed to achieve an EMC-compliant PCB design.

2 PCB design guidelines for NXP automotive Ethernet devices

This section focuses on topics that need to be considered when designing a PCB containing NXP Ethernet devices. It provides recommendations on the implementation of multipurpose media-independent interfaces MII/RMII, RGMII and SGMII, including multiple implementations of these interfaces. It contains design guidelines for implementing a medium dependent interface, along with power supply rules for the application examples shown in Figure 1.

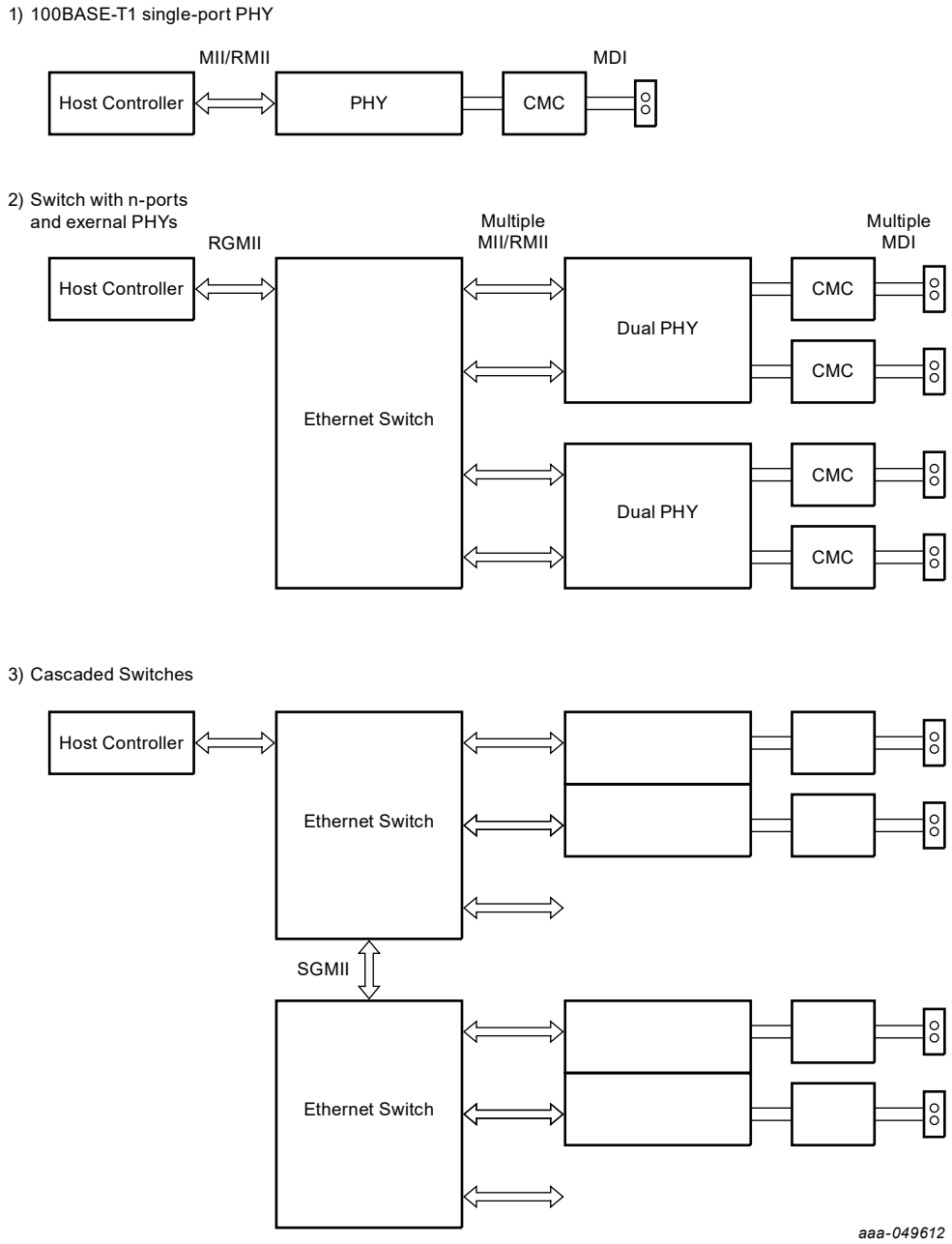


Figure 1. Typical Ethernet switch and PHY application

2.1 MII, RMII interface

2.1.1 Use of inner and outer layers

If the power supply network and grounding is designed as described Section 3, the MII, RMII and RGMII signals (referred to as 'high-speed' signals in this document) should be routed on the outer layers, with a continuous GND return path underneath the signal traces on adjacent layers. If this arrangement is not possible, the high-speed signal paths should be located on the inner PCB layers to ensure as little radiation as possible is generated, paying particular attention to the design of vias. Place vias-to-ground close to the point where the

signal traces change layer (see Figure 2). This provides a path for the return current to change ground plane and helps keep the return current path short.

Placing continuous ground planes above and below the high-speed signals can provide shielding for electromagnetic emissions and decrease radiation and cross-coupling.

Rules:

- Route xMII signal traces on the top or bottom layer if possible, assuming the power supply and ground have been designed properly (see Section 3.2 and Section 3.3)
- Embed (R)MII signal traces on inner PCB layers if power supply network and ground are not designed as described in this document
- Place ground planes above and below signal traces

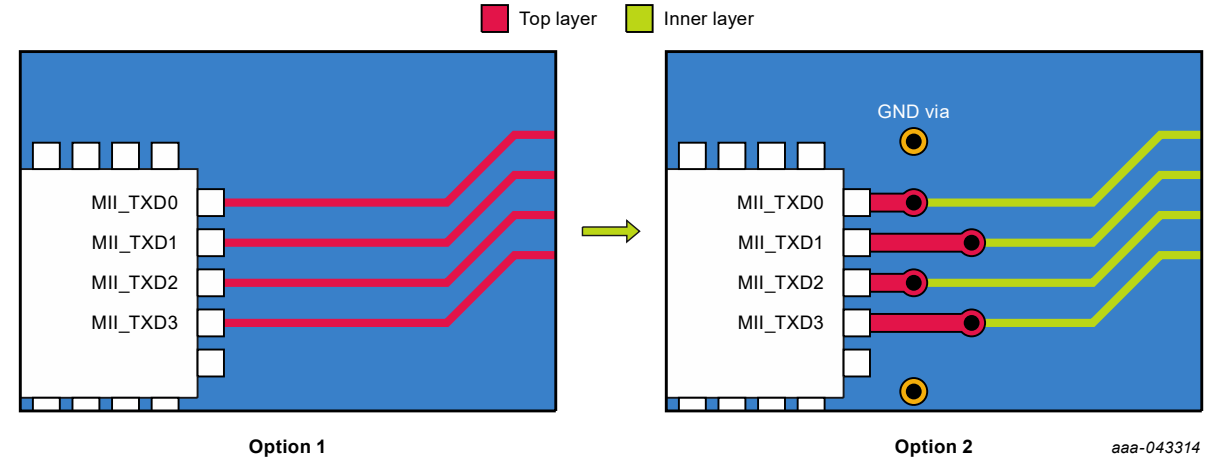


Figure 2. Options for routing high-speed signals (xMII)

The spaces next to the high-speed signal traces should be filled with copper that is connected directly to ground. This reduces external couplings and crosstalk between adjacent signal traces (see Figure 3 and Figure 4).

Try to minimize layer changes, and therefore the number of signal vias, when routing high-speed signals. Through-hole vias are commonly used to implement layer changes. They can act as stubs and lead to impedance discontinuities and signal reflections. Blind or buried vias are preferred where high-speed signals need to change layer. An additional ground trace connected to the local ground plane though regularly spaced vias can reduce coupling by a factor or four. This routing method is recommended if crosstalk is an issue with the board layout.

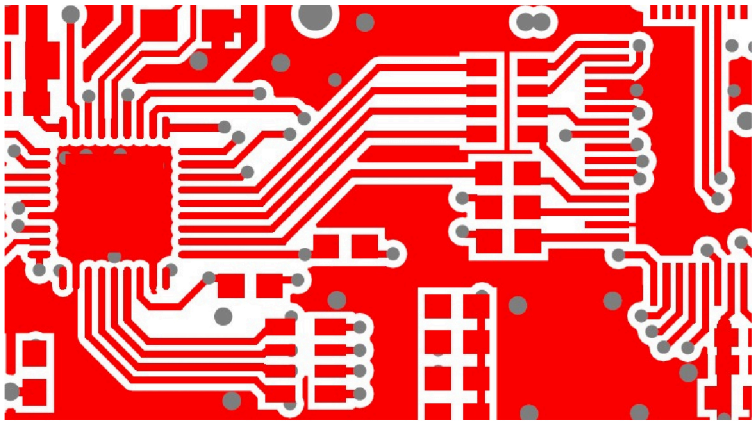


Figure 3. MII signal lines routed to microcontroller on top layer

Rules:

- Fill the space next to signal tracks with copper if crosstalk is an issue
- Minimize layer changes and therefore signal vias when routing (R)MII signals

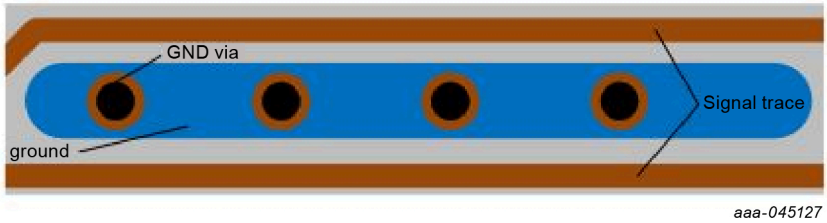


Figure 4. Two signal traces being shielded by a ground trace with regularly spaced vias

2.1.2 Routing and trace distance

Make sure that the distance between adjacent signal lines is at least the width of one signal trace. A better approach would be to increase the spacing to twice the substrate height to reduce crosstalk. This arrangement would prevent the magnetic fields of the signal traces interacting with each other, reducing the current induced in the other traces as illustrated in Figure 5.

Rule:

- Separate adjacent signal traces and (R)MII signals by at least by one trace width or twice the substrate height

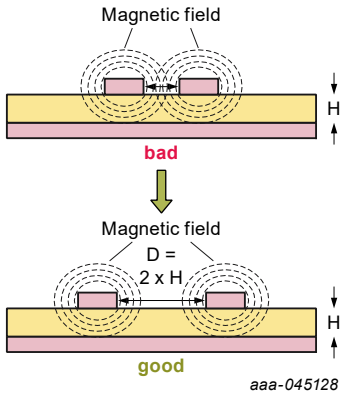


Figure 5. Separation of adjacent signal tracks to avoid interacting magnetic fields

In general, the signal return path should be routed directly above or below the signal trace. Do not cross signal lines on adjacent layers (see Figure 6). Crossing signal lines on adjacent layers causes reflections and result in impedance mismatching leading to signal integrity issues. At least one continuous layer (without slots, crossing traces etc.) should be placed between the crossing signal lines. If possible, route the crossing signal track perpendicular to the crossed signal trace using a stitching capacitor as described in Section 3.2.5.

The MIIx pairs should be routed together on the same layer to ensure the trace length and characteristic impedance are the same.

The length of the MII and RMII pairs should be matched to within 3 mm or less.

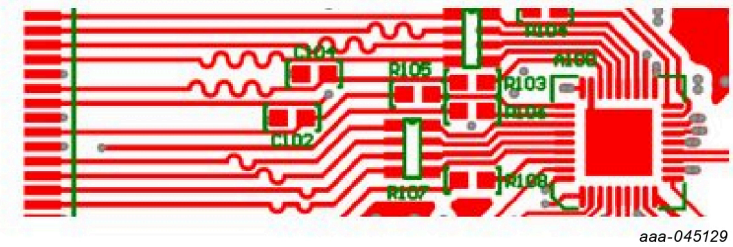


Figure 6. MII signal lines routed to the microcontroller on the top layer

Clock and other sensitive traces should not be designed to run in parallel. To minimize interference, avoid placing traces close to a crystal or oscillator.

Keep power supply lines and (R)MII signal tracks far enough apart to avoid noise coupling into the power distribution network.

To minimize electromagnetic interference, the TX and RX signals on the MII interface should be kept separate.

For reasons of emission, the xMII paths in the layout should be as short as possible - this ensures that the distance between the microcontroller and the PHY is minimized. If it is not possible so to reduce the path lengths sufficiently, an SGMII interface (differential interface) could be used as an alternative.

Rules:

- Do not cross (R)MII signals on adjacent layers
- Route (R)MII pairs together
- Match (R)MII pair length to within 3 mm or less
- Do not run clock traces and sensitive traces in parallel
- Keep power supply lines and (R)MII signal tracks apart
- Separate TX and RX signals

- Keep (R)MII paths as short as possible

2.1.3 Characteristic impedance

MII/RMII lines must be designed as impedance-controlled single-end traces to minimize signal reflections. The characteristic impedance depends on the I/O cell design and should be in the range 50 Ω to 60 Ω.

If a layer change is needed for an MII/RMII trace, it may be advisable to adjust the geometric dimensions. Traces on outer layers with an adjacent conductive plane are called micro striplines; traces on inner layers are called striplines. To achieve the same impedance, the geometries of micro striplines and striplines must be different. When a trace changes layer, the trace width must be adapted. Keeping the same trace width for top and inner-layers results in reflections and impedance mismatching that can generate radiation.

Rules:

- Design (R)MII lines as impedance-controlled single-end traces
- Adjust trace width if a layer change is needed

2.2 RGMII interface

The same design rules described for MII/RMII apply to RGMII. With its higher clock frequency (125 MHz) and faster slopes, pay particular attention to signal integrity and length matching. An example of a well-designed RGMII interface is shown in Figure 7 .

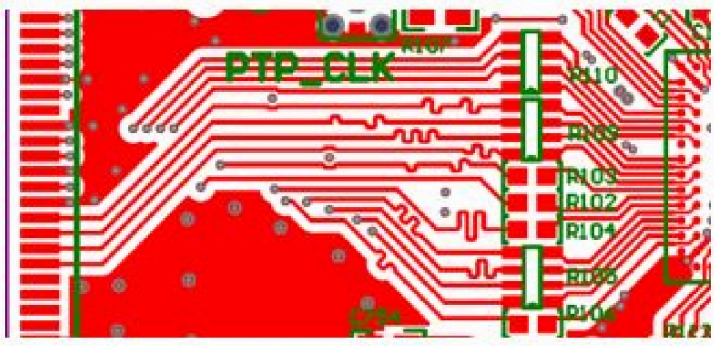


Figure 7. RGMII signal lines on the top layer

2.3 SGMII interface

The same design rules described for the MDI interface (see Section 2.4) apply to SGMII. With its higher clock frequency (625 MHz) and faster slopes, pay particular attention to signal integrity and impedance matching. The skew of the differential signal (see Figure 8) and signal asymmetry can generate common-mode noise, which can lead to increased emissions.

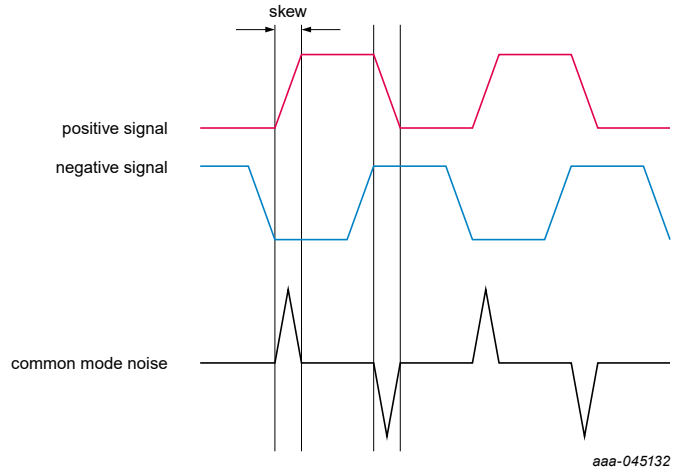
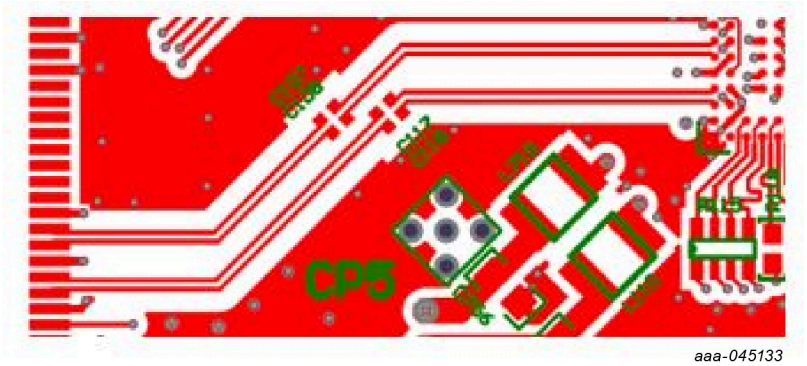
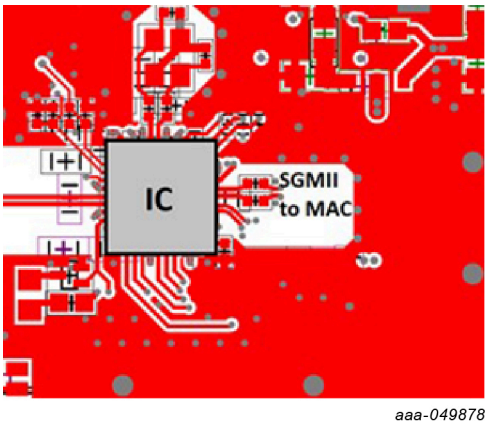


Figure 8. Common-mode noise caused by skew between differential signal pairs

SGMII trace lengths should be matched to within 1 mm or less. Capacitors should be placed as close as possible to the driver (see Figure 9).



a) SGMII signal line design on top layer



b) SGMII capacitors placed close to the driver IC

Figure 9. SGMII trace design and capacitor placement

2.4 Medium-dependent interface (MDI)

2.4.1 Symmetry

The ground planes next to the differential MDI should be as symmetrical as possible. Differences between isolation, component-pad positioning, cut-out-areas etc. can result in bus asymmetry and increased common-mode noise (see Figure 10).

If a continuous ground plane is placed underneath the differential MDI, the isolation to the ground on the top layer should be at least twice the trace width (see Figure 11). Too short a distance between the MDI traces and the adjacent ground can affect the MDI signals and lead to additional skew, which can increase common-mode noise.

Asymmetrical placement of ground vias next to the MDI should be avoided. The vias to the ground plane should be equally spaced. Otherwise, a skew in the signal rise time can lead to an increase in common-mode noise up to the amplitude of the differential signal.

The spacing between the MDI+ and MDI- traces should be held constant. Otherwise, the differential impedance will change and cause reflections. Variations in the distance to the adjacent ground can also affect the trace impedance.

Rules:

- Keep ground connections next to the MDI pair symmetrical
- The distance between the MDI traces and the adjacent ground should be at least twice the trace width

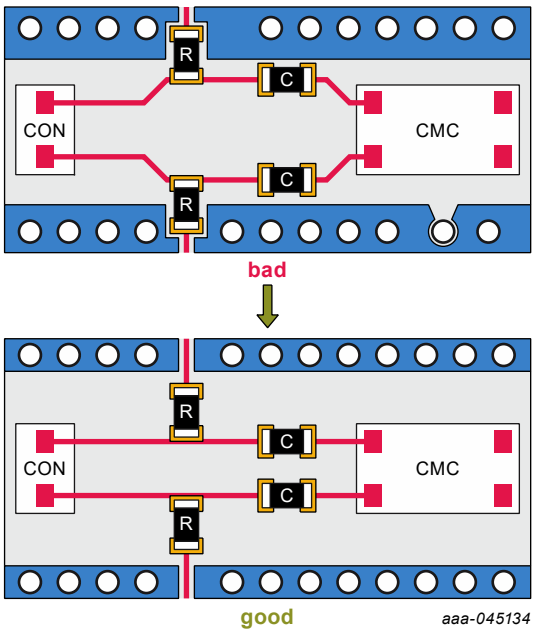


Figure 10. Recommended MDI interface design to ensure a high level of symmetry

The MDI and MII trace lengths should be matched as close as possible to avoid skew and asymmetry. Skew between the MDI+ and MDI- traces can generate common-mode noise.

The MDI pair trace lengths between the connector and choke should be matched to within 1 mm.

Rule:

- Ensure MDI trace lengths between connector and choke are matched to within 1 mm

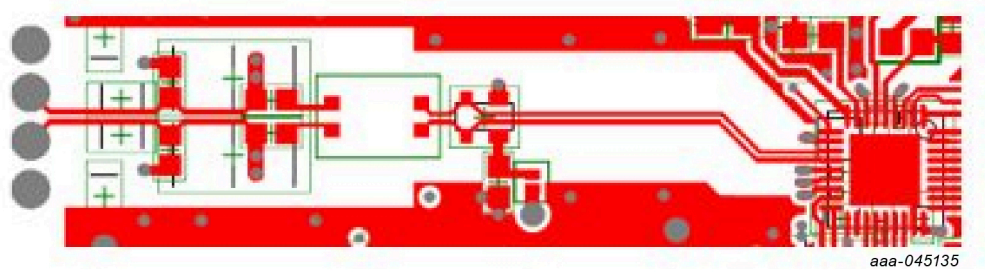


Figure 11. MDI interface design showing a high level of symmetry

2.4.2 MDI routing

Critical signal lines, such as the MDI and the clock, should be routed first. They should be routed manually because the Autorouter results from CAD tools are not always optimal. MDI traces must be routed as edge-coupled microstrips or edge-coupled striplines with 100 Ω impedance.

To avoid potential asymmetry between the traces, route the MDI pair on a single layer. Minimize layer changes, and therefore the number of vias, as far as possible. Consider symmetrical via placement. Via diameter and MDI trace width should be the same.

The MDI+ and MDI- traces should be routed in parallel to ensure differential coupling. Stubs on the MDI should be avoided because they work as equivalent resonance circuits and might lead to antenna effects.

The MDI traces should be as short as possible. Trace lengths between the PHY and board connector can be minimized by placing the PHY near the board edges. This approach avoids signal quality degradation due to the lossy PCB traces. Longer traces can act as antennas, especially in interfaces where steep signal slopes occur (RGMII, SGMII, clock). Small impedance mismatches in the design are more tolerable if trace lengths are short.

To prevent crosstalk, avoid routing multiple MDI signal pairs close to each other. The 5-W rule (see Figure 13 can be applied to ensure sufficient distance between pairs (see Figure 13). If it is not possible to apply the 5-W rule, they should be separated using copper connected to ground.

The MDI ground design between CMC and connector depends on the application.

For unshielded twisted pair cable applications (UTP), it is recommended to cut out the copper between the choke and the connector underneath the MDI on all layers (see Figure 12). This minimizes mode conversion losses (5 db to 10 dB compared to a design with ground) and return losses and prevents crosstalk disturbances. At a minimum, ensure that there is no copper underneath the common-mode-choke to avoid interference.

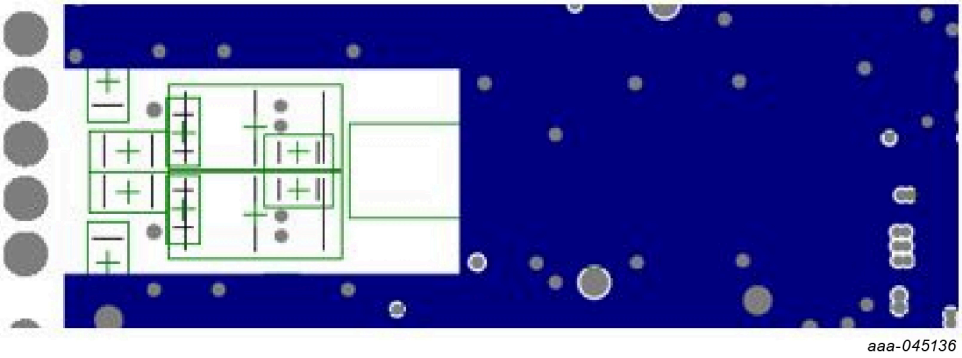


Figure 12. GND cutout between CMC and connector through all layers in UTP applications.

For shielded twisted pair cable applications (STP), it is recommended to decouple the PCB and connector grounds via DC capacitors to keep return current paths short. The ground of the STP cable (shield) is

connected to the connector ground. Therefore, it is not necessary to cut out the copper underneath the MDI. With this robust approach, a galvanic decoupling of the PCBs in the application is guaranteed. Additionally, an AC plate capacitor can be built via layer stack-up to further improve the robustness of the application at higher frequencies. An example is provided in Figure 13.

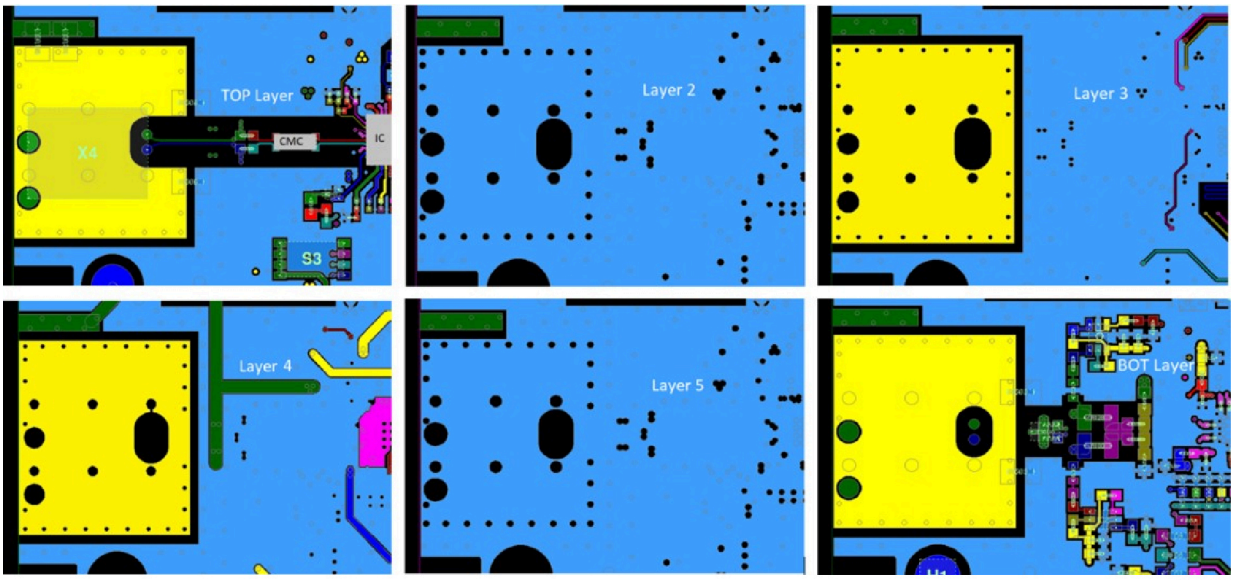


Figure 13. Layout example for STP application (yellow: connector GND, blue: PCB GND)

Rules:

- Route MDI first
- Minimize layer changes and therefore signal vias
- Route MDI pair on a single layer
- Do not route different MDI signal pairs close to each other
- Route MDI+ and MDI- in parallel
- Keep MDI and (R)MII traces as short as possible
- UTP: cut out the copper under the MDI, including between the choke and connector, through all layers
- STP: DC decoupling is recommended with separate connector and PCB grounds

The MDI tracks should be designed with 45° or arc layout. Try to avoid a 90° layout (see Figure 14) for reasons of signal integrity. Stubs should be avoided, especially on the differential signal pairs. Connections to passive components can easily generate stubs. They can lead to impedance mismatching and asymmetry.

Rule:

- Use 45° or arc layout instead of 90° layout and avoid stubs

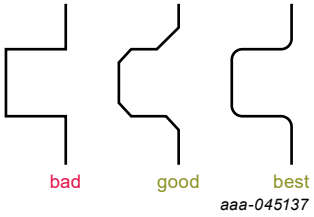


Figure 14. MDI trace layout

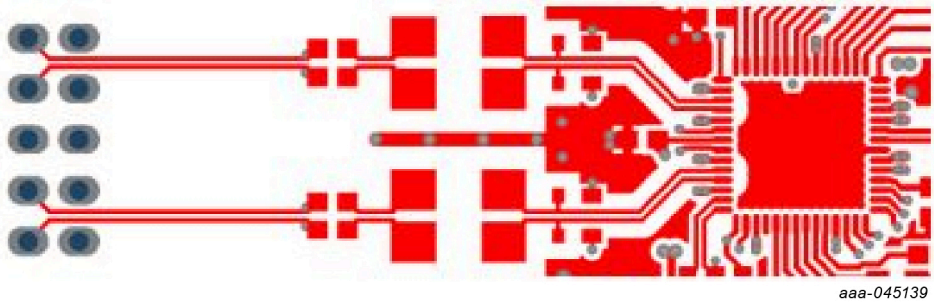


Figure 15. Dual MDI interface design to ensure high level of symmetry

To minimize crosstalk, the spacing between MDI traces (multiple MDI interfaces) and/or to adjacent ground traces should be five times (5-W rule) the width of a single MDI trace. Avoid placing clock and other periodic signals next to the MDI. If this cannot be avoided, the distance to the clock/periodic signal traces should follow the 5-W rule to prevent crosstalk (see Figure 16).

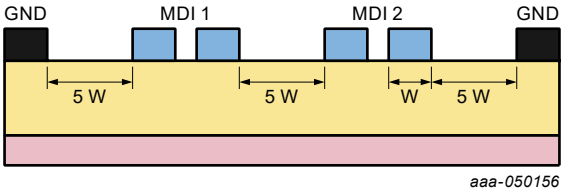


Figure 16. Layout of multiple MDI interfaces to minimize crosstalk

2.4.3 Differential impedance design

The MDI traces should be designed with 100 Ω differential impedance. Route the MDI traces as close as possible to each other for better coupling and low common-mode noise. The minimum distance between the MDI traces is determined by the spacing of the MDI IC pins. For reasons of geometry, the soldering pads of the CMC and DC blocking capacitors should be connected via 45° or arc layout and not via 90° layout. If the IC pitch is greater than the distance between the MDI traces, the geometrical adaptation of the trace impedance should be performed close to the IC pins (see Figure 17).

Rules:

- Ensure 100 Ω differential impedance for MDI pair
- Route the MDI traces as close as possible to each other
- Connect soldering pads of CMC and DC blocking capacitors via 45° or arc layout
- Geometrical adaptation of MDI traces should be performed close to the IC pins

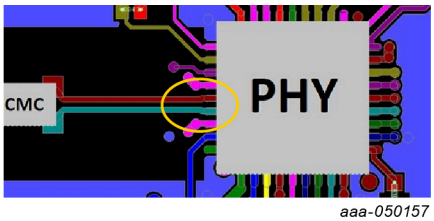


Figure 17. Trace impedance adjustment close to the PHY

The differential impedance depends on the D/H ratio, where D is the distance between the two parallel traces and H is the height of the substrate below the MDI (Figure 18).

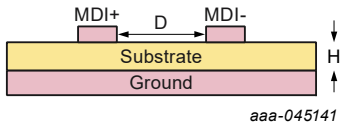


Figure 18. Structure of the MDI traces forming a differential pair

If the copper under the MDI pair is cut out completely, the ground plane next to the MDI pair acts as the reference. In this case, the differential impedance should be calculated using appropriate calculators or software.

2.4.4 Termination network and ESD protection diode

The termination network, along with with the ESD protection circuit, should be placed on the bottom layer (see Figure 19). This arrangement makes routing easier and keeps the differential pair as symmetrical as possible on the opposite layer. A connection to the bottom layer can be made using two vias near the solder pads of the DC blocking capacitors (see Figure 20).

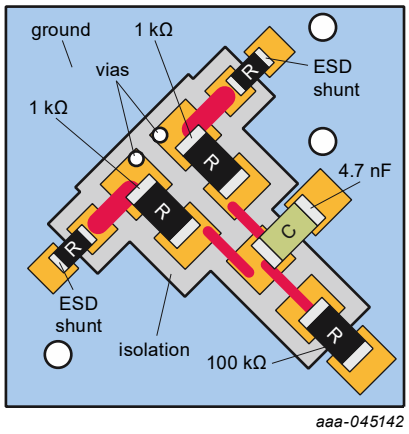


Figure 19. Reference design of termination network on opposite side of IC

Rule:

- Place termination network on the bottom layer

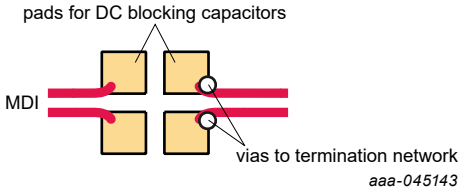


Figure 20. Proposed via connection at DC blocking capacitors

If an ESD protection diode is used, the following layout constraints need to be considered.

Parasitic inductances (e.g. traces, vias etc.) are a major concern when designing ESD protection circuits. The high di/dt (current over time) at an ESD event can lead to large voltage drops over inductances. A small number of inductances can generate tens of volts in the system. Minimizing these parasitic effects is, therefore, key to good ESD design. These inductances are illustrated in Figure 21.

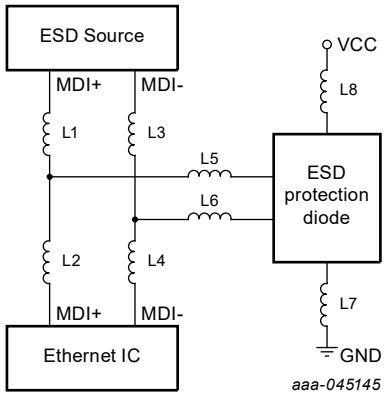


Figure 21. Inductances present on a PCB around ESD protection diode

L1 and L5, as well as L3 and L6, represent the inductance between the ESD source (normally the connector) and the ESD protection device. L2 and L4 represent the inductance between the ESD protection diode and the Ethernet IC. In addition, connections from the ESD protection diode to ground and to the supply also have some inductance.

L1, L2, L3, L4 are normally determined by the trace design of the MDI pair. By making L1 and L3 much smaller compared to L2 and L4, the ESD current can be forced toward the ESD protection circuit. This can be achieved by placing the ESD protection diode as close as possible to the PCB connector, with the Ethernet IC further away This is also very important in terms of electromagnetic compatibility. The rapidly changing ESD current leads to fast-changing electromagnetic fields that can cause interference. Short connections from the connector to the ESD protection diode reduce interference. These connections should be routed with straight traces. Traces with 90° geometry should absolutely be avoided because they can increase radiation. No other traces should be routed close to the connector or ESD protection circuit to avoid noise coupling.

To minimize L5 and L6, the ESD protection diode should be soldered to the MDI tracks to avoid stubs.

To keep inductances L7 and L8 as small as possible, the connections to VCC (if an ESD diode is used) and GND must be kept short and low ohmic. The GND connection is of particular concern. The GND pin of the ESD protection diode should be connected directly to a GND plane on the top layer with multiple stitching vias to adjacent ground planes. The diameter of the GND vias should be as large as possible to ensure low inductance. This helps to minimize the voltage generated by the ESD current.

However, a compromise between GND and ESD structures should be considered when designing the PCB. The design of the ESD structure (traces, pads) should be as symmetrical as possible. The ground underneath the ESD structure should be designed as a plane. Figure 22 shows a possible solution to keep the GND and ESD structures symmetrical.

The ESD protection circuit should be connected to the connector ground to keep current loops short. The termination network should be connected to PCB ground.

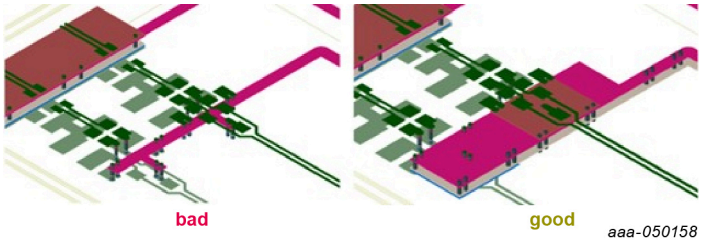


Figure 22. ESD and GND structure for multi MDI-Design

Rules:

- Place the ESD protection circuit close to the connector
- Keep distances to the ESD protection circuit short and, therefore, inductances low
- Solder ESD protection directly onto the MDI tracks to avoid stubs
- Design the ESD structure to be as symmetrical as possible

2.5 Reference clock output

If the device contains reference clock output pins, the dedicated tracks should be shielded in an inner layer between two GND layers for EMC reasons. Traces on the top and bottom layers should be routed as short as possible. Additionally, slew rate control and anti-phase options are configurable via register settings. Further information can be found in the data sheet.

Rules:

- Shield clock traces in inner layer
- Keep clock traces as short as possible
- Use slew rate control and anti-phase options

2.6 MDIO interface

The same rules described for the xMII interface (Section 2.1) apply to the MDIO interface.

The trace impedance for the MDIO interface should have a single-ended characteristic impedance in the range 50 Ω to 60 Ω, depending on the I/O cell design.

The MDIO topology should be routed as 'balanced topology', meaning that the MDIO traces should be well matched with regard to trace length if using multiple MACs/PHYs (see Figure 23).

The MDIO pull-up resistors should be placed as close as possible to the PHY. When using a level shifter between PHY and MAC, an external pull-up resistor should be added on each side of the level shifter (between PHY and level shifter and between level shifter and MAC).

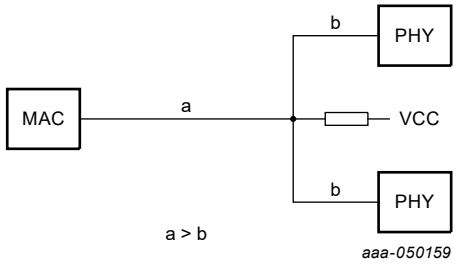


Figure 23. MDIO balanced topology and pull-up at Starpoint

Rules:

- Ensure 50 Ω single-ended trace impedance
- Ensure balanced bus topology
- Place pull-up resistors as close as possible to the PHY
- Use a pull-up resistor on each side when using a level shifter

2.7 Pin-strapping layout

The startup configuration of the IC is often realized via external pin strapping resistors. To avoid impedance discontinuities, pay particular attention to the layout of these resistors. The resistors should, preferably, be placed near the IC and connected directly to the power supply or GND without stubs (see Figure 24).

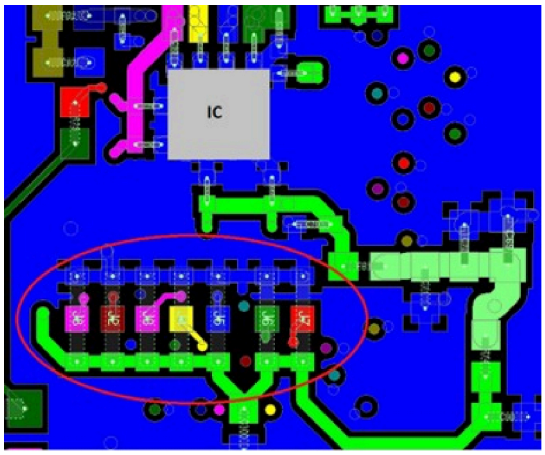


Figure 24. Pin strapping layout near the IC

Rules:

- Place pin-stripping resistors close to the IC
- Connect resistors directly to power supply or GND without stubs

3 General PCB layout guidlines

3.1 General distance rule for signal traces

For signal traces other than xMII and MDI interfaces, a general distance rule applies. The 3-W-Rule states that the distance between traces should be at least three times the trace width as illustrated in Figure 25.

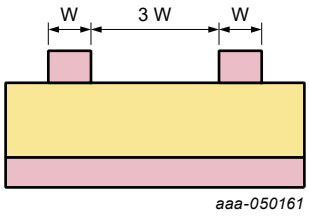


Figure 25. Distance of adjacent signal tracks based on the 3-W-Rule

3.2 Power supply design

3.2.1 Power planes

Power islands and/or power planes (power planes are power islands that capture almost an entire layer) are recommended to ensure a low trace impedance design. Using narrow traces widths to route power distribution network (PDN) traces tends to increase impedance due to parasitic inductance, which can lead to larger voltage drops. Inductance in the PDN may lead to oscillations and ringing on the supply voltage and can generate resonance with existing trace capacitances. These unwanted effects can be avoided with a low impedance design using power islands and power planes. Additional decoupling capacitors can be used to avoid resonance on power supply tracks. If simulation tools are used to calculate the impedance of the power supply, the impedance should be as low as possible over a broad frequency range. At frequencies above 400 MHz, conventional capacitors become less effective. Power islands and power planes are more effective at higher frequencies.

Rules:

- Use power islands and/or power planes
- Reduce trace impedance by increasing trace width
- Use additional decoupling capacitors to reduce resonances
- Avoid long inductive power supply lines, which may act as antennas

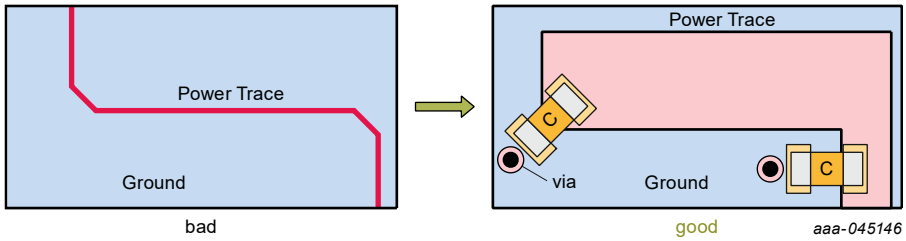


Figure 26. Power trace design with adjacent ground layer

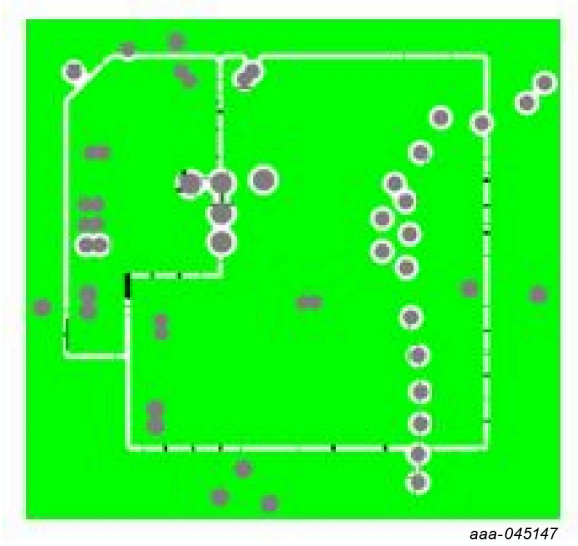


Figure 27. Power supply islands underneath the IC

3.2.2 Decoupling

Decouple PDN traces with a number of regularly placed capacitors (e.g. 10 nF, 100 nF). RF disturbances are shorted to ground by these decoupling or so-called bypass capacitors. They ensure a low-impedance return path for high frequency currents while stabilizing the supply voltage. Decoupling capacitance decreases trace impedance because it is inversely proportional to the trace impedance.

Capacitors can deliver energy at short notice and short high-frequency noise to ground. These characteristics are influenced by the self-resonant frequency (SRF) of the non-ideal capacitor. Above the SRF, capacitors behave like inductors. Decoupling capacitors should, therefore, be chosen according to their SRF and operating frequency range. A common approach is to use several capacitors of the same value. Using capacitors with different values can lead to anti-resonances (see Figure 28). This can cause noise amplification and should be avoided.

Supply lines or power planes that are not decoupled tend to show resonances in their impedance profiles because they exhibit inductance, capacitance and resistance. These structures can lead to antenna effects and disturbances at higher frequencies.

Rules:

- Decouple power supply traces
- Use several decoupling capacitors of the same value rather than different values to avoid anti-resonances

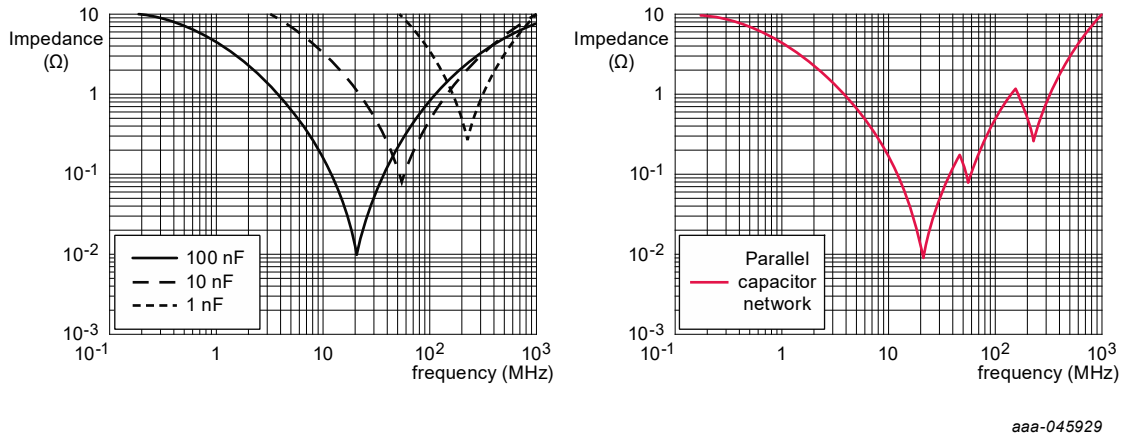


Figure 28. Anti-resonances caused by parallel capacitors with different values and SRFs.

Smaller capacitors tend to have less parasitic inductances and impedance than larger capacitors. Capacitors with smaller dimensions can ensure effective filtering over a wide frequency range (see Figure 29). SRF is higher for smaller capacitors compared with lager capacitors, even for components of the same value.

Smaller component sizes can achieve good decoupling effects up to 2 GHz and can reduce the bill of materials.

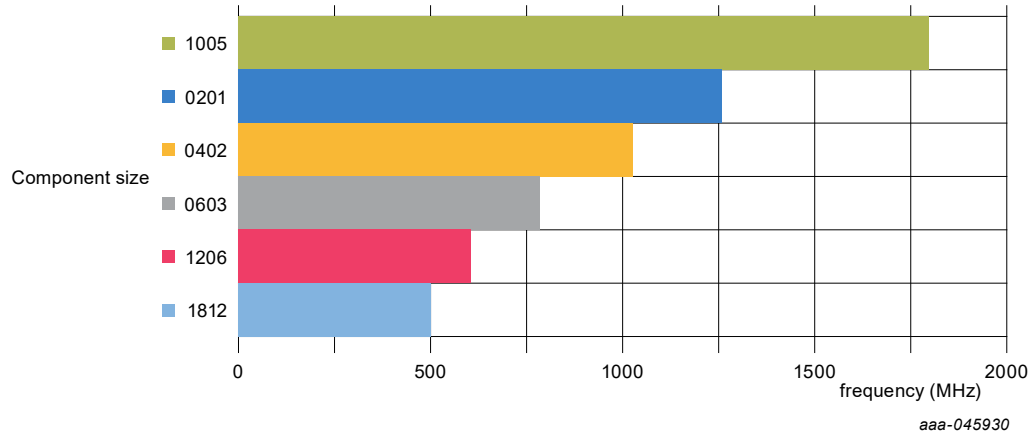


Figure 29. Filter efficiency by capacitor size

Long traces or stubs to discrete components (e.g. resistors, jumpers) should be avoided or minimized (see Figure 30). Additionally, power traces with small cross sections and no decoupling may generate resonances that can, in turn, cause disturbances.

Rules:

- Avoid long traces and stubs with small cross sections

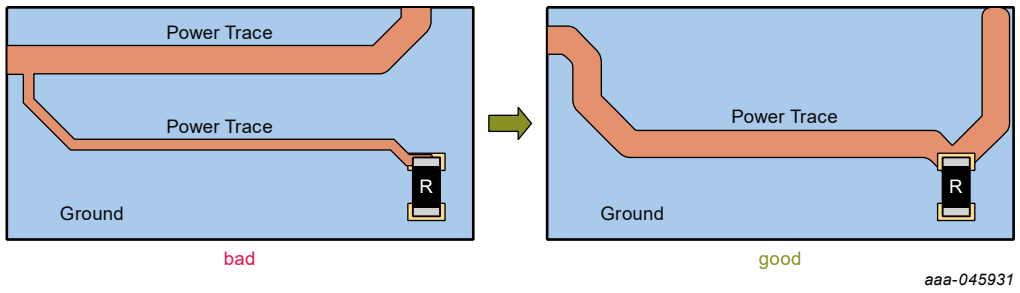


Figure 30. Long stubs to resistors can lead to resonances

3.2.3 Decoupling capacitor placement

Decoupling capacitors should be placed as close as possible to the power supply pins on the IC (see Figure 31). This requirement takes precedence over top/bottom layer preference. Parasitic inductances should be minimized as far as possible. The shortest connections to the IC pins can be achieved using the power planes underneath the IC.

The ground connection of the decoupling capacitor is even more critical and should be prioritized. When using power planes and power islands, placing decoupling capacitor on the opposite layer to the IC is less problematic if the ground connection is kept very short (in the example in Figure 31, the decoupling capacitor is connected to the GND via under the IC).

Rule:

- Place decoupling capacitors close to power supply pins

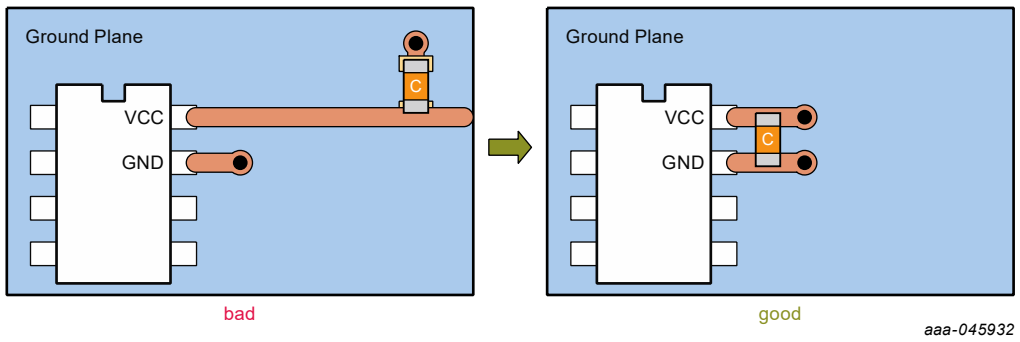


Figure 31. Decoupling capacitor placement at IC pins

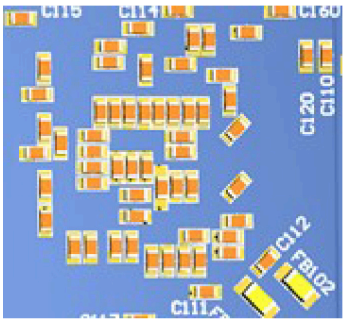


Figure 32. Example showing IC decoupling capacitors on bottom layer

The supply current should first flow through the decoupling capacitor and then through the IC supply pin. Otherwise, disturbances can reach the IC input without being filtered (see Figure 33). In addition, some disturbances generated in the IC can get into the power supply network.

Rule:

- Ensure that the electric field wave generated by the IC reaches the decoupling capacitor before the power supply network

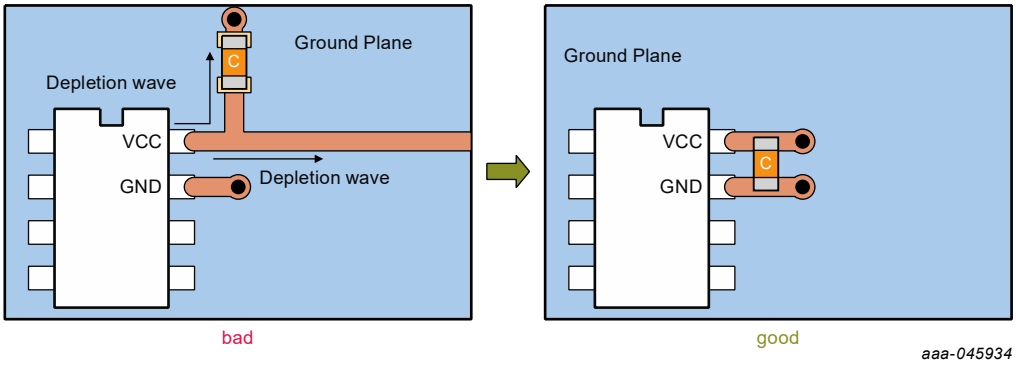


Figure 33. The wave from the IC has to see the energy stored in the capacitor as soon as possible

Use at least one via to GND and one to the power supply for each decoupling capacitor to ensure a low ohmic current path (see Figure 34). Multiple decoupling capacitors sharing a via to GND should be avoided to prevent via stress. Vias should be placed as close as possible to the decoupling capacitors to minimize parasitic effects. Copper connections to the vias should be as wide as is practical to further decrease inductance. Larger vias are recommended as they tend to have lower inductance. If a power supply track changes reference (e.g. from layer 1/5 to layer 2/6), interleaved vias can be used to provide multiple paths for fields to move from one dielectric to another in the PCB stack (see Figure 35).

Rule:

- To ensure a low ohmic connection, connect one or more vias to GND and one or more vias to the power supply for each decoupling capacitor.

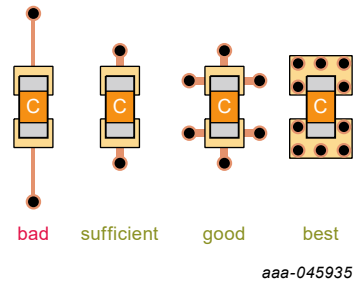


Figure 34. Via connections for decoupling capacitors to power and ground plane

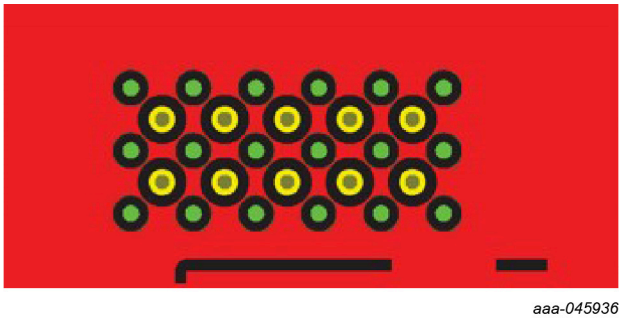


Figure 35. Example: Interleaved power and ground vias

Place the vias for the decoupling capacitor as close as possible to the component (see Figure 36) to avoid increasing the current and to minimize the risk of noise coupling with other structures. Increasing the distance between the vias and the decoupling capacitor generates additional parasitic inductance in series with the decoupling capacitor. Since parasitic inductance lowers the SRF of a capacitor, the overall decoupling effect decreases.

Rule:

- Place ground vias close to the decoupling capacitors

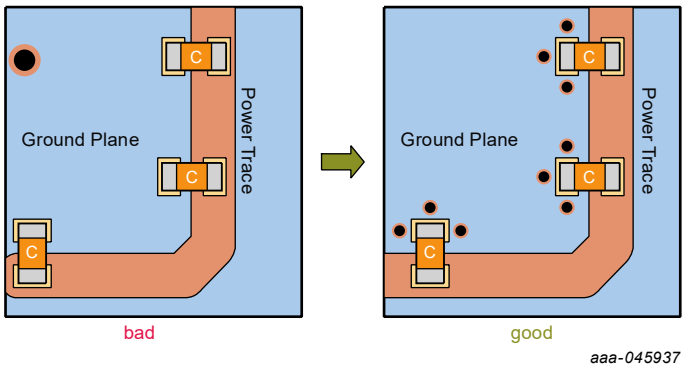


Figure 36. Via connections to ground plane for multiple decoupling capacitors

3.2.4 Power supply integrity

Do not cross power supply planes or traces and high-speed signals on adjacent layers. Doing so can cause coupling to occur! Furthermore, the return current on the high-speed signal traces would need to flow across

this barrier, leading to characteristic trace impedance mismatching. If a crossing cannot be avoided, a continuous ground plane should be placed between the layers containing the power supply and high-speed signal traces (see Figure 37).

Rules:

- Do not cross power supply lines and high-speed signals on adjacent layers
- If it is not possible to avoid crossing supply tracks and high-speed signals, place a continuous ground plane between them

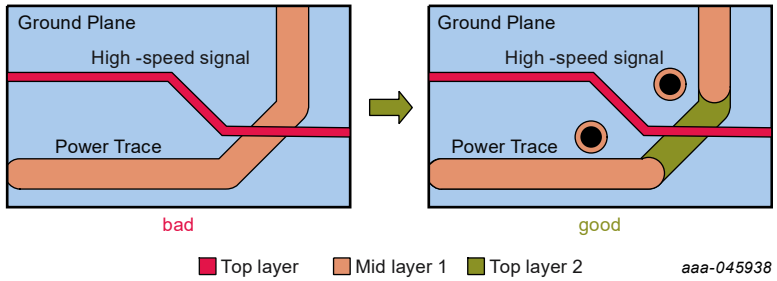


Figure 37. Power supply track design over multiple layers.

3.2.5 Stitching capacitors

Power planes or power islands should not be used as signal references because they are often split into different voltage domains. Crossing signal and power traces on adjacent layers should be avoided to prevent crosstalk.

Rules:

- Avoid using a power plane as reference
- Avoid crossing power and signal traces on adjacent layers

When a critical signal changes layer, the signal reference also changes. A stitching capacitor connected between the two reference planes allows the return current path to flow close to the signal track (see Figure 38).

If a power supply track changes reference (e.g. from layer 1/2 to layer 5/6), a matrix of interleaved ground and power vias can be used to provide multiple paths for fields to move from one dielectric to other dielectrics on the PCB stack (see Figure 35) and, therefore, provide a low impedance connection.

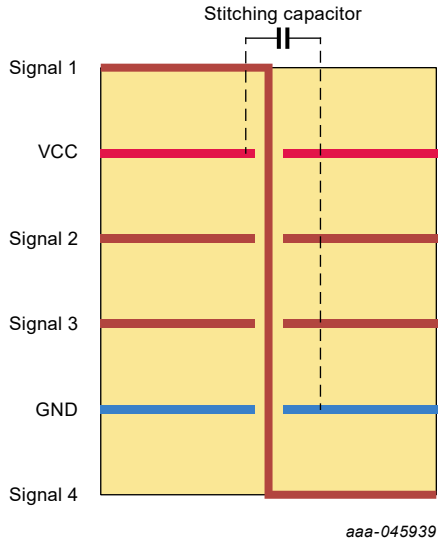


Figure 38. Use of stitching capacitor if a signal track changes layer (VCC is reference voltage)

3.3 Ground design

3.3.1 Ground planes

Use continuous ground planes to provide low-impedance references. A low impedance results in a low voltage drop over a ground plane, minimizing potential differences at the IC pins. This approach also maintains noise margin at the IC input pins, since voltage potentials do not differ between ICs.

Unused spaces on the layers should be filled with copper and connected with multiple vias to GND. These additional measures can provide shielding against disturbances and reduce interference.

Rules:

- Use continuous ground planes
- Fill unused areas on the layers with copper

3.3.2 Cut outs in ground planes

Slots (e.g. other traces) and cut out areas in ground planes should be avoided because they increase the inductance to structures in adjacent layers. This reduces the rise time of crossing signal lines and leads to signal integrity issues. It also increases crosstalk.

Additionally, return currents must flow around these slots (see Figure 39), increasing the likelihood of larger current loops interacting with other return currents and inducing noise in other circuits.

Avoid routing PCB traces over areas without copper created by component isolation or other slots as shown in Figure 39. Routing traces over areas without copper can cause crossing tracks to lose reference.

Rules:

- Avoid slots or cut-out areas in ground planes
- Do not route PCB traces over copperless areas

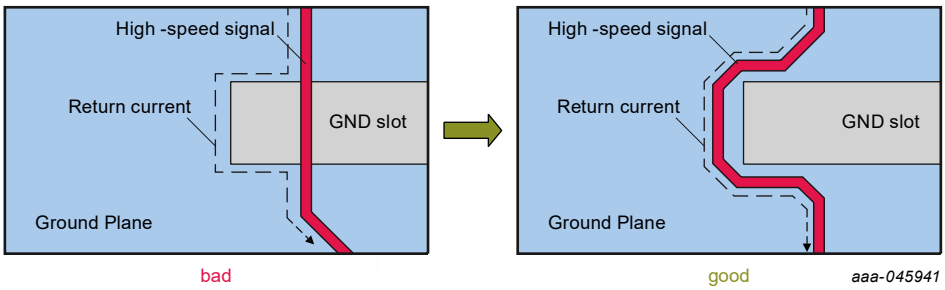


Figure 39. Proposed signal routing when a GND slot is present

Floating ground patches (also known as ground antennas) created when ground patches are not securely connected to an inner ground layer should be avoided. Use enough vias to ensure a low-ohmic current path; otherwise these patches can lead to resonances (see Figure 40).

Rule:

- Avoid floating ground patches

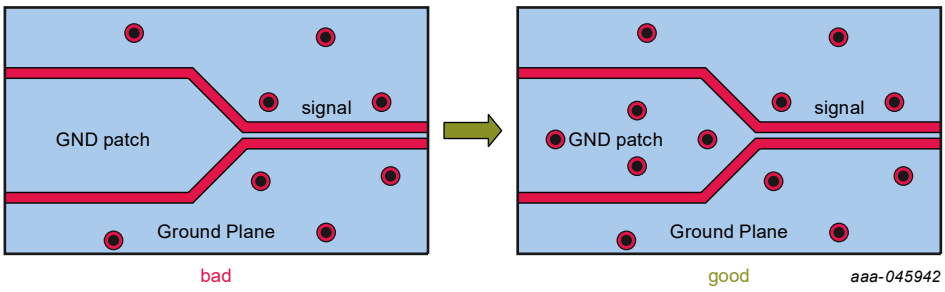


Figure 40. Connection of GND patch to common ground reference

3.3.3 PCB stack-up

In general, higher data rates with steeper slopes generate harmonics at higher frequencies. Impedance discontinuities created by the design of trace lengths, vias, stubs etc. become more important as data rates and frequencies increase. At higher data transmission rates, a more complex PCB stack-up is needed in order to minimize signal integrity issues and electromagnetic compatibility problems. Additional layers help to build low impedance power supply networks over a broad frequency range. Grounding can be improved and radiation from high-speed signal tracks lowered. As systems become more complex, more PCB layers are needed.

At least 6 layers are recommended for designs using automotive Ethernet devices. Figure 41 shows three possible PCB stack-ups. The greater the distance between the inner signal layers, the lower the capacitance between them. This helps to minimize crosstalk. The use of two continuous ground planes in a 6-layer design is the best option, since it increases the probability of an immediate return path and reference for the signal layers. Use thin substrates to reduce the spacing between the outer layers and the adjacent ground layers. This reduces crosstalk between signal tracks, as described in Section 2.1.2.

Keeping narrow spacing between the ground and power layers can reduce inductance and increase the capacitance between them. This helps achieve very low ohmic power supply networks with reduced risk of resonances.

It is possible to use a power plane as reference but it is not recommended because power planes are often split into different voltage domains (e.g. 1V2, 1V8, 2V5, 3V3). This can increase the chances of signal traces crossing different power planes and changing reference as described in Section 3.2.5.

Rules:

- PCB with 6 or more layers recommended
- A layer stack containing at least two continuous ground planes and one power plane is recommended
- Ground should be preferred reference for return currents

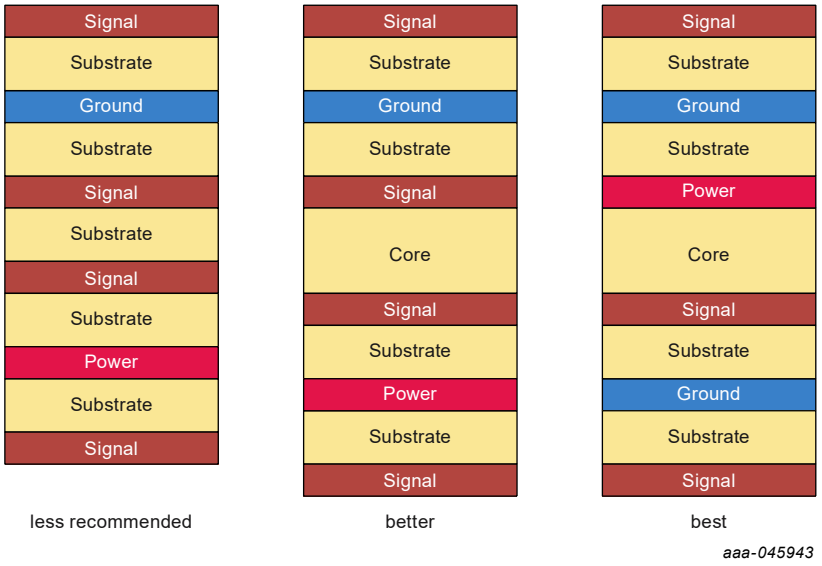


Figure 41. Examples of 6-layer PCB designs

3.4 Vias

Use enough vias to avoid having stresses due to high currents. Vias are characterized by inductance and resistance; the greater the current flow through them, the greater the voltage drop. Therefore, larger vias are needed at higher currents. High currents can generate stronger radial H-fields.

Rules:

- Use enough via to avoid stresses due to high currents
- Take care when designing the geometry of the vias

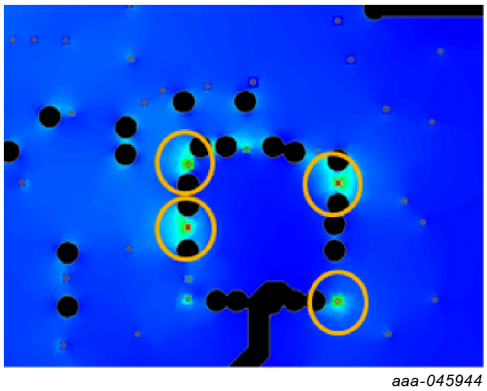


Figure 42. High currents lead to stressed ground vias

Use 'via fencing' at the PCB edges to reduce radially propagated energy from the PCB corners. This involves placing additional vias at the PCB corners to ensure an electrical short circuit between ground planes (see Figure 43). Via fencing can decrease emissions by several dB (up to 20 dB). The more fencing vias used, the less radiation generated at the edges of the PCB.

Rule:

- Use via fencing at the PCB edges

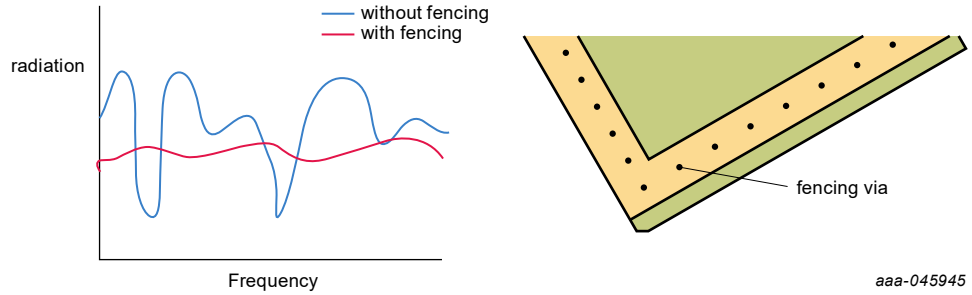


Figure 43. PCB radiation influenced by via fencing

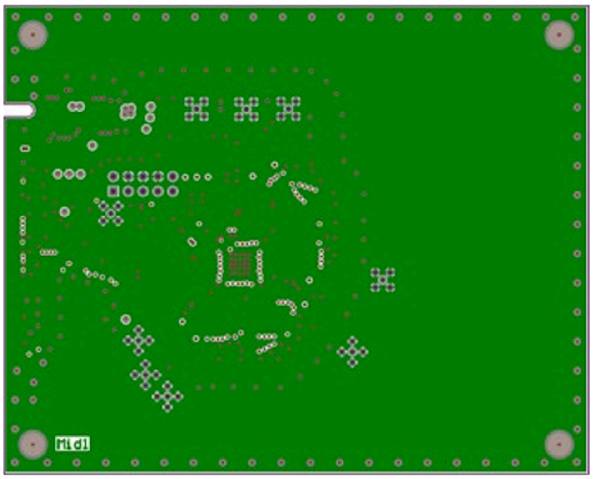


Figure 44. Example showing via fencing

Attention should be paid to via placement to avoid ground slots. Grouping vias too close together can result in PCB areas with increased current density and emissions. In addition, return current must flow around slots created by via-structures (see Figure 45).

Rule:

- Avoid ground slots due to poor via placement

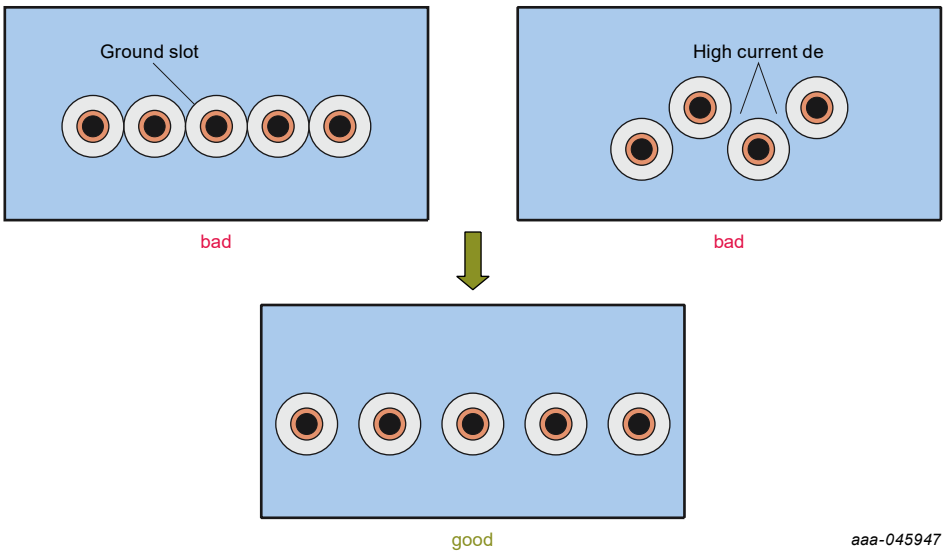


Figure 45. Via placement to avoid ground slots and areas with high current density

3.5 Oscillator design

If an external oscillator is used, the layout should be designed according to the manufacturer's recommendations. A typical oscillator circuit for Ethernet ICs is shown in Figure 46.

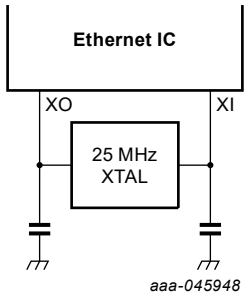


Figure 46. Typical oscillator circuit used for Ethernet ICs

The load capacitors should be chosen according to the manufacturer's specifications. Adding series resistors in the XO and XI paths can improve EMC performance.

Rules:

- To avoid crosstalk, keep the oscillator away from high frequency signals (e.g. clock traces) and devices
- Ground connections for load capacitors should be as short as possible to minimize parasitic capacitance
- Load capacitors should be placed close together
- Route Xtal traces carefully to further reduce parasitic capacitance
- If the IC has a dedicated oscillator ground pin, the ground pins on the oscillator should be connected to this pin with a guard ring; otherwise they should be connected to an adjacent ground layer using multiple GND vias.
- Add series resistors in the XO and XI paths if needed to improve EMC performance

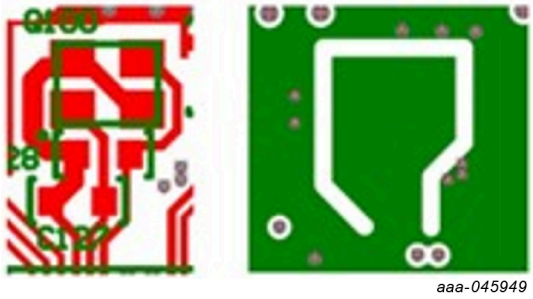


Figure 47. Example of oscillator design on top and second layers

3.6 Level-shifter and SMPS components

Level-shifter and SMPS components, if used, can contribute to emissions in the application so their influence should be carefully considered. The parameters of the components should be matched with the application. Further design features (e.g. shielding) may be necessary to safeguard the EMC performance.

Rules:

- Evaluate the electrical parameters of level shifter and SMPS components
- Consider the use of alternative components with better EMC performance
- Consider adding shielding

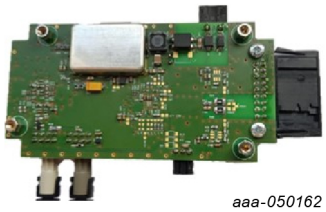


Figure 48. Power supply shielding example

4 Abbreviations

Table 1. Abbreviations

Acronym	Description
BOM	Bill of materials
GND	Ground potential
MAC	Media access control (unit)
MII	Media independent interface
PCB	Printed-circuit board
PDN	Power distribution network
PHY	Physical layer (device)
RGMII	Reduced gigabit media independent interface
RMII	Reduced media independent interface
SGMII	Serial gigabit media independent interface
SRF	Self-resonant frequency

Table 1. Abbreviations...*continued*

Acronym	Description
STP	Shielded twisted pair (cable)
UTP	Unsielded twisted pair (cable)

5 References

[1] 802.3bw-2015 - IEEE Standard for Ethernet Amendment 1: Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair Cable (100BASE-T1), 26th October 2015, IEEE-SA Standards Board

[2] IEEE 100BASE-T1 EMC Test Specification for Common Mode Chokes, Version 1.0, Oct. 2017, OPEN Alliance [3]
IEEE 100BASE-T1 EMC Measurement Specification for Transceivers, Version 1.0, Oct. 2017, OPEN Alliance

[3] OPEN Alliance Automotive Ethernet ECU Test Specification, Version 2.0, July 2017, OPEN Alliance

[4] A printed Circuit Board reference design for physical layer of 100BASE-T1 automotive Ethernet; April 2019; NXP Semiconductors Germany GmbH

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